Design Methodology for a Planarized High Power Density EV/HEV Traction Drive using SiC Power Modules

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***Abstract*— This paper provides a methodology for overall system level design of a high-power density inverter to be used for EV/HEV traction drive applications. The system design is guided to accommodate off-the-shelf SiC power modules in a planar architecture that ensures proper electrical, thermal, and mechanical performances. Bi-directional interleaved DC-DC boost structure and a three-phase voltage source inverter (VSI) have been utilized with the primary focus on the size, weight and loss reduction of passive components. A stacked layer approach has been used for a unique PCB-based busbar, ultra-low profile gate driver, and controller board. This holistic design approach results in a highly compact traction drive inverter with power density of 12.1 kW/L that has lower volume and weight compared to the commercially available state-of-the-art power converter systems.**

Keywords—EV; HEV; SiC; wide bandgap; high power density; bidirectional DC-DC converter; inverter thermal design; passive component design.

I. INTRODUCTION

The push for electrification of the transportation sector for combating climate change is and will remain a major focus of national governments and worldwide automotive manufacturers. Currently, the transportation sector contributes to approximately 30% of the greenhouse gas emissions annually [1]. Therefore, electric drivetrains in industrial, commercial, and consumer vehicles provide a feasible, high impact solution to the climate and energy crisis. Further penetration of EV/HEVs into the transportation sector is bolstered by the advent of commercially available Wide-bandgap (WBG) power semiconductor devices and power modules, specifically SiC-based technology that offer system level benefits to electric drivetrains [2]-[3]. The main advantages of WBG power semiconductor devices over conventional Si semiconductors include greater voltage and current handling capabilities, higher maximum operating temperatures, and faster switching [4].

This paper provides a complete EV/HEV electric drivetrain design methodology capable of producing a stacked, planarized topology. Commercial off-the-shelf (COTS) SiC power modules from Wolfspeed (SKU: CCS050M12CM2) are the centerpiece of both the DC-DC boost and inverter stages. The remaining passive components of the power plane, signal plane PCBs, and cold plate are optimally incorporated into the inverter design around the SiC power modules. In Fig. 1, the planarized design approach of the overall system can be seen. The system constitutes of several stacks for each subsystem, from the inductor at the bottom to the integrated cold-plate in the middle layer and SiC power modules on the top. Further stacks have been added for interconnect in the form of a PCB based busbar. A low-profile gate driver and controller board has been developed alongside. This system level integration approach results in a motor drive inverter with significantly reduced volume and increased power density while providing very high efficiency. The presented design approach is currently on track to meet the DoE's 2020 targets for EV/HEV power density requirements.

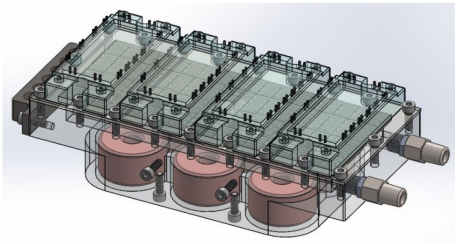

Fig. 1. High-power density EV traction drive

II. PLANARIZED INVERTER DESIGN

A. System Topology

The system topology of the traction drive consists of a two-stage bidirectional power converter developed to energize a 3-phase permanent magnet synchronous machine (PMSM) commonly used in EV/HEV powertrains. The topology is shown in Fig. 2.

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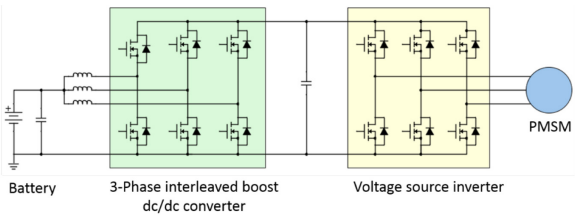


Fig. 2. System topology.

A bidirectional DC-DC converter has been utilized for stepping up the low battery voltage (typically 200 V-450 V) to the DC-link bus voltage of 200 V – 700 V with an interleaved structure to significantly reduce the input DC current ripple as well as providing flexibility to the DC bus stage. The boost topology provides the opportunity to employ a high DC bus voltage which can be varied depending on the system operating condition. The back-end is composed of a typical voltage source inverter (VSI) to provide necessary 3-phase power to the motor. The overall symmetry of the topology greatly simplifies the adoption of a planarized system design philosophy and contributes significantly in reducing the overall system volume.

B. Thermal Design

Power semiconductor devices and the passive components, specifically the inductors, in an electric drivetrain require cooling in order to operate below their fusing currents and maximum junction temperature. Ultimately, the more effectively heat can be extracted from the power modules and the inductors, the more current can be pushed through the electric drivetrain, resulting in higher power density [5]-[7]. Effective cooling also ensures long-term reliability as most failure mechanisms in electronics are due to the inability to remove heat from the active and passive components [8]-[10].

The system level packaging approach, level 2 (package-on-board) and above, facilitates the thermal extraction. Based on the planar, stacked structure design methodology a cold plate mounted directly to the baseplate of the power modules is required to provide cooling. A multi-physics simulation was done to analyze the ΔT within the module for a single phase-leg using boundary conditions derived from the cooling method.

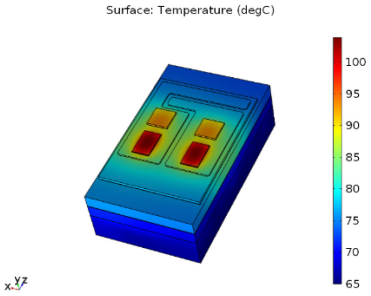


Fig. 3. Phase-leg surface temperature within the power module.

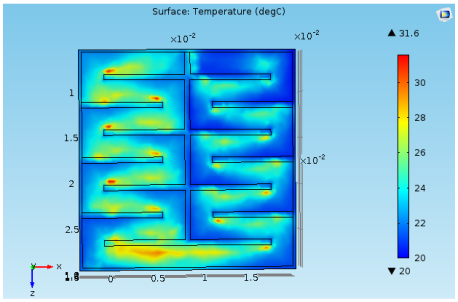
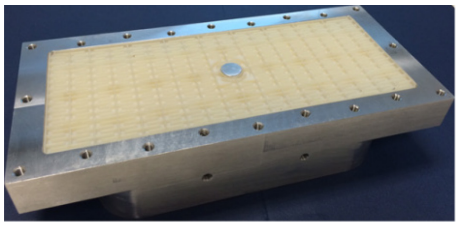


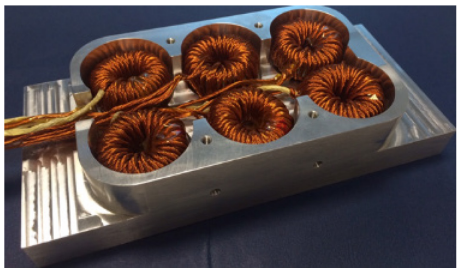
Fig. 4. Surface temperature simulation of turbulator cell beneath power module baseplate.

Improved system-level thermal management, with little thermal gradient across all four power modules and six inductors, is achieved using an impingement cooling technology. The approach is based on ShowerPower cooling technique developed by Danfoss that proved to be scalable for the total baseplate footprint of the power modules [11]-[13]. Simulations are run on a unit cell of the cold plate for verification (Fig. 3-4).

A high power density design requires functional integration. Cavities were created within the base of the cold plate to house the inductors. A potting material was poured over the inductors to thermally, and mechanically integrate them into the electric drivetrain. Here, a thermoset SC-320 thermally conductive silicone encapsulant from LORD Corporation was used, as it offered relatively high thermal conductivity (3.2 W/m-K) along with mechanical strength (Shore A hardness of 60) [14]. The footprint area of the cold plate derived from the planarized layout of the power modules acts as a design constraint for the inductor topology (this will be further discussed in the following section). The functional integration of the cold plate can be seen in the Fig. 5 below, following the stacked, planarized design methodology that has been enumerated thus far.



(a)



(b)

Fig. 5. (a) Customized turbulator using Danfoss ShowerPower cell structure, (b) Integration of boost inductors into the cold-plate for active cooling.

The remainder of the inverter drive circuit can be designed with the power modules and the inductors being provided the necessary cooling to meet the motor requirements.

C. *Passive Component Design*

The interleaved DC-DC boost topology enables significant reduction in the ripple current supplied from the battery which has positive impact on the battery lifetime. Also, on the DC-bus side, lower ripple current in the DC bus capacitors can be observed which results in lower requirements on the DC-link bus capacitors [15]-[17].

Interleaved boost structure inherently requires multiple boost inductors and increased number of switches. However, this tradeoff can be balanced by proper selection and sizing of the passive components. To exploit the commercially available 6-pack SiC switches, a three-phase boost topology has been employed. By proper switching scheme, the ripple current on the input side has been reduced significantly (Fig. 6(a)).

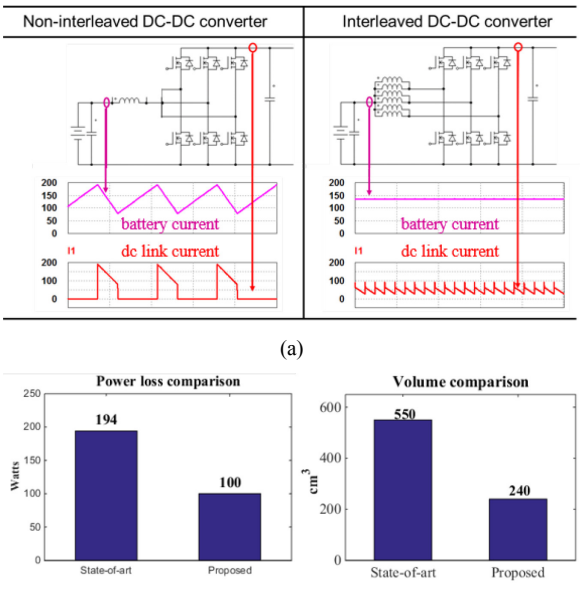
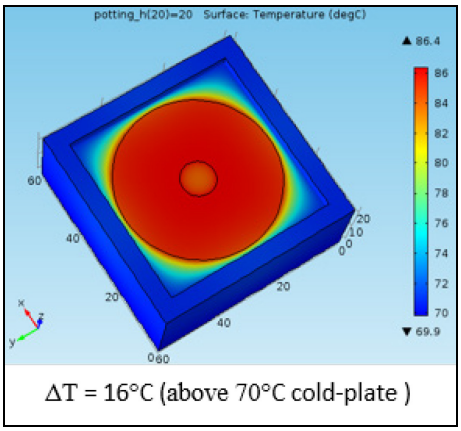


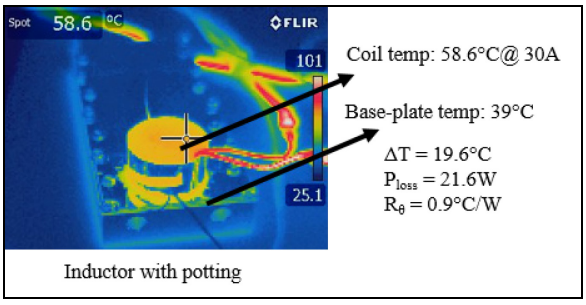
Fig. 6. (a) Comparison of current ripple between conventional boost and interleaved boost DC-DC converter, (b) Power loss and volume comparison between six interleaved boost inductors and Gen-III Toyota Hybrid System (THS).

Also, the high switching frequency of the boost stage (70 kHz) enables the considerable downsizing of the inductors. Compared to the multi-gapped JNEX sheet core boost inductor used in the Gen-III Toyota Hybrid System (THS-III), powder core materials with distributed air gap has lower core loss at high frequency operation with excellent DC bias characteristics along with good thermal reliability and relatively low cost [18]-[19]. By parallel connection of six toroidal inductors to make a three-phase boost inductor, a significant reduction in power loss and volume (Fig. 6(b)) has been achieved. Thermal management of the boost inductors is required and as such the inductors have been integrated into the custom-designed cold-plate (Fig. 5(b)) and potted with a thermally conductive silicone based encapsulation material, as evident from the thermal simulation ((Fig. 7(a)) and experiment (Fig. 7(b)). For physical realization of the inductors, toroidal "High-flux" powder core from Chang Sung Corp. has been used with inductance designed at 110 µH @ 25 A for 70 kHz switching frequency.

A similar distributed strategy has been employed in designing the DC link bus capacitor. The DC bus architecture takes into account the voltage and current ripple, voltage transients and resonance [20]. A low-inductance high-current film capacitor can replace the conventional bulky electrolytic DC-bus capacitors [21]. Further improvement has been achieved by using multiple smaller polypropylene film based DC capacitor as a shunt configuration significantly reduces the current requirement. Localized *dV/dt* issue due to high frequency switching can be mitigated by employing high-frequency ceramic-type snubber capacitors with higher than 2 MHz self-resonance frequency, which will significantly reduce the voltage spikes in the SiC MOSFET switching signals. Proper power balancing between the DC-DC and DC-AC converter further decreases the energy storage requirement of the DC-bus. During hardware design, automotive grade MPP capacitors from Vishay has been selected for their inherent low ESL and ESR, as well as the overall geometry that enables easier integration to the overall system. The high temperature resilience is also a key feature that supports the use of these capacitors for EV/HEV traction drive applications.



(a)

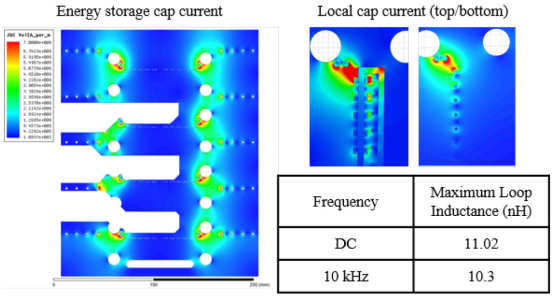


(b)

Fig. 7. (a) Thermal simulation of inductor with potting compound, (b) Experimental thermal profile of inductor with potting.

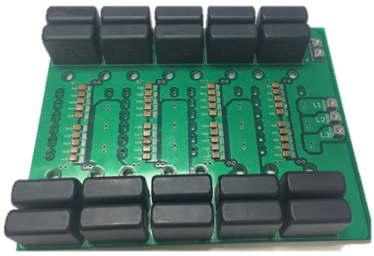
D. Busbar Design

For the power stage interconnection, a PCB-based busbar falls in line with the stacked layer approach and the planarized design philosophy. Typically, high power busbar is designed with copper sheets with the dimensions and geometry dictated by the effects of high-frequency currents with the goal to minimize parasitic inductance and increase electromagnetic compatibility [22]-[24]. Routing of high current conductors through a multi-layer PCB reduces the overall volume while adding flexibility. The multi-layer busbar with thick copper traces (4 oz.) has been designed to minimize the overall loop inductance [25] (Fig. 8(a)), and also enables the mounting of the DC-bus and local snubber capacitors in a symmetric layout utilizing the minimum amount of space (Fig. 8(b)). The physical placement of the power modules has been taken into the design criteria such that the copper traces are connected directly onto the module pins. A "pass-through" design has been chosen so that relevant pins needed for device gating purposes are available for direct connection from the top-layer of the PCB busbar.



Frequency	Maximum Loop Inductance (nH)
DC	11.02
10 kHz	10.3

(a)



(b)

Fig. 8. (a) Simulation of parasitic loop inductance of half-bridge power module, (b) Assembled PCB-based busbar with DC-link and snubber capacitors.

Following the "stacked" architecture, an "Ultra-low profile" gate driver with focus on high switching frequency capability, high dV/dt immunity, and a high-bandwidth controller board have been developed concurrently. An integrated approach has been taken so that the controller board and the gate driver follows the same design language of the PCB busbar and thus connects to the power modules and the cold-plate into a very dense structure. Overall volume and weight can be reduced significantly following this methodology.

III. Experimental Results

The SiC traction drive rated at 55 kW (peak) has been designed and fabricated (Fig. 9) following the design process explained in the previous section. A low-profile high-frequency isolated gate driver board has also been designed at the same time [26].

The planarized design has been implemented in the power stage using four CREE SiC 6-pack module, while the cold-plate, PCB busbar and the gate driver has been integrated in a stacked structure, yielding a total system volume of 4.5 liter corresponding to a power density of 12.1 kW/L.

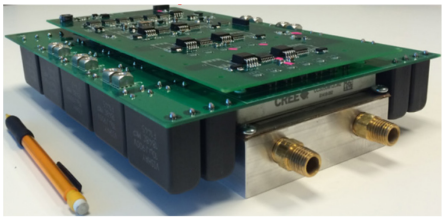


Fig. 9. 55 kW traction drive power converter with cold-plate, power modules, PCB-based busbar, and gate driver.

The cold-plate has been attached to a cooling loop representing a system typically found in HEV applications, and temperature and pressure gauges have also been used to monitor the various system variables.

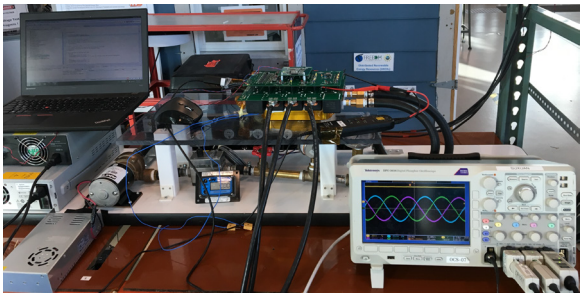
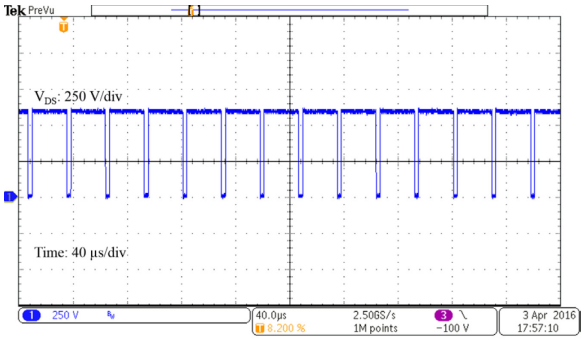


Fig. 10. Hardware test set-up.

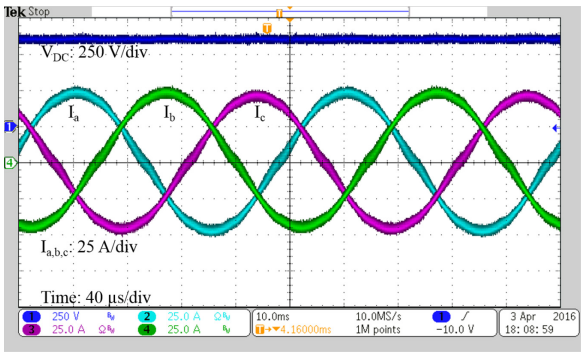
The system has been tested for 15 kW continuous power with static RL load with R = 9 Ω and L = 500 µH per phase. The space vector PWM based drive controller algorithm has been implemented in a dual-core Delfino F28377 based DSP from Texas Instruments.

The voltage and current waveforms for 15 kW continuous power test are shown in Fig. 11. The drain-to-source voltage (VDS) of the one of the bottom switches of the inverter, as seen in Fig. 11(a) demonstrates the absence of noticeable voltage spikes during the switching transients and thus verifies the low-inductance system design as mentioned in the previous section. This is also evident in Fig. 11(b) where the DC bus voltage is free from significant ripple as well. The line current waveforms in Fig. 11(b) also shows that high-frequency current ripple is also minimized.

Using a Yokogawa WT3000 power analyzer, the input-output efficiency has been measured for the 3-phase inverter stage, as shown in Fig. 12 (a-b). The measured peak efficiency for the inverter stage is approximately 99%.

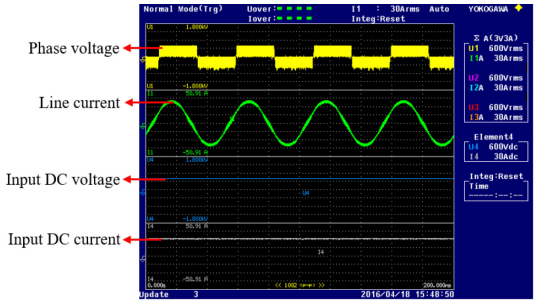


(a)

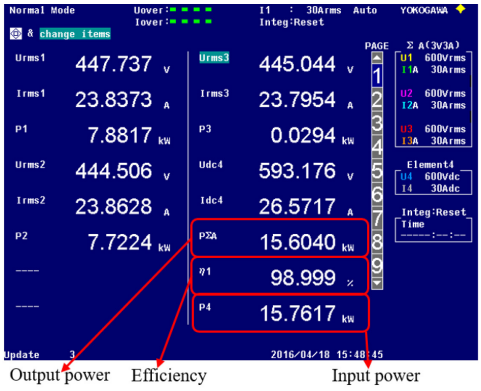


(b)

Fig. 11. 15 kW continuous power test waveforms using static (R-L) load: (a) Drain-to-source voltage of 600V and (b) DC link voltage and 3-phase output current (line-to-line).



(a)



(b)

Fig. 12. Power efficiency calculation for 15kW inverter operation.

As shown in Fig. 13, the thermal performance has also been evaluated using an infrared camera from FLIR. The thermal performance at 15 kW continuous power level shows acceptable increase in temperature (ΔT) compared to an ambient temperature of 25°C.

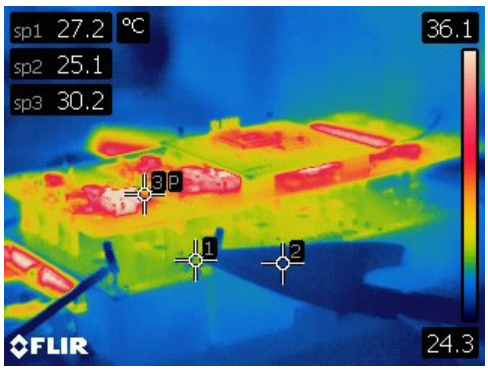


Fig. 13. Thermal profile of the inverter operating at 15kW

Effiency measurement at varying power levels (Table I) demonstrates the trend of the power conversion efficiency of the system (Fig. 14), and validates the design target of 99% inverter efficiency at rated power level.

TABLE I. POWER EFFICIENCY MEASUREMENT

Input power (kW)	Efficiency (%)
3.63	96.98
6.63	98.03
9.75	98.58
12.69	98.97
15.76	99.00

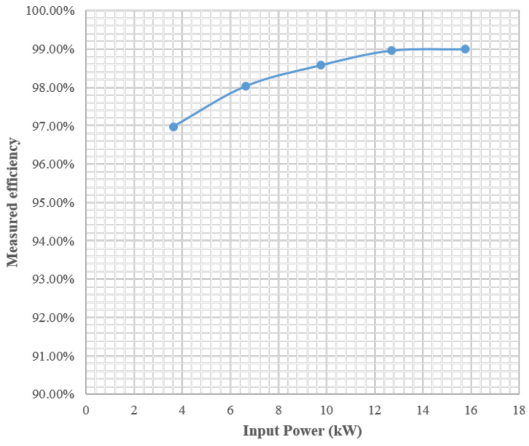


Fig. 14. Inverter efficiency plot.

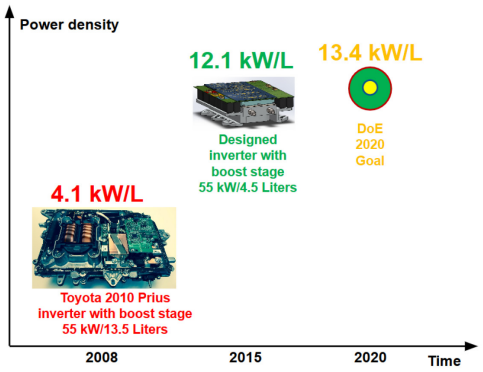


Fig. 15. Power density comparison of 55kW traction drive using SiC, Gen-III THS, and 2020 DOE goal

The planarized EV boosted-inverter design presented achieved a 3X greater power density compared to the 2010 Toyota Prius boosted-inverter. The design is on target for meeting the U.S. Department of Energy goal of 13.4kW/L by 2020 as shown in Fig. 15.

IV. CONCLUSION

Engineers of electric drivetrains for transportation applications are provided with a design methodology for WBG traction inverter. The design, centered around a multi-physics packaging approach, enables high power density. The stacked, planarized topology exploits the inherent characteristic advantages of SiC technology over its Si counterparts. Key features of the proposed design are as follows:

1) Commercially available low-profile SiC module has been used in a planarized design that is suitable for stackable approach for system level integration.

2) Customized cold-plate design enables simultaneous cooling of SiC power modules and inductors further improving power density.

3) Low-profile PCB busbar based interconnect enhances the parasitic reduction of the system.

4) Passive component sizing has been optimized for improved performance and efficiency as well as tighter system integration.

All these key features together result in a high-power density, high-efficiency inverter with a variable DC bus and wide input battery voltage range, which is ideal for EV/HEV traction drive. These features have been verified using a 55 kW prototype.

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DISCLAIMER

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