Advanced Multi-physics Simulation for High Performance Power Electronic Packaging Design

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***Abstract*—Power electronics packaging is required by almost all areas of power electronics applications, such as consumer electronics, automotive, aircraft, and military applications. Due to the significant heat dissipation from the switching behavior of power semiconductor devices, the interactions between thermal, electrical and mechanical aspects become very important to not only power electronics packaging design, but also long-term reliability of power modules. The interactions become more and more significant as the development of wideband gap power semiconductor devices has pushed the power modules to be able to operate at higher voltage levels, higher ambient temperature and higher switching frequencies. Power module development relies more and more on Finite Element Method (FEM) based multi-physics simulations, reducing design cycles, to couple the electrical, thermal and mechanical fields in simulations of different processes such as power module assembly, operations and reliability assessments. In this paper, several cases were introduced to demonstrate how multi-physics simulation worked in power module development. The first case was the simulation of the fringing effects to estimate the difference between practical parasitic capacitance value and theoretical parasitic capacitance value of double-side metallized ultra-thin ceramic. The second case was the pre-stress analysis of power module substrate made of a specific ultra-thin ceramic. The third case was the study of electrical field distribution and temperature distribution in a high voltage and high temperature Silicon Carbide power module. The last case was parasitics extraction of a PCB busbar for 50 kW Electric Vehicle Motor Drive Applications.**

Keywords—multi-physics simulation; finite element method; power electronics; power module; packaging

I. INTRODUCTION

As the demand for power electronics becomes significantly increasing in various areas such as automotive, aerospace, green & renewable energy industry, semiconductor based power modules are essential for power delivery with high efficiency. The further improvements in the performance, reliability and cost-effectiveness of electric energy processing systems cannot be realized without the integrated system approach based on the advanced packaging of new generations of semiconductor devices [1]. Due to the heat dissipation from the switching behavior of power semiconductor devices in power modules, interactions between thermal, electrical and mechanical aspects in power modules are important to power electronics packaging design and long-term reliability. As Wide bandgap (WBG) semiconductor devices has shown superior materials properties enabling potential power device operation at higher temperature, voltages, and switching speeds than Si technology, the use of WBG semiconductor devices will improve the performance of existing power converters and the development of new converters, counting for an increase in the efficiency of the electric energy transformations and a more traditional use of the electric energy [2-4].

By applying WBG semiconductor devices, the multi-physics interactions, including coupling of electrical, thermal and mechanical fields in the power electronics modules become more severe. Thus, power electronics packaging is more dependent on the rigorous use of the proven finite element methods based multi-physics simulations, as multi-physics simulation can effectively save design time and reduce design cycles [5-7].

In this paper, several multi-physics simulation cases were introduced, based on design of power electronics modules for different applications. Including fringing effect simulation to estimate the difference between theoretical capacitance and practical capacitance of a double-side metallized ultra-thin ceramic for power module substrate applications, stress distribution of a specific ultrathin ceramic with thick copper on each side as power substrates, electrical and thermal simulations for the design of power module with >10 kV and > 225 ^{o}C ambient capability. Besides, parasitics in a 50 kW three phase electric vehicle motor drive busbar was extracted by simulations.

II. POWER MODULE SUBSTRATE

With relatively high thermal conductivity, low coefficient of thermal expansion (CTE), excellent heat-resistance and chemical resistance, Al_2O_3, Si_3N_4 and AlN Direct-bonded-Copper (DBC) has been recognized as general substrates in power electronics packaging [8]. However, the firing temperature of these ceramic substrates are usually above 1700 ^{o}C, and fabrication processes are also complex [9]. Also, to get

good blocking voltage capability, the thickness of DBC substrate is usually relatively large, result in larger thermal mass and larger volume. To further improve the power density with smaller volume and weight, the ultra-thin Zirconia (ZrO_2) based ceramic substrate, 20 µm and 40 µm, was investigated by simulation, as an alternative approach for power module substrates.

A. Fringing Effect of Ultra-thin Zirconia Based Ceramic Substrate

For double-side metallized power module substrates, electrical field existed not just directly between the thick metal film layers on both sides of ceramic, but extended some distance away as fringing field. The simulation to calculate how much different the fringing field was induced in the parasitic capacitors in the substrate, was required, especially for high frequency applications.

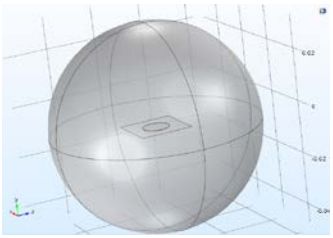

Fig. 1. Model for Fringing Effect Simulation, 40 µm ZBC substrate with 40 µm electrode on both sides, covered by the air sphere with 40mm radius.

The model for fringing effect simulation was established in COMSOL Multi-physics, as shown in Fig. 1. The ceramic with electrodes on both sides was located in the center of a sphere with properties of air, the sphere should be large enough to not impact simulation results. The thickness of ZBC substrate was 40 µm, the electrode thickness was defined as 40 µm. Electrical potential was applied on both electrodes, 1 V on one side, ground on the other. The simulation results were as shown in Fig. 2.

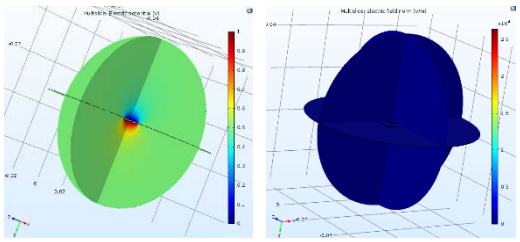

Fig. 2. Electrical Potential and electrical field distribution in 40 µm ZBC substrate with 40 µm electrode on both sides.

To further investigate the impact of ZBC on the fringing effects, thickness of ZBC substrate was re-defined as 4 mm, and the simulation results were as shown in Fig. 3.

In the simulation, the relative permittivity of ZBC substrate was define as 29, the theoretical capacitance for metallized 4mm ZBC substrate is 5.039 pF, while that for metallized 40µm ZBC substrate is 503.9 pF.

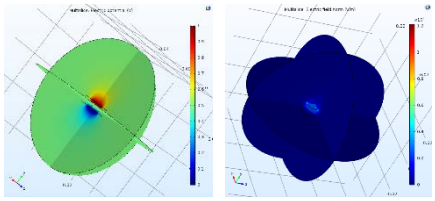

Fig. 3. Electrical Potential and electrical field distribution in 4 mm ZBC substrate with 40 µm electrode on both sides.

The capacitances of metallized ZBC substrates with different electrode thicknesses were calculated by COMSOL multi-physics based on the electrical field distribution in the models, as shown in Fig. 4.

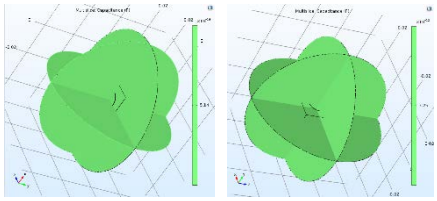

Fig. 4. Capacitance of Metallized ZBC substrate with different ceramic thickness calculated by simulations, 40µm (left), 4mm (right).

The capacitance of metallized 40 µm ZBC substrate was 514 pF, which means the fringing effect induced 2% difference from the theoretical value, while that of the metallized 4mm ZBC substrate was 7.25 2% pF, 43.88% difference from the theoretical value was induced. To further investigate the impact of electrode thickness on fringing effects, the electrode thickness was re-defined as 20 µm. The simulation results were shown in Fig. 5.

The simulated capacitance of metallized 40 µm ZBC substrate with 20µm electrodes was 503.9 pF, the difference induced by fringing effect was reduced to 1.8%. It was found from the simulation results that reduced dielectric thickness and electrode thickness can help to reduce the fringing effect on parasitic capacitance.

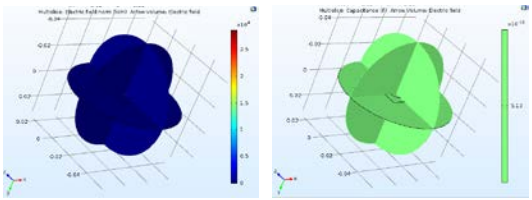

Fig. 5. Electric Field distribution and Calculated Capacitance of 40 µm ZBC substrate with 20 µm electrode.

B. Pre-stress Analysis of ZBC substrate with thick copper on both sides

Pre-stress analysis of ulra-thin (20 µm / 40 µm) ZBC substrate is important, since the potential of this materials for power module substrate applications has never been investigated before this work.

The ultra-thin ceramic can provide 2 kV ~ 3 kV breakdown voltage, the performance of this ceramic was compared with traditional DBC substrates with 10mil AlN / Al_2O_3 and 5 mil

copper on each side. In the FEM model as shown in Fig. 6, Sn63Pb37 was selected as interconnection between SiC devices and DBC substrates. 1/4 symmetric model was established to improve simulation efficiency.

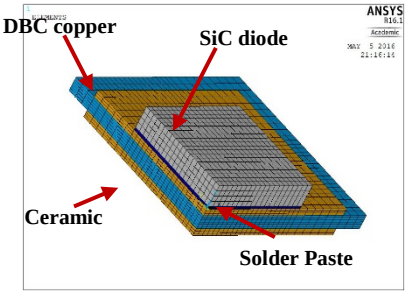

Fig. 6. 1/4 Symmetric FEM model for pre-stress analysis

The dimension of SiC die was 4 mm × 4 mm ×0.4 mm, the area of copper layers was 6 mm × 6 mm, and the area of ceramic layer was 7 mm × 7 mm. The thicknesses of ZBC substrates were 20 µm and 40 µm. The displacement and rotation of bottom layer center point were defined as zero, and symmetric boundary conditions were applied. Anand constitutive model was applied to describe the viscoplastic behavior of Sn63Pb37 solder layer [10].

The von mises stress distributions in different models were as shown in Fig. 7. It was found that the maximum von mises stresses in different models were located at the far end corner of the interface between ceramic layers and copper layers. The model with 20 µm ZBC substrate suffered maximum von mises pre-stress, 292 MPa, compared with those in the other 3 models, which were 141 MPa, 248 MPa, and 261 MPa respectively, by the sequence shown in Fig. 7.

Since the solder layer tended to fail first during power module operations, and the ZBC substrate was primarily investigated in this work. Shear stress distributions in solder layers and ceramic layers in different models were compared, as shown in Fig. 8 and Fig. 9.

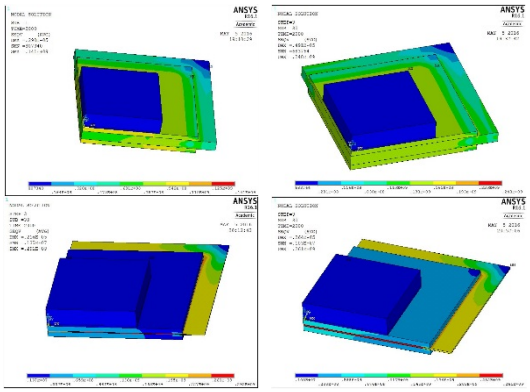

Fig. 7. Von Mises Stress distribution in models, (a) 10 mil AlN; (b) 10 mil Al_2O_3; (c) 20 µm ZBC substrate; (d) 40 µm ZBC substrate.

The shear stresses on the solder layers were concentrated at the far end corner of the SiC devices in different models, located in the middle of that area. Solder layer of the model with 20 µm ZBC substrate suffered maximum shear stress, 0.772 MPa, while those in other models were 0.3586 MPa, 0.2904 MPa, and 0.7612 MPa, respectively, by the sequence shown in Fig. 9. The shear stresses induced by the soldering process in solder layers were not so significant.

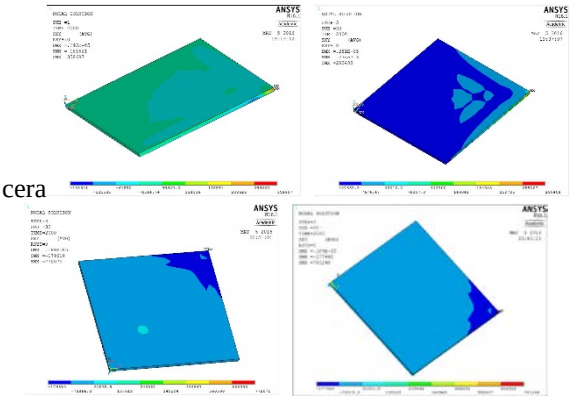

Fig. 8. Shear stress distributed on solder layers of different models, (a) 10 mil AlN; (b) 10 mil Al_2O_3; (c) 20 µm ZBC substrate; (d) 40 µm ZBC substrate.

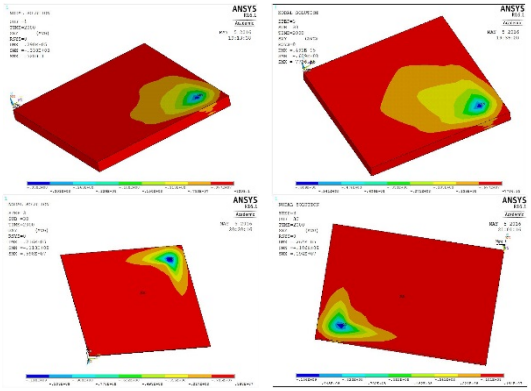

Fig. 9. Shear stress distributed on ceramic layers of different models, (a) 10 mil AlN; (b) 10 mil Al_2O_3; (c) 20 µm ZBC substrate; (d) 40 µm ZBC substrate.

The shear stresses on the solder layers were concentrated at the far end corner of the SiC devices in different models, located in the middle of that area. Solder layer of the model with 20 µm ZBC substrate suffered maximum shear stress, 0.772 MPa, while those in other models were 0.3586 MPa, 0.2904 MPa, and 0.7612 MPa, respectively, by the sequence shown in Fig. 9. The shear stresses induced by the soldering process in solder layers were not so significant.

According to the simulation results shown in Fig. 9, it was found that the maximum stresses in the ceramic layers of different models were 33.8 MPa, 60.9 MPa, 118 MPa and 194 MPa, respectively by the sequence shown in Fig. 9. The models with thin ZBC substrate suffered significantly higher shear stresses than those in models with traditional AlN and Al_2O_3 substrates. And the model with 40 µm ZBC substrate suffered maximum shear stress in the ceramic layer among all the models. The maximum shear stresses in different models were all located at the far end corner of the interface between ceramic layers and copper layers. The results also showed that the maximum shear stresses on ceramic layers were compression stresses.

III. High Voltage and High Temperature Power Module Development

High voltage and high temperature power modules were required by different applications, such as aircraft on-engine controls. Multi-physics played important role in high voltage and high temperature power module designs for electrical field distribution and junction temperature estimation [11].

A. Electrical field distribution in high voltage power modules

Layout design and components selection process was important to determine the high voltage capability of power modules, to verify the capability before the fabrication process is necessary. Fig. 10 showed a model for > 10 kV power module design with selected component models assembled together.

In the model, 0.1 inch minimum distance between different copper islands was defined, and terminals with round shape were selected to avoid severe high voltage concentrations. 12 mil bonding wire interconnected the anodes of SiC diodes to other pieces of copper islands on which high voltage terminals were attached. The cathodes of SiC diodes were attached by high temperature solder paste through reflowing process. The transparent part is high temperature silicone gel with high breakdown voltage capabilities.

In the simulation, 10 kV was applied to the anodes of SiC diodes and the cathodes were connected to the ground. The simulation results were as shown in Fig. 11.

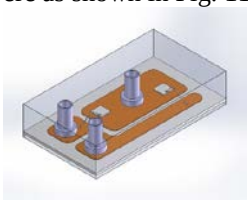

Fig. 10. Model of a high voltage SiC power module with > 10 kV capability

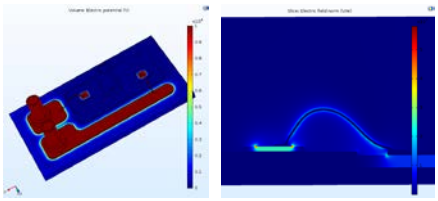

Fig. 11. Electric Potential and Electric Field Distribution in the high voltage power module

The simulation results showed that there was field stress concentration at the edges of device topside metallization layers, which were about 5×10^7 ~ 6×10^7 V/m, this value was higher than the dielectric strength of the silicone gel (3×10^7 V/m). This would not happen in practice, since different kinds of edge terminations and passivation will be applied at this location of power semiconductor devices to avoid high electrical field stress [12]. The layout design and components selections were verified by the electric simulations.

B. Junction Temperature in the High Temperature Power Module

According to the highest isolation temperature of the silicone gel we applied to the power modules, the highest temperature within the encapsulations should not exceed 225 ºC. And it was found that the highest power the SiC device can generate is about 1920 W/cm^2 for 224 ºC junction temperature, as shown in Fig. 12.

According to the performance of SiC devices in the power modules, the power density generated by each SiC device is 1.042×10^6 W / m^2.

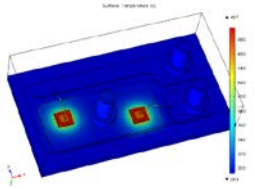

Fig. 12. Temperature Distribution in power modules with maximum power generated.

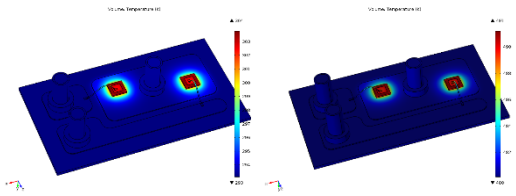

Fig. 13. Junction Temperature of Power Module under different ambient temperature: (a) 20 ºC; (b) 207 ºC.

From the simulation results, as shown in Fig. 13, it was found that the Junction Temperature of the power module was 31 ºC at room temperature. When the ambient temperature increased to 207 ºC, the junction temperature was 218 ºC. The junction to ambient thermal impedance of the power module can be derived as:

$$T_j = T_A + (R_{\theta jA} \times \text{Power}) \quad (1)$$

From the equation, the junction to ambient thermal impedance can be calculated,

$$R_{\theta jA} = 0.4398\ ^{o}\text{C / W}$$

According to the criteria that the maximum temperature in the packaging should be lower than 225 ºC, the maximum ambient temperature which the power module can operate at was 214 ºC.

IV. Parasitics Extraction of EV Motor Drive Busbar

Study of the parasitic parameters of DC busbar is especially important with fast switching wide-bandgap power semiconductor devices. Electrical-magmatic FEA simulation can be utilized to extract parasitics for any physical power electronic design. As shown in Fig. 14 was the basic schematic of 3 phase inverter with DC-link capacitors.

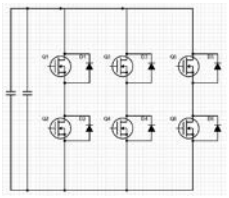

Fig. 14. Schematic of a 3 phase inverter.

A 4-layer PCB board with 4 oz copper on each layer was designed as the busbar for SiC based 50kw three phase VSI topology. Due to the geometry symmetry, only partial of the board is simulated for the power loop inductance as in Fig. 15.

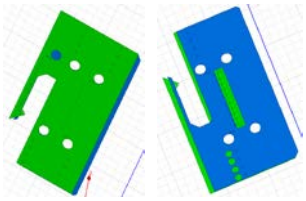

Fig. 15. Part of the busbar for one single phase circuits of the three phase motor drive.

On the busbar, both ceramic and film capacitors are used. The ceramic capacitors are located very close power modules for absorbing high frequency transient current while film capacitors are located relatively further from the power module to absorb high magnitude and low frequency transient current. Fig. 16. shows current density distribution in a phase leg at 100 A.

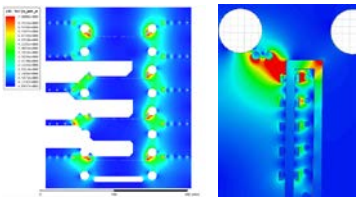

Fig. 16. Current distributions around film capacitors (left) and ceramic capacitors (right) on the busbar at low frequencies.

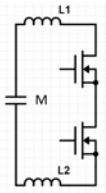

Fig. 17. Schematic of parasitics in one phase loop of the 3 phase motor drive.

The lumped parameter parasitics are defined as in Fig. 17. Self-inductance L_1 , L_2 and mutual inductance M are simulated. Total loop inductance is calculated according to (2).

$$L = L_1 + L_2 - 2M \quad (2)$$

The phase leg loop parasitic inductances for ceramic and film capacitor are 4 nH and 9 nH respectively. The simulations results were applied to optimize the busbar design.

V. CONCLUSIONS

Multi-physics simulation has become a powerful tool to investigate interactions between electrical, thermal, and mechanical aspects in power electronics packaging. As a time-efficient modeling approach, multi-physics simulation is reliable in different processes, including power module design verification, fabrication process parameters optimization, and reliability assessment. The cases introduced in this paper has proved the capability of multi-physics simulation and its essentiality in various areas of power electronics, especially for power electronics packaging.

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