

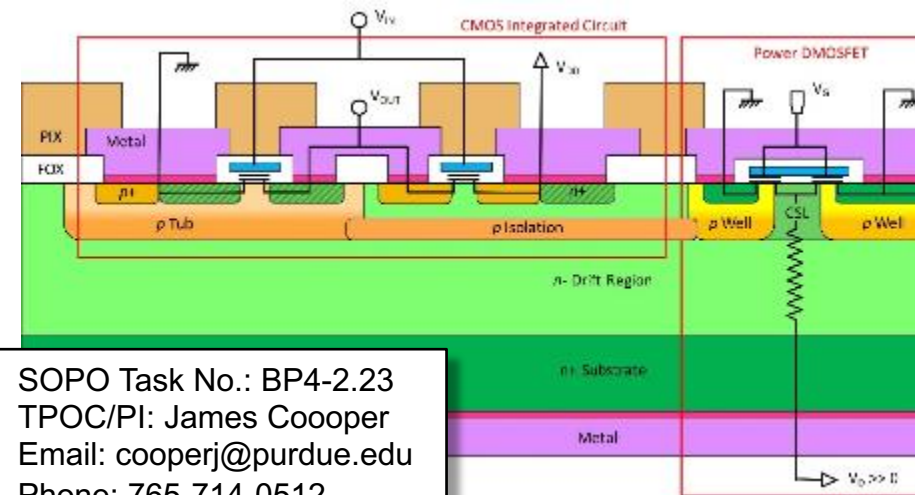


Project Title: SiC Planar DMOSFETs and Power IC's with Enhanced Short-Circuit Withstand Time

Objectives: Demonstrate CMOS power ICs on a 3.3 kV vertical SiC DMOSFET with 4x longer SCWT

Major Milestones: Q2: begin mask design, Q3: finalize design & process flow, Q4: begin fabrication

Deliverables: Mask layout & process flow (Q3)



WBG Technology Impact

1. SiC CMOS ICs on power DMOSFET die for on-chip sensing and protection circuitry
2. More robust devices under shorted-load events
3. Application sector: EV and HEV, renewable energy, motor drives, server power supplies
4. Timeframe for commercialization: Two years for longer SCWT, five years for CMOS ICs on-chip
5. SCWT of existing technology is 3 – 5 μ s. This project can increase SCWT to 10 – 20 μ s *without impacting on-state performance.*

More WBG Impact and Additional impacts

1. More robust SiC power MOSFETs & IGBTs
2. Increased flexibility in device control, allowing self protection and adaptive operation
3. More flexible and robust technology will increase confidence in SiC technology, increasing their acceptance by system designers
4. Technology maturity: The SCWT improvement only requires reducing the oxide thickness, and can be immediately applied to any production process, including both planar and trench MOSFETs.