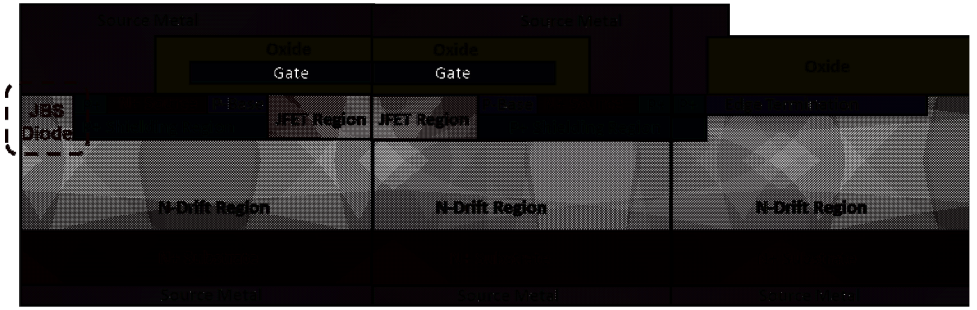
Company: Sicamore Semi/NCSU Membership Level:

Project Title: 3.3 kV SiC Planar-Gate Power JBSFETs
Objectives: Create a NCSU Gen 5 PRESiCE™ chip design and process technology in partnership with SiCamore Semi for manufacturing 3.3 kV rated SiC planar-gate power JBSFETs.
Major Milestones: Fabrication of 2 process lots
Deliverables: Statistical Data & Wafer-maps for 3.3 kV JBSFETs; and JBSFET Die to Device Bank



Task No. BP5-2.31 (OIF)
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WBG Technology Impact

1. Open domain manufacturing process for 3.3 kV SiC JBSFETs.
2. Market segments impacted: Industrial Motor Drives, Traction Drives etc.
3. Timeframe for commercialization: BP-5
4. The outcome of this project will serve as the baseline process for PA members to design their own products by licensing the Gen-5 PreSiCE™ process.
5. SiCamore will be a second source foundry option for manufacturing SiC power devices in the United States.

Accomplishments/Outcomes

1. Increase market penetration for SiC Power devices.
2. Workforce Development: 1 graduate student is involved.
3. TRL level

   At project start: TRL7

   Expected at project completion: TRL 8