GAN POWER TRANSISTORS:
DEVICES, TECHNOLOGY AND RELIABILITY

Matteo Meneghini, Carlo De Santi, Gaudenzio Meneghesso, Enrico Zanoni

University of Padova, Department of Information Engineering,
via Gradenigo 6/B, Padova, 35131, Italy
matteo.meneghini@unipd.it
Knowing GaN
- Wide bandgap semiconductors: why?
- GaN vs other semiconductors (FOMs)
- How to get high sheet charge and high mobility?

Knowing GaN devices
- AlGaN/GaN HEMTs: structure and properties
- How to get normally-off operation?
- Vertical GaN devices
- Driving E-mode GaN devices

Applications of GaN transistors

Degradation and reliability issues
- Dynamic-Ron (problem solved!)
- Gate stability
- Hot electrons and hard switching
- Degradation in off-state, avalanche

Vertical devices: perspectives
- Avalanche capability (!)
- (No) current collapse, $V_{TH}$ stability
- Advanced 3D structures
- Performance of vertical GaN

GaN integrated circuits

Conclusions
Wide bandgap semiconductors – Why?

Breakdown field has a power-law dependence on energy gap: \( E_{\text{crit}} \propto E_G^{2.3} \)

Wide bandgap semiconductors \( \Rightarrow \) electron devices with high breakdown voltage and small thickness (efficient power conversion)

Among the commercially-available materials, GaN has the highest breakdown field of 3.3 MV/cm

See also: Hudgins, TPEL 18, 907 (2003)
### GaN vs Other Semiconductors

<table>
<thead>
<tr>
<th>Material</th>
<th>Si</th>
<th>GaAs</th>
<th>4H-SiC</th>
<th>GaN</th>
<th>β-Ga$_2$O$_3$</th>
<th>Diamond</th>
<th>AlN</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_G$(eV)</td>
<td>1.12</td>
<td>1.42</td>
<td>3.23</td>
<td>3.4</td>
<td>4.9</td>
<td>5.5</td>
<td>6.2</td>
</tr>
<tr>
<td>$\varepsilon_r$</td>
<td>11.7</td>
<td>12.9</td>
<td>9.66</td>
<td>8.9</td>
<td>10</td>
<td>5.7</td>
<td>8.5</td>
</tr>
<tr>
<td>$\mu$ (cm$^2$/Vs)</td>
<td>1440</td>
<td>9400</td>
<td>950</td>
<td>1400</td>
<td>250</td>
<td>4500</td>
<td>450</td>
</tr>
<tr>
<td>$E_{\text{crit}}$ (MV/cm)</td>
<td>0.3</td>
<td>0.4</td>
<td>2.5</td>
<td>3.3</td>
<td>8*</td>
<td>10*</td>
<td>15*</td>
</tr>
<tr>
<td>$v_s$ ($\times 10^7$ cm/s)</td>
<td>1</td>
<td>0.9</td>
<td>2</td>
<td>2.4</td>
<td>1.1</td>
<td>2.3</td>
<td>1.4</td>
</tr>
<tr>
<td>$k_{\text{th}}$ (W/cmK)</td>
<td>1.3</td>
<td>0.55</td>
<td>3.7</td>
<td>2.5</td>
<td>0.1-0.3</td>
<td>23</td>
<td>2.85</td>
</tr>
</tbody>
</table>

Excluding the three semiconductors for which commercial devices are not available, GaN is the semiconductor with

- the largest energy gap
- the largest critical field
- the highest saturation velocity

→ ideal candidate for power semiconductor devices (high temperature/high voltage)

Values from [https://doi.org/10.1007/978-3-030-20208-8_2](https://doi.org/10.1007/978-3-030-20208-8_2)
**JFOM = (maximum voltage) x (maximum transit frequency), for a given value of the drain-source spacing**

\[
\text{Johnson FOM} = f_T V_{DS,max} = \frac{E_{\text{crit}} v_s}{2\pi}
\]

The JFOM of GaN is
- **slightly higher** than that of SiC (0.556)
- **comparable** to β-Ga\(_2\)O\(_3\) (0.978)
- **much larger** than that of silicon (0.0379) and GaAs (0.0455)

AlN and diamond are better than GaN, but their JFOMs are between 2.5 and 3 (same order of magnitude of GaN)
Baliga FOM → compares semiconductors for application in power electronics

Material parameters that help minimizing the *conduction losses* in power transistors

BFOM of GaN is **substantially larger than those of silicon and GaAs**, higher than SiC, similar to Ga$_2$O$_3$.

Diamond and AlN (UWBG semiconductors) have a much higher Baliga FOM (to further push the limits).
WIDE BANDGAP MATERIALS: THE PROBLEM OF DEEP DOPANTS

<table>
<thead>
<tr>
<th>Material</th>
<th>n-dopant</th>
<th>$\Delta E_d$ (eV)</th>
<th>p-dopant</th>
<th>$\Delta E_a$ (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>P</td>
<td>0.045</td>
<td>B</td>
<td>0.045</td>
</tr>
<tr>
<td>GaAs</td>
<td>Si</td>
<td>0.006</td>
<td>Be</td>
<td>0.028</td>
</tr>
<tr>
<td>GaN</td>
<td>Si</td>
<td>0.015</td>
<td>Mg</td>
<td>0.16</td>
</tr>
<tr>
<td>4H-SiC</td>
<td>N</td>
<td>0.085</td>
<td>Al</td>
<td>0.2</td>
</tr>
<tr>
<td>AlN</td>
<td>Si</td>
<td>0.16</td>
<td>Mg</td>
<td>0.5</td>
</tr>
<tr>
<td>Diamond</td>
<td>P</td>
<td>0.6</td>
<td>B</td>
<td>0.37</td>
</tr>
<tr>
<td>$\beta$-Ga$_2$O$_3$</td>
<td>Si</td>
<td>0.046</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

**Issue 1:** shallow donors, no shallow acceptors

**Issue 2:** impurity scattering at high doping

Note: *none of the wide band gap semiconductors listed above has a shallow acceptors; they all have a shallow donor except for AlN and diamond; in addition, high doping levels lead to scattering (unwanted!)*

Thus engineering of free carriers by doping may be an issue for some wide band gap (WBG) semiconductors.

So WBG materials have great figures of merit, but may lack of free carriers

→ How to solve this issue?

The High Electron Mobility Transistor (HEMT)

Values and content from [https://doi.org/10.1007/978-3-030-20208-8_2](https://doi.org/10.1007/978-3-030-20208-8_2)

GaN power transistors: devices, technology and reliability – matteo.meneghini@unipd.it
The concept of heterostructure transistor is known since many years

**Idea:**

- **Use a heterostructure** to create a 2-dimensional electron gas (2DEG)
- **Separate the doped region** from the 2DEG, to reach high mobility

Still, the AlGaAs/GaAs transistor is doped

To avoid doping → **Use polar semiconductors** (polarization doping, instead of impurity doping)
GaN: Spontaneous Polarization

Nitrogen has a higher electronegativity, compared to gallium.

As a consequence, Ga and N atoms have anionic (+) and cationic (-) characteristics → spontaneous polarization $P_{sp}$ along the (0001) axis

On top of this → Piezoelectric polarization!

Nitrogen has a higher electronegativity, compared to gallium.

As a consequence, Ga and N atoms have anionic (+) and cationic (-) characteristics → spontaneous polarization $P_{sp}$ along the (0001) axis

On top of this → Piezoelectric polarization!

<table>
<thead>
<tr>
<th>Material</th>
<th>GaN (C m⁻²)</th>
<th>InN (C m⁻²)</th>
<th>AlN (C m⁻²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{sp}$</td>
<td>-0.029</td>
<td>-0.032</td>
<td>-0.081</td>
</tr>
<tr>
<td>$P_{sp}$</td>
<td>-0.034</td>
<td>-0.042</td>
<td>-0.090</td>
</tr>
</tbody>
</table>


GaN power transistors: devices, technology and reliability – matteo.meneghini@unipd.it
Both the **GaN** and the **AlGaN layers** are typically left **undoped**, to minimize electron scattering at impurities.

Undoped GaN has a **weak n-type conductivity**, with electron densities that depend on the quality of the epitaxy (always higher than $10^{15}$ cm$^{-3}$)

When a potential $V_G$ is applied to the gate, the charge in the 2DEG can be modulated:

$$n_S(V_G) = \frac{[Q_\pi(AlGaN) - Q_\pi(GaN)]t + \epsilon \left[V_G - \left(\phi_b - \frac{\Delta E_C}{q}\right)\right]}{q(t + d)}$$

$$E_{AlGaN} = \frac{qN_{DD}^{-} - Q_n(AlGaN)}{\epsilon_{AlGaN}}$$
The off-state voltage is **supported by the gate-drain access region**

The on-resistance then depends on the breakdown voltage:

\[
R_{on} = R_{\text{channel}} + R_{\text{drain}} = \frac{1}{W_G q \mu n_s L_G} \left( L_G + \frac{BV}{E_{\text{crit}}} \right)
\]

Decreasing the gate length from 1 µm to 0.25 µm can lead to a substantial reduction in the resistive losses

For high breakdown voltage devices, the resistive contribution of the gate-drain access region becomes relevant

See also: *Ueda, Properties and Advantages of Gallium Nitride (in Power GaN Devices)*

GaN power transistors: devices, technology and reliability  – matteo.meneghini@unipd.it
Silicon-based power transistors have an **intrinsic body diode** → large reverse recovery charge $Q_{rr}$

**Lateral GaN devices** are based on the HEMT concept, and **do not have any body diode**. HEMTs are majority carrier devices, and the lack of minority carriers leads to a near-zero $Q_{rr}$ ($R_{DS,ON} \times Q_{rr}$ down to 2.2 mΩnC)

Table: [https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7862945](https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7862945)
Image: [https://encrypted-tbn0.gstatic.com/images?q=tbn:ANd9GcSKCh_LeCZ9mGIlbUlqrrZ3Ei4d8Cj7acEVlrw&usqp=CAU](https://encrypted-tbn0.gstatic.com/images?q=tbn:ANd9GcSKCh_LeCZ9mGIlbUlqrrZ3Ei4d8Cj7acEVlrw&usqp=CAU)

---

**Table: Comparison of Key FOMs for Si, GaN, and SiC Devices (All Numbers Typical Values Extracted From Data Sheets at 25 °C [44, 45, 47–49])**

<table>
<thead>
<tr>
<th>Device</th>
<th>Rating [V]</th>
<th>$R_{DS,ON}$ [mΩ]</th>
<th>$R_{DS,ON} \cdot Q_{oss}$ [mΩ·μC]</th>
<th>$R_{DS,ON} \cdot Q_{rr}$ [mΩ·μC]</th>
<th>$R_{DS,ON} \cdot E_{oss}$ [mΩ·μJ]</th>
<th>$R_{DS,ON} \cdot Q_{G}$ [mΩ·nC]</th>
<th>$V_{f} @15 A$ [V]</th>
<th>$V_{GS_{max}}$ [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si SJ [47]</td>
<td>600</td>
<td>56</td>
<td>23.5</td>
<td>336.0</td>
<td>450</td>
<td>3800</td>
<td>0.9</td>
<td>20</td>
</tr>
<tr>
<td>GaN E-mode GIT [48]</td>
<td>600</td>
<td>55</td>
<td>2.2</td>
<td>2.2</td>
<td>350</td>
<td>300</td>
<td>2.7</td>
<td>N.A. 4)</td>
</tr>
<tr>
<td>GaN E-mode [20]</td>
<td>650</td>
<td>50</td>
<td>2.8</td>
<td>2.8</td>
<td>350</td>
<td>290</td>
<td>3.2</td>
<td>7</td>
</tr>
<tr>
<td>GaN Cascode [44]</td>
<td>650</td>
<td>52</td>
<td>5</td>
<td>7.0</td>
<td>730</td>
<td>1460</td>
<td>1.4</td>
<td>18</td>
</tr>
<tr>
<td>SiC DMOS [45]</td>
<td>900</td>
<td>65</td>
<td>4.5</td>
<td>8.5</td>
<td>570</td>
<td>1950</td>
<td>2.7</td>
<td>18</td>
</tr>
<tr>
<td>SiC TMOS [49]</td>
<td>650</td>
<td>60</td>
<td>3.8 2)</td>
<td>3.3 3)</td>
<td>540</td>
<td>3480</td>
<td>3.3</td>
<td>22</td>
</tr>
</tbody>
</table>
C\textsubscript{GD} originates from a small corner of the gate (extremely low, fast switching capability, great dV/dt immunity)

C\textsubscript{GS} originates from the gate-to-channel and gate-dielectric-field plate capacitances (still very small compared with silicon MOSFETs)
\( V_{\text{TH}} \) depends on several parameters related to the gate metal and the heterojunction properties:

\[
V_{th}(x) = \phi_B(x) + E_F(x) - \Delta E_C(x) - \frac{\sigma(x)}{\varepsilon_0 \varepsilon_{AlGaN}(x)} d_{AlGaN} - \frac{q N_D}{2 \varepsilon_0 \varepsilon_{AlGaN}(x)} (d_{AlGaN})^2
\]

Several knobs to turn to tune the \( V_{\text{TH}} \):

- Schottky barrier height
- Thickness of AlGaN barrier layer
- Aluminum content in the AlGaN barrier
- Different topologies for normally-off
  - Insulated-gate
  - p-type gate
  - cascode configuration

Images: https://q3p9g6n2.rocketcdn.me/wp-content/ml-loads/2013/08/knobs.jpg

GaN power transistors: devices, technology and reliability – matteo.meneghini@unipd.it
Each approach has advantages and drawbacks, in terms of reliability, as will be discussed later.
The use of a p-GaN gate lifts the conduction band diagram at the AlGaN/GaN interface, resulting in normally-off operation.

Figure: [http://dx.doi.org/10.1016/j.mssp.2017.09.027](http://dx.doi.org/10.1016/j.mssp.2017.09.027)
Simulated conduction band diagrams of a p-GaN/AlGaN/GaN heterostructure, for two different values of Al molar fraction (a), or two different values of the AlGaN thickness (b).

For normally-off, **thin barriers with moderate Al content** are needed (see (c)).

Figure: [http://dx.doi.org/10.1016/j.mssp.2017.09.027](http://dx.doi.org/10.1016/j.mssp.2017.09.027)
• $R_G$ controls switching speed
• Separate $R_G$ for turn-on and turn-off

**Turn-on resistor**
• Controls turn-on slew rate
• Too small $\Rightarrow$ high $dV/dt$, drain current ringing

**Turn-off resistor**
• $R_{GOFF}$ smaller than $R_{GON}$ to obtain strong pull down
• Too small $R_{GOFF}$ may create $V_{GS}$ undershoot and ringing

**Turn-on:** when parasitic diode ($D_P$) reaches the $V_{GS,SS}$, steady electric current flows through $D_P$ ($V_{GS}$ is clamped); the voltage drop across this gate resistor $R_{G2}$ can be selected to produce a relatively stable mA-scale current.

**Turn-off:** negative bias is applied to the gate thanks to the $R_{G3}/C_{SU}$ network.

---

Source:
- [https://doi.org/10.1002/9781119594406.ch3](https://doi.org/10.1002/9781119594406.ch3)
- [https://www.infineon.com/dgdl/Infineon-ApplicationNote_CoolGaN_600V_emode_HEMTs_Driving_CoolGaN_high-electron_mobility_transistors_with_EiceDRIVER_1EDI_Compact-ApplicationNotes-v02_00-EN.pdf?fileId=5546d46262b31d2e016368e4d7a90709](https://www.infineon.com/dgdl/Infineon-ApplicationNote_CoolGaN_600V_emode_HEMTs_Driving_CoolGaN_high-electron_mobility_transistors_with_EiceDRIVER_1EDI_Compact-ApplicationNotes-v02_00-EN.pdf?fileId=5546d46262b31d2e016368e4d7a90709)
GaN power devices are typically grown on a silicon substrate (6”-8”). The large lattice mismatch results in high threading dislocation densities.

- Cross section TEM image of AlGaN/GaN HEMT structure showing the high dislocation density.
Two main device architectures:

- **Lateral**: high speed, highest mobility, already on the market on silicon substrate
- **Vertical**: high breakdown voltage, high current capability, several concepts proposed

GaN power transistors: devices, technology and reliability  – matteo.meneghini@unipd.it
GaN power transistors: devices, technology and reliability  – matteo.meneghini@unipd.it

Vertical GaN devices enable higher current/power levels, with high blocking voltages, compared to the lateral counterparts.

Vertical GaN Transistors

1-30KW

30KW-100KW

100KW-20MW

Grid Level power conversion

Rail Electrification

Hybrid Electric Vehicles

Total Electric Vehicles

- Industrial power supplies
- Motor Drives
- Solar Inverters, Charger
- Auxiliary electronics for automotive

Solar Inverters

Motor Drives

Hybrid cars

Smart Grid

High speed trains

10KW

100KW

10MW

Appropriately stacking

Source: S. Chowduri, IWN 2014


All GaN vehicle!
High powers (10 kW-1 MW) require vertical structure

*Blocking voltage $\propto L_{GD}$*

Vertical geometry is preferred over lateral geometry to enable:

- Higher Blocking voltage
- Higher current density
- Smaller chip size and potentially lower cost

Research on vertical power GaN processes and devices pushing performance beyond current state-of-the-art (also on on silicon substrate!)

GaN is currently being explored for voltages above 1 kV (commercial up to 900 V)
Consumer electronics will be one of the largest markets for power GaN devices.
APPLICATIONS OF GaN TRANSISTORS

Entering a new era
(Source: Compound Semiconductor Quarterly Market Monitor, Yole Développement, March 2020)

2018
Consumer Market dominates
$9M

2025
Automotive market introduction
Consumer co-exist
> $700M

2030
Industrial market take-off
Consumer and Automotive co-exist

Expansion in many markets:
Consumer, Automotive and Industrial

Power supply for UPS, Datacenters,....

**Applications of GaN Transistors: Telecom**

**Mobile basestation:**
- Higher efficiency
- Reduced cost of ownership
- High reliability

**Thanks to GaN:**
- **reduction in power loss** and heat dissipation
- **reduces the energy wastage by 50%**, but also the environmental footprint and operating expense (OPEX)

---

**3000 kW/48V**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Single base station South Italy</th>
<th>Central office in UK</th>
</tr>
</thead>
<tbody>
<tr>
<td>System load (avg.)</td>
<td>6 kW</td>
<td>250 kW</td>
</tr>
<tr>
<td>Energy cost (kWh)</td>
<td>0.17 €</td>
<td>0.13 €</td>
</tr>
<tr>
<td>Annual consumption*</td>
<td>57.130 kWh</td>
<td>2,380,434 kWh</td>
</tr>
<tr>
<td>Annual Energy cost reduction*</td>
<td>576 €</td>
<td>18,352 €</td>
</tr>
<tr>
<td>Annual CO2 emission reduction**</td>
<td>2.2 tons</td>
<td>97.3 tons</td>
</tr>
</tbody>
</table>

---

https://www.eltek.com/insights/she-is-so-cool/
Source: https://link.springer.com/article/10.1007/s11664-020-08397-z

**GaN power transistors: devices, technology and reliability** – mattheo.meneghini@unipd.it
APPLICATIONS OF GaN TRANSISTORS: BATTERY CHARGERS

100 kHz Dual Active Bridge for 3.3kW Bi-directional Battery Charger

**Note:** devices are operated in hard switching when a DAB works at either low power or a strong voltage transfer ratio

**Benefits of GaN:**

- High switching frequency
- Low loss during hard switching

**These benefits derive from:**

- Low output charge
- Low reverse recovery charge
- Low switching losses

Applications of GaN Transistors: PV Inverter

- 3 kW Solar inverter
- Storage capacity of 3 kWh
- Based on cascaded transistors (close replacement to silicon)

GaN enables:
- high-temperature operation without internal cooling fan
- 40 % increase in power density
- Wider range of operating gate voltages (±20 V)
- 33 % higher power output
- 50 % decrease in product weight

Source: https://link.springer.com/article/10.1007/s11664-020-08397-z
Applications of GaN Transistors: USB Type-C Chargers

- Integration of GaN enabled power density of 11 W/in³
- 450 V power IC, optimized for high frequency, soft-switching topologies
- Monolithically-integrated GaN HEMT and gate drive circuitry in low profile QFM package
- 2 MHz switching frequency
- Rated for 8 A (T_c=100 °C), 170 mΩ

Specification

<table>
<thead>
<tr>
<th>Specification</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output power</td>
<td>45 W</td>
</tr>
<tr>
<td>Input voltage</td>
<td>100 V–240 V AC @ 50/60 Hz</td>
</tr>
<tr>
<td>Input current</td>
<td>1.25 A</td>
</tr>
<tr>
<td>Output voltage and current</td>
<td>(USB-C PD 3.0) V/3A, 9 V/3A, 12 V/3A, 15 V/3A, 20 V/2.25A</td>
</tr>
<tr>
<td>Dimension</td>
<td>3.1 x 2.2 x 0.6 in</td>
</tr>
<tr>
<td>Weight</td>
<td>2.72 oz</td>
</tr>
</tbody>
</table>

Source: https://link.springer.com/article/10.1007/s11664-020-08397-z
Applications of GaN Transistors: Lidars

- Capacitor $C_1$ is discharged resonantly through the (stray) inductance $L_1$ and laser $D_L$
- $C_1$ is charged at moderate voltage (20-150 V), to achieve fast current rise-time and overcome inductance $L_1$

For very high power, using a low inductance surface mount laser, recent GaN transistors can achieve 26 A, 1.8 ns pulses (8 ns, 155 A pulses)

Source: https://epc-co.com/epc/Portals/0/epc/documents/application-notes/How2AppNote002%20LiDAR.pdf
APPLICATIONS OF GaN TRANSISTORS: WIRELESS POWER TRANSFER

Class D: reduction of power losses between silicon and GaN is 30%
Class E: much better waveforms, low $C_{oss}$

https://www.infineon.com/dgdl/Infineon-Gallium_nitride_benefits_of_GaN_e-mode_HEMTs_BISinfotech-Article-v01_00_EN.pdf?fileId=55d64d62d6b26b7016b06d406aa1f31
https://epc-co.com/epc/Portals/0/epc/documents/application-notes/AN021%20FETs%20for%20Low%20Cost%20WiPo.pdf

GaN power transistors: devices, technology and reliability – matteo.meneghini@unipd.it
Applications of GaN Transistors: Class-D Audio

Why GaN in Class-D amplifiers?

- THD, damping factor and intermodulation distortion depend on transistor properties
- GaN FETs have low propagation delays, fast slew rates, zero $Q_{rr}$
- Higher efficiency from low conduction and switching losses
- the dead-time – typically 25 ns for silicon power MOSFETs – can be reduced by 80%, to 5 ns or less

---

https://upload.wikimedia.org/wikipedia/commons/thumb/4/4c/Pwm_amp.svg/400px-Pwm_amp.svg.png
https://www.eeweb.com/wp-content/uploads/articles-articles-fig-3-1392656037.png
https://www.infineon.com/dgdl/Infineon-Audio_solutions_MERUS_class_D_audio_solutions_EN-ApplicationBrochure-v03_00-EN.pdf?fileId=5546d462677d0f460167bba4f4e81abd

GaN power transistors: devices, technology and reliability  – matteo.meneghini@unipd.it
1. Off-state, high lateral and vertical field (dielectric failure, GaN TBD)

2. Hard-switching, hot electrons and self-heating

3. ON-state, positive gate, p-GaN or gate dielectric degradation

Meneghini et al., Energies 2017, 10, 153
Dynamic On-resistance (Ron) → recoverable increase in on-resistance induced by trapping

When a HEMT is switched on after a trapping phase → current shows an exponential transient before reaching steady-state value (de-trapping transient)

The same happens if $I_D-V_D$ curves are measured from several QBPs
Trapping in off-state may induce a non-monotonic variation of on-resistance

Meneghini et al., [http://dx.doi.org/10.1016/j.mssp.2017.10.009](http://dx.doi.org/10.1016/j.mssp.2017.10.009)
**HOW TO EXPLAIN THE NON-MONOTONIC BEHAVIOR?**

1) In off-state, at $V_{DS} < 200$ V, $C_N$ (carbon at nitrogen site) acceptors in the buffer are ionized, and this induces a significant increase in dynamic-$R_{DSon}$.

2) For higher $V_{DS}$, electrons in the buffer can transfer to the 2DEG through BTB or trap-assisted leakage → positive charges are formed at the interface with the strain relief layer → decrease in dynamic-$R_{on}$.

3) For higher $V_{DS}$, vertical (drain to substrate) leakage becomes relevant.

**Note:** field-assisted detrapping may also lower dynamic-$Ron$.

Meneghini et al., [http://dx.doi.org/10.1016/j.mssp.2017.10.009](http://dx.doi.org/10.1016/j.mssp.2017.10.009), [https://doi.org/10.1016/S0040-6090(99)00344-2](https://doi.org/10.1016/S0040-6090(99)00344-2)

GaN power transistors: devices, technology and reliability – matteo.meneghini@unipd.it
HOW TO EXPLAIN THE NON-MONOTONIC BEHAVIOR?

- Dynamic-Ron is a balance between trapping/detrapping process
- At low voltages, negative charge build up is promoted by the ionization of buffer acceptors
- At high bias, E-field assisted (or leakage-assisted) negative charge detrapping (or positive charge storage) is promoted

![Graph showing the relationship between V_DS and R_DSon with temperature variations.](image)
Almost complete suppression of dynamic ON-resistance in AlGaN/GaN high-electron-mobility transistors is obtained by proton irradiation (Stockman, IEEE-TED 66, 372 (2019))
• 3 different mechanisms for threshold voltage instability were identified:

- **Mechanism 1**: electron injection from 2DEG into the AlGaN barrier [Tajalli et al., ESREF 2018]

- **Mechanism 2**: accumulation of holes at the p-GaN/AlGaN interface and subsequent hole trapping in the AlGaN barrier [Stockman et al., ISPSD 2019]

- **Mechanism 3**: depletion of holes within the p-GaN layer [Sayadi et al., IEEE TED 65, 2454 (2018)]
Positive and negative $V_{\text{TH}}$ shifts are observed, depending on the voltage range analyzed.

Threshold voltage instability can be suppressed through optimized passivation of the p-GaN sidewall.
Reference samples show zero dynamic-Ron up to $V_{DS} = 600$ V in soft-switching.

Does dynamic-Ron become an issue in hard switching?
How to characterize this effect?

Dynamic-Ron is no longer a problem, if buffer/structure are optimized.
SWITCHING RELIABILITY IS THE TOPIC OF RECENT JEDEC PUBLICATIONS

Guideline for Switching Reliability Evaluation Procedures for Gallium Nitride Power Conversion Devices

Version 1.0

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

JEP180.01
(EDITORIAL REVISION OF JEP180, FEBRUARY 2020)

JANUARY 2021

The switching locus curve and its usage

5.1 The switching locus curve

The switching locus is the trajectory of the \( i_D - V_{DS} \) waveform during a switching cycle. It is plotted by capturing both \( i_D \) and \( V_{DS} \) waveforms during a switching period, and plotting \( i_D \) vs. \( V_{DS} \) at each sampling instant [4]-[7]. There are three common types of switching experienced during switching transitions, as shown in Figure 2: hard, soft and resistive.

![Diagram](image)

(a) hard-switched turn-on and turn-off, e.g., high-side DUT in a buck converter with inductive storage element,

(b) soft-switched ZVS-turn-on and turn-off transitions e.g., low-side DUT in a buck converter with inductive storage element,

(c) switching in a resonant topology with soft-switched (ZVS) turn-on and hard-switched turn-off transitions,

(d) resistive-load switching. The addition of a capacitor in parallel with the resistor will change the shape of the locus.
Previous publications on the topic

Inductive-load switching (6.6 kHz, 480 V, 10 A)

K. Tanaka et al., IEEE-IRPS 2017

Works on packaged parts (e.g. 10 A switching current)

Non-realistic waveforms, pulse overlap is changed to induce hard switching

J. Joh et al., IEEE-IRPS (2014)
I. Rossetto et al., IEEE-TED 64, 3734 (2017)
F. Yang et al., IEEE-TED 67, 869 (2020)
OUR APPROACH: ON-WAFER TESTING

On-wafer boost converter

Capacitor-based circuit

Clamp circuit to get fast scope reading

\( R_{ON} \) reading after turn-on transient (<1 \( \mu s \))

GaN power transistors: devices, technology and reliability  – matteo.meneghini@unipd.it

Barbato et al., IET Power Electronics (2020)

Meneghini, IEDM 2018

Barbato et al., IET Power Electronics (2020)
HOW TO TEST DEVICES IN HARD SWITCHING? – A NOVEL ON-WAFER SETUP

The drain node capacitance (CSW) is discharged on the device, thus having a condition in which $V_{DS}$ and $I_{DS}$ are simultaneously high.

The circuit is based on RF tips, to reach high speeds even at wafer level (here $dV/dt$~10V/ns)

Detail of the output waveforms during the turn-ON transient. The commutation speed is close to the real applications.

**Note:** $C_{SW} = C_{oss} + C_{par} + C_L \gg C_{oss}$, to enhance degradation process ($C_{oss} = C_{DS} + C_{GD}$)

---

https://doi.org/10.1016/j.microrel.2020.113830
The three plots give a full description of the turn-on transients; the device turns on in the saturation region, and then reaches the linear region when $C_{SW}$ is discharged.

https://doi.org/10.1016/j.microrel.2020.113830
Hard-switching transitions lead to a stronger increase in dynamic $R_{on}$

All these effects are fully recoverable → current collapse comes from a charge-trapping effect and the device is not affected by any damage

The additional $\Delta R_{ON}$ in semi-ON cannot be attributed to HE injection in the buffer:
- small measured HE mean free path (14 nm) in GaN
- results of hydrodynamic simulations (see next slide)

Dynamic-Ron increase in hard switching (red) and soft switching (blue) with different stress voltage ($V_{DD}$), and frequency of 10 kHz

Minetto, TED 67, 4602 (2020)
Modolo SST 36, 014001 (2020)
Proposed trapping mechanism in semi-ON state: the electrons in the 2DEG acquire high enough energy to overcome the AlGaN barrier and to get trapped into states at the passivation/AlGaN interface.

At the end of the trapping transient, interface traps are occupied in correspondence of the hotspots at the drain edge of the gate and in the access region close to the field-plate edge.

Minetto, TED 67, 4602 (2020)
EVIDENCE OF HOT-ELECTRONS IN HARD-SWITCHING CONDITIONS

Electroluminescence measured under hard-switching conditions at different voltages

Dependence of EL signal on the switching voltage for different device conditions. A significant increase in the EL signal is observed above 350 V, indicating hot-electrons during hard switching

Meneghini, IEDM 2018
In off-state conditions, both lateral and vertical breakdown may occur.

**The lateral breakdown voltage** mostly depends on the geometry of the device, and is typically proportional to the distance between the gate and the drain terminals.

**The vertical breakdown voltage** depends on the properties of the epitaxial layers. When the devices are operated in off-state, a large field drops on the uid-channel layer and on the GaN buffer.
**LATERAL DEGRADATION RELATED TO DIELECTRICS (EXTRANSCIC)**

**Extrinsic failure may be related to lateral breakdown**

- OFF-state stress induces time-dependent breakdown
- TEM analysis demonstrates degradation located in the gate edge at the drain-side → **dielectric failure**
- Can be solved by adding a graded SiN passivation under gate head

---

Rossetto et al., IEEE-TED 64, 73 (2017)
Rossetto et al., IEEE-TED 65, 1303 (2018)
Laterale degradation related to dielectrics (extrinsic)

The voltage required for the catastrophic failure decreases exponentially with increasing $L_{GH}$.

An additional SiN layer is introduced in order to reduce the electric field at the edge of the gate. The extra nitride layer increases time to failure by one order of magnitude.

Rossetto TED 64, 73 (2017)
The failure mechanism was found to be strongly field-dependent, and weakly thermally activated ($E_a=0.25$ eV).

The failure was ascribed to the creation of defect paths (due to percolation) between drain and substrate.

(a) Schematic representation of the device under test
(b) Drain current monitored during a constant voltage stress ($V_D=800$V)

https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7994660
HOW TO INCREASE THE VERTICAL BREAKDOWN VOLTAGE OF GaN-ON-Si STACKS?

- Increase in breakdown voltage with semi-insulating substrates → depletion of substrate splits voltage drop between EPI and substrate
  - plateau region in the vertical I-V plots, trade-off with trapping
- A further improvement can be obtained by increasing the SL thickness

Resistivity:
- $\rho = 0.01 \, \Omega \cdot \text{cm}$
- $\rho = 1 \, \Omega \cdot \text{cm}$
- $\rho = 6 \, \Omega \cdot \text{cm}$

We compared three structures obtained by sequential epitaxial growth on Si substrate.

Tajalli et al., Micromachines 2020, 11, 101

The presence of a large density of V-pits in wafers A and B resulted in a high variability in the IV curves.

The use of a thick GaN:C layer results in a much narrower distribution of the leakage curves.
No avalanche? No problem! GaN FETs are surge robust

GaN lateral transistors do not have avalanche capability → Is this a problem?

A recent (IRPS2019) presentation by Bahl et al. demonstrated that they are surge-robust in power supplies (720 V, 61000-4-5 industry-standard surge waveform), for 50 strikes

There was no loss of efficiency, and neither the high- nor low-side GaN FET showed hard failure

https://e2e.ti.com/blogs_/b/powerhouse/archive/2019/04/03/no-avalanche-no-problem-gan-fets-are-surge-robust#

For Si transistors, avalanche rating relates to the ability of silicon power FETs to survive power-line disturbances

In Si FETs, not much headroom above max voltage rating

If silicon FETs had been able to switch through surge events, then the thinking would have been different
Wait a minute!

Are these fundamental limits of GaN?

NO!
Degradation mechanisms are continuously identified and solved

Always better devices

Dynamic-Ron
Gate reliability
Off-state degradation
Hard switching
ESD events

More tests with respect to conventional Si-JEDEC
Qualified GaN reduces system size, thus resulting in better system reliability
Better converter & new applications

First 900 V devices already on the market
Now exploring the 1200 V range, see also
http://www.inrel-npower.eu

https://www.jedec.org/sites/default/files/files/4_1%20%20ROCS%202017_presentation.pdf

GaN power transistors: devices, technology and reliability – matteo.meneghini@unipd.it
• The competition with Si/SiC is becoming stronger
• GaN lateral: sensitive to surface trapping, BDV scales with area (i.e. with cost), lower current density
• GaN vertical devices can target the 1-10 kV range, with low $R_{on}$ and parasitic capacitance

Over the last years, we’ve evaluated/tested different structures:

All of these structures have potential advantages and drawbacks, in terms of reliability ⇒ Not problems, but research opportunities!
GaN power transistors: devices, technology and reliability – matteo.meneghini@unipd.it

Polarization doping

- GaN:Mg > 10^{20}, 20 nm
- Polarization-doped p-AlGaN, Mg 10^{19}, Al 5 \rightarrow 0\%, 400 nm
- Polarization-doped n-AlGaN, Al 0\rightarrow 5\%, 1 \mu m
- GaN:Si 2 \times 10^{16}, 7 \mu m
- GaN:Si 10^{18}, 200 nm
- GaN substrate

- polarization charge to induce mobile holes
- better transport: less impurity scattering
- better electrical characteristics at low temperature

Polarization-doped devices have avalanche capability \rightarrow positive temperature coefficient (consistent with literature)

De Santi, IEDM 2018 (UNIPD and Cornell collaboration)
GaN-based VFET are very promising for application in power conversion

At high gate voltages, drain current flows vertically through the channel formed (by accumulation) at the Al₂O₃/GaN interface

Below threshold (~1 V), the channel is depleted

Investigated issues:
- Trapping at the gate insulator
- Stability at high drain bias

Ruzzarin, TED 10.1109/TED.2017.2716982 (UNIPD and MIT collaboration)
DYNAMIC BEHAVIOR UNDER OFF-STATE AND POSITIVE GATE BIAS

The analyzed devices (optimized for 200 V operation) do not show significant current collapse up to $V_{DS} = 200$ V.

No deep trap is found in n-type GaN (no intentional doping, apart Si).
NANOWIRE-BASED TRANSISTORS

Robust (and high) threshold voltage

NBTI-free devices

Ruzzarin, APL 117, 203501 (2020)
NEXT-GENERATION VERTICAL GaN DEVICES (ALSO ON Si SUBSTRATE)

Mukherjee, *Materials 2020, 13*(21), 4740
Mukherjee, IRPS 2020

GaN power transistors: devices, technology and reliability  – matteo.meneghini@unipd.it

http://www.ultimategan.eu/
REALISTIC DEVICES (STILL UNDER STUDY)

Schematic cross-section of the developed vertical GaN trench MOSFET with FP edge termination

https://iopscience.iop.org/article/10.7567/1347-4065/ab02e7/pdf
Comparison of reverse recovery characteristics of GaN SBD chip mounted in a TO–247 package and commercially available Si FRD and SiC SBD

https://iopscience.iop.org/article/10.7567/1347-4065/ab02e7/pdf

Figure shows the measured dynamic characteristics with resistive load at a supply voltage of 300 V and a drain current of 10 A

The rise time and fall time of the GaN MOSFET is about half or slightly shorter than those of the SiC MOSFETs

Delay times of the GaN MOSFET, especially turn-on, are much shorter than those of the SiC MOSFETs (smaller capacitances and intrinsic gate resistance of the GaN MOSFETs)
Building blocks for the production of all-GaN power ICs:

- half-bridges
- diodes
- capacitors
- drivers
- dead-time control
- level shifters
- pulse-width modulation
- diagnostic and protection circuits
- regulators
- bandgap reference
- bootstrap circuits

Source: [https://compoundsemiconductor.net/article/111292/Monolithically_Integrated_GaN_Power_ICs/feature](https://compoundsemiconductor.net/article/111292/Monolithically_Integrated_GaN_Power_ICs/feature)
Key to success:

- electrical isolation between different modules → combining trench isolation with the incorporation of a buried oxide layer on SOI substrate
- Suppression of crosstalk → Si (111) is cut-off by deep trench

Source: https://compoundsemiconductor.net/article/111292/Monolithically_Integrated_GaN_Power_ICs/feature
Lack of complementary pFET devices $\rightarrow$ Resistor-transistor logic (RTL) $\rightarrow$
next step is integrating a depletion-mode HEMT, which replaces the 2DEG with E/D-mode co-integration, and will drive an improvement in GaN IC performance

pMOS is replaced by 5 $\mu$m wide 2DEG resistor

p-GaN gate HEMT with $W=6$ $\mu$m and $L_{GD}=1.5$ $\mu$m is used for logic nFET

Source: [https://compoundsemiconductor.net/article/111292/Monolithically_Integrated_GaN_Power_ICs/feature](https://compoundsemiconductor.net/article/111292/Monolithically_Integrated_GaN_Power_ICs/feature)
The designed all-GaN ICs have been successfully processed on 200 mm GaN-on-SOI.

Transient switching waveforms of a **48 V-to-1 V single-stage buck converter**, where the $V_O$ gradually stabilised at 1 V, proving the function of the GaN IC.

Detailed single pulse of the converter, highlighting a **narrow pulse width of 46 ns and a low duty cycle of 2.2 percent**, which guarantees the high switching frequency of **0.5 MHz**.

Source: [https://compoundsemiconductor.net/article/111292/Monolithically_Integrated_GaN_Power_ICs/feature](https://compoundsemiconductor.net/article/111292/Monolithically_Integrated_GaN_Power_ICs/feature)
CONCLUSIONS

• GaN is an excellent material for power electronics → High speed, high breakdown voltage
• Great flexibility (improved design, new applications)
• Great reliability → Reliability issues are being continuously discovered and solved → Not fundamental limitations, but research challenges (900 V devices already on the market, JEDEC-qualified transistors available)

Future directions:
• kV-range lateral devices
• vertical GaN devices (already subject of many research projects)
• integration (first GaN ICs commercially available, MHz-range operation)

We are still scratching the surface → Novel device structures are being studied, developed and investigated to further increase performance and reliability