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SiC vs IGBT Costs & SiC Substrate Surface Quality

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Director of Strategic and Technical Marketing

PowerAmerica Panel Discussion | Aug 3-5, 2021

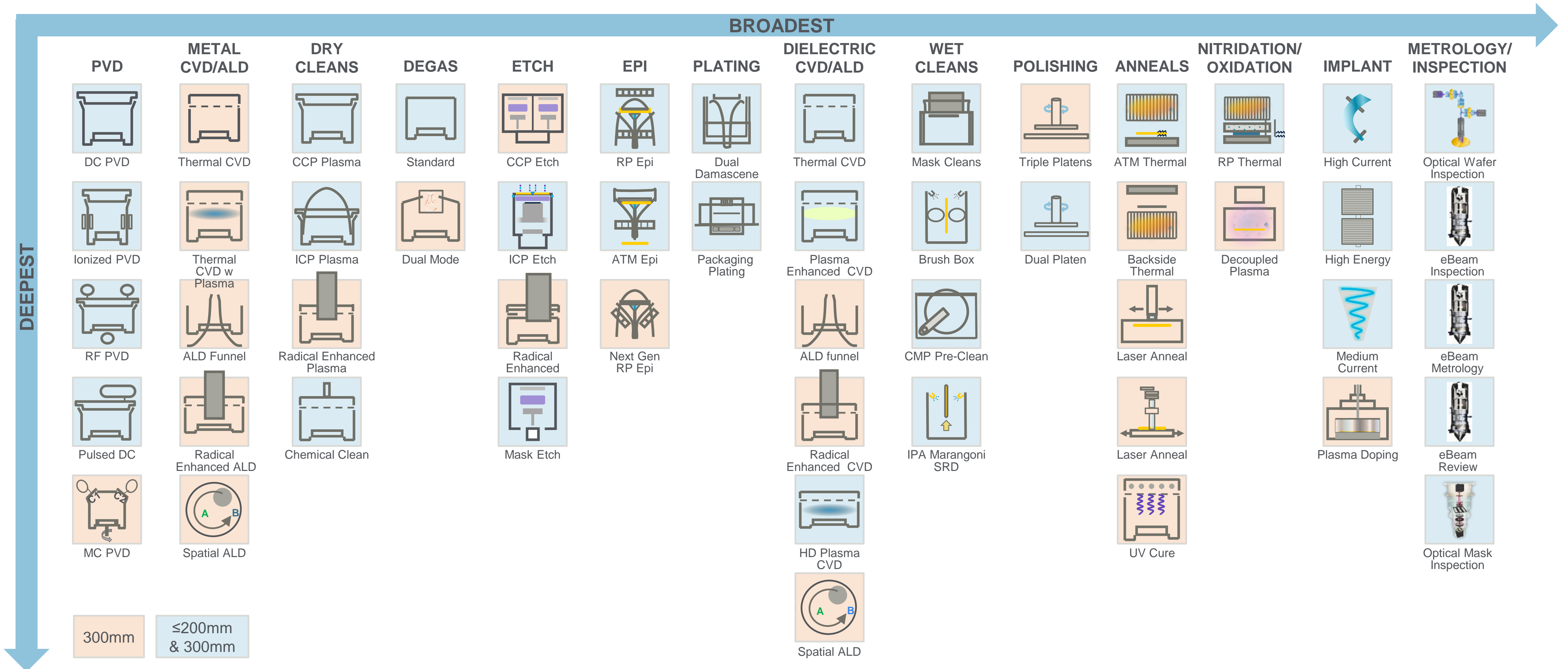
ICAPS

IoT Coms Auto Power Sensor

Increase focus on specialty markets
Better serve diverse customer base
Pursue opportunities for new technology and new business models

External Use

ICAPS | Applied Materials Product Portfolio



150 / 200 / 300mm Wafer Fab Equipment for Silicon and Compound Semiconductors

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Agenda

1 IGBT vs SiC MOSFET cost – transitioning to larger wafer sizes

2 SiC substrate surface quality – ready for epitaxial growth

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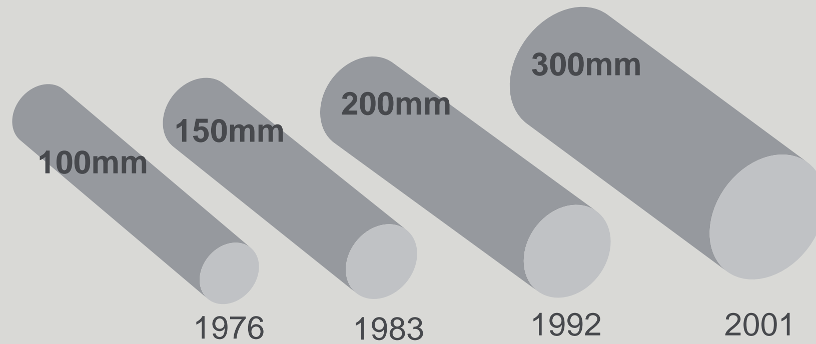
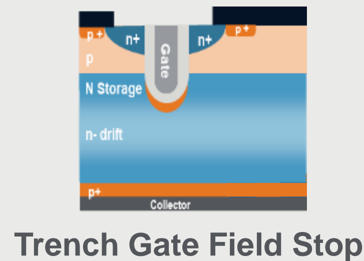
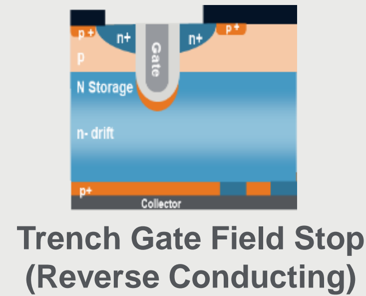
200mm Silicon Wafers - In Production for 30 Years
200mm Silicon Carbide Wafers - Start Production in 2022

IGBT





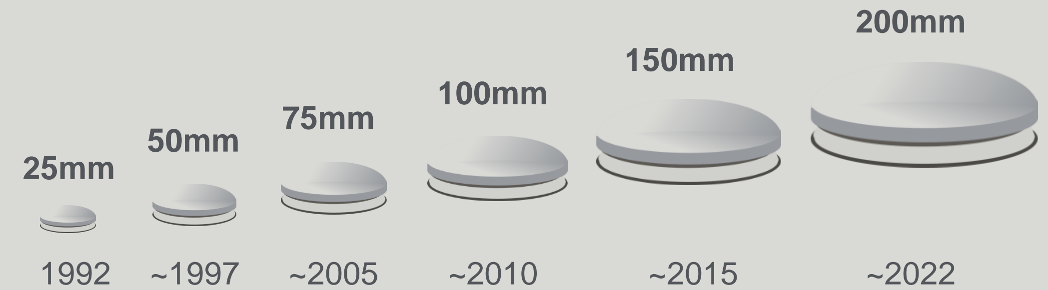
Trench Gate Field Stop

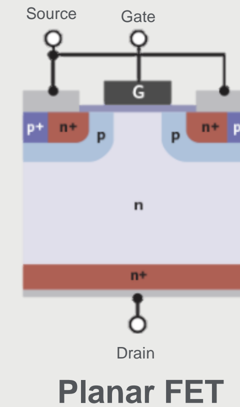


Trench Gate Field Stop (Reverse Conducting)

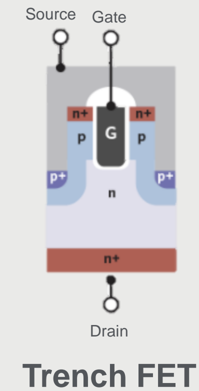
SiC MOSFET

*High volume production





Planar FET



Trench FET

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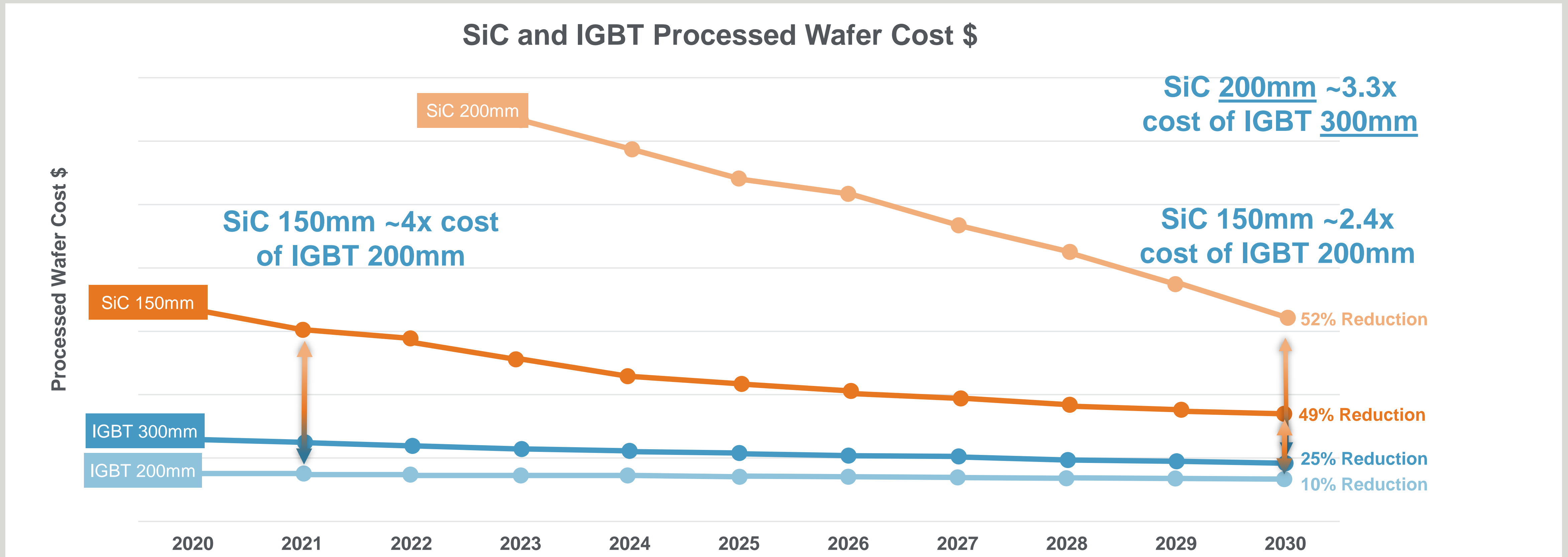
Processed Wafer Cost of SiC MOSFET Will Always Cost More Than Si IGBT

- SiC Processed Wafer Cost will Decrease ~50% by 2030



Source: Systems Plus, Omdia, PowerQ Consulting, Applied Materials

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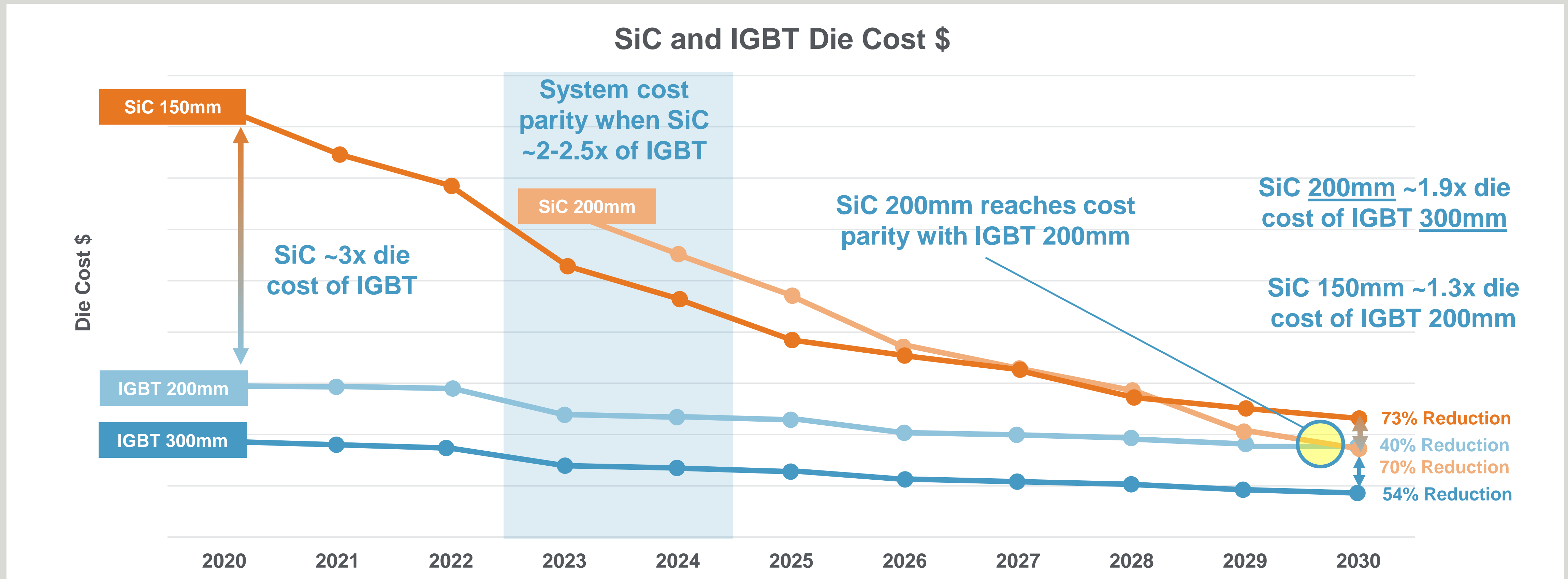
SiC MOSFETs Must Transition to 200mm Wafers to Compete with IGBTs at 300mm

- SiC die cost parity in 2029; however IGBTs will transition to 300mm



Source: Systems Plus, PowerQ Consulting, Applied Materials

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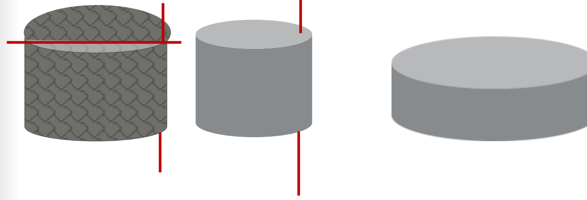
Creating a Finished SiC Substrate

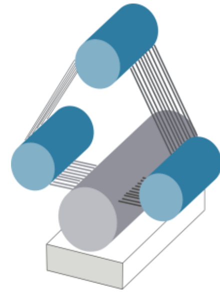
Sawing, Grinding and Polishing Second-Hardest Material in World!

Raw Boule

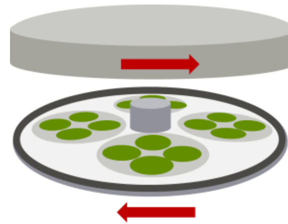
Processed Boule



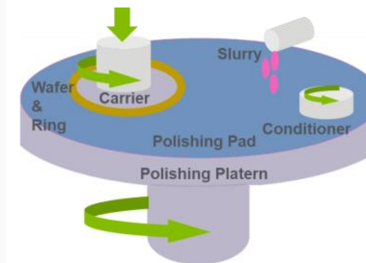
Slice – Wire Saw Laser



Mechanical Processing (Grind and Lapping)



Chemical Mechanical Polish (CMP) and Etch



Finished Substrate

Image Source: Entegris

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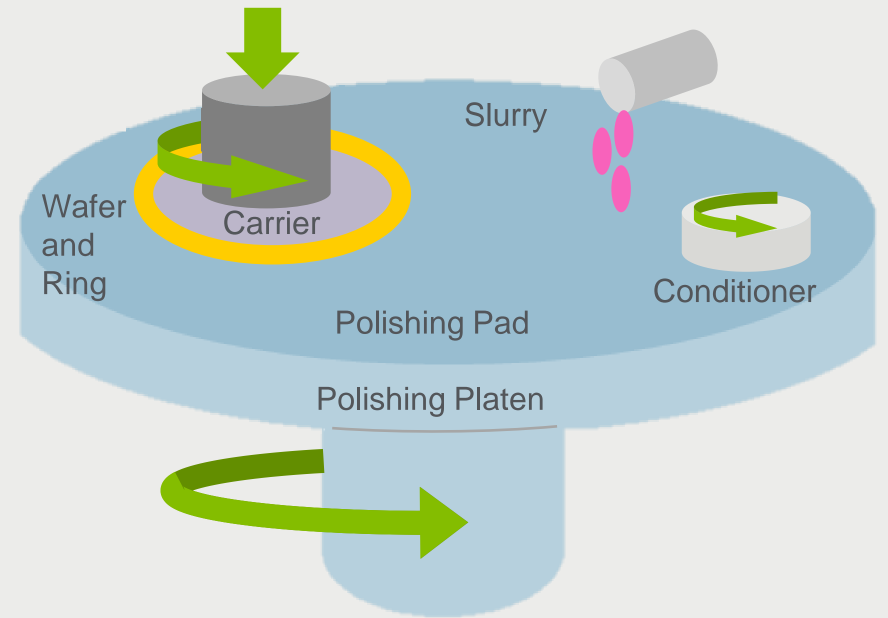
Highest-Quality Surface Critical for Epitaxial Growth with Fewest Defects

- Flat
- Smooth
- No Scratches
- No Particles
- No Pits



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CMP Requirements to Enable High Volume Manufacturing

Highest Quality

- Single-wafer processing (vs. batch)
  - Wafer-to-wafer repeatability/performance
- Insensitivity to pre-CMP wafer thickness variations
- Ability to modulate within-wafer thickness (multi-zone polishing head)
- Optimization in polishing sequence using multi-slurry configurations

Highest Productivity

- High throughput
  - Dry in, dry out
  - Wafer cleaning, drying
  - Material weight removal measurement
  - Wafer ID reading
- Lowest cost of ownership
  - Cost of slurries, pads, other consumables, power, cooling/cleaning water, etc.
- Capable of 200mm wafers

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Summary

1. SiC MOSFET processed wafers will always cost more than Silicon IGBT processed wafers. However, **SiC die cost will reduce to ~1.3x of IGBT in 2030** (150mm SiC vs 200mm IGBT)

2. **SiC substrate surfaces must be of the highest quality** to support the best epitaxial growth, resulting in fewer defects, and **higher device yield and reliability**

3. To meet the **surging demand** in EV, manufacturing tools, including CMP, must be **superior in manufacturing quality, throughput, and competitiveness**

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