Wide bandgap engineered substrates paving a new way for the Power Electronics industry

Power America Summer Workshop 2021
Thomas Piliszczuk EVP, Strategy Office
Outline

1. Introduction to Soitec
2. Smart Cut™ SiC solution
3. Power GaN epiwafer solution
4. Conclusion
Introduction to Soitec
Soitec – Who we are

DESIGNER & MANUFACTURER OF INNOVATIVE SEMICONDUCTOR MATERIALS

1. Largest manufacturer of engineered substrates
   LEADER

2. Unique technologies
   SMART CUT™, SMART STACKING

3. High-growth markets
   MOBILE COMMUNICATIONS, AUTOMOTIVE & INDUSTRIAL, SMART DEVICES

4. Wafer fabs (150, 200 & 300 mm)
   FRANCE, BELGIUM, SINGAPORE, CHINA*

5. Employees Worldwide
   GLOBAL PRESENCE**

---

We design and deliver innovative substrates & solutions to enable our customers’ products shaping everyday life.

*Partnership with Shanghai Simgui Technology Co. Ltd. (Simgui)
Soitec has built a unique position in the value chain...
Key contributors to enable growth

- Continue Moore’s Law
- New architectures
- New structures / 3D
- New materials
- New ways to shrink
- Advanced packaging

PPAC
TIME TO MARKET
SUSTAINABILITY

ENGINEERED SUBSTRATES
Global industrial footprint - Capacity expansion

- **SOITEC BERNIN 1, FRANCE** - 950K wafers/year - max capacity
- **SOITEC BERNIN 2, FRANCE** - from 650K improved up to 700K wafers/year - max capacity
- **SOITEC BERNIN 3, FRANCE** - from 500K improved to 750K wafers/year - max capacity
- **SOITEC BELGIUM N.V HASSELT, BELGIUM** - 60K wafers/year - max capacity
- **SOITEC BERNIN 2, FRANCE** - from 650K improved up to 700K wafers/year - max capacity
- **SIMGUI SHANGHAI, CHINA** - from 350K push to 450K wafers/year - max capacity
- **SOITEC BERNIN 3, FRANCE** - from 500K improved to 750K wafers/year - max capacity
- **SOITEC PASIR RIS, SINGAPORE** - 1M wafers/year - max capacity

**NEW CAPACITIES (PENDING BUSINESS MILESTONES)**

- **300 mm**
- **150 mm**
- **200 mm**
- **300 mm SOI CAPACITY EXPANSION** - 1M wafers/year - max capacity
- **150 – 200 mm SiC NEW CAPACITY EXPANSION** - 1M wafers/year - max capacity

**NEW CAPACITIES**

- **200 mm**
- **300 mm**

**NEW CAPACITIES**

- **300 mm SOI CAPACITY EXPANSION** - 1M wafers/year - max capacity
- **150 – 200 mm SiC NEW CAPACITY EXPANSION** - 1M wafers/year - max capacity
Soitec addressable market expected to more than double in the next five years

~7 MILLION WAFERS ADDRESSABLE MARKET IN FY26

x2.5 GROWTH
FY 2021 - 2026

SOITEC SERVES 3 STRATEGIC END MARKETS

MOBILE COMMUNICATIONS
RF-SOI, FD-SOI, POI, GaN

AUTOMOTIVE & INDUSTRIAL
Power-SOI, FD-SOI, SiC, GaN

SMART DEVICES
FD-SOI, Imager-SOI, Photonics-SOI, PD-SOI
Soitec products portfolio automotive & industrial

APPLICATIONS
- Autonomous driving systems
- Connected car
- Vehicle electrification
- Industry 4.0

SOITEC PRODUCTS ENABLE
- Autonomous driving
- Infotainment
- Vehicle electrification

Power-SOI
Power management IC, In-vehicle networking & gate driver

FD-SOI
MCUs, ADAS-Radar
ADAS-Vision

GaN
DC-DC converters
On-board charger

Smart Cut™ SiC
Automotive electrification
Soitec solutions for Power applications

Very Low Voltage
- Wearable
- IoT
- Mobile Devices

Low Voltage
- Power Supply
- Smart actuator & pneumatics
- IVN, PMIC, BMIC
- Class D Audio Amplifier

Medium Voltage
- Medical Equipment
- Motor control
- Power Inverter
- UPS
- Fast charging, USB adaptors

Very High Voltage
- Windmill
- Freight & Vessels
- Smart Grid
- Rail Transport

Power - SOI (30V ~ 900V), BCD Process, High Integrated System, < 200W

EpiGaN-HV (100V ~ 650V ~ 1.2kV)
- E- & D-mode GaN/Si transistors

SiC (600V ~ 10kV), SiC Transistor

< 1V 3.3V 20V < 200V 600V 900V 1700V 3.3kV 10kV+
Smart Cut™ SiC Solution
EV market acceleration

- **Acceleration of EV deployment driven by:**
  - CO₂ regulations
  - Battery cost reduction
  - ICE Bans

![Graph showing CO₂ emission regulation (gCO₂/km) for 2020, 2021, and 2030 with a further reduction plan in EU.]

Source: ICCT 2020

- **SiC is key to address the challenges of EV adoption**

- **Reduction in EV Battery cost**

![Graph showing reduction in EV battery cost from 2010 to 2030.]

Source: DNV 2020, Evercore 2020

- **Internal combustion engine bans or electrification targets**

![Chart showing countries and years for internal combustion engine bans or electrification targets.]

Source: IEA 2021

- **SiC**
  - Weight
  - Reliability
  - Thermal conductivity
  - Range anxiety
  - Charging time
  - Cost
The key challenges for greater SiC market adoption

- Quality: Quality and reliability issues caused by defects coming from wafer materials and/or epitaxy
- Device Cost of ownership: High substrate, epitaxy and processing yield are needed to reduce device cost
- Scalability: 200 mm time to market for SiC device roadmap acceleration

Availability of large diameter and high quality substrates are the key challenges
**Smart Cut™ SiC: the new paradigm for availability, higher yield and scalability**

**MAJOR STAGES OF SMART CUT™ SiC**

- **Donor wafer**: Prime quality SiC
- **Handle wafer**: Low Res SiC
- Conductive bonding interface
- Finishing including CMP & high temperature anneal
- Donor wafer re-use for new process cycle
**Smart Cut™ solution: SiC engineered substrate**

Current industry solution (monocrystalline bulk)

- Conventional SiC substrate

SiC Device structure

- Device
- Epi layer (drift)
- Conversion buffer
- Substrate

Smart Cut™ engineered Epi-ready substrate solution

- Device Epi ready SiC layer
- Low resistivity substrate
**Smart Cut™ SiC for Automotive and Industrial applications**

### Value proposition

Smart Cut™ SiC vs SiC: It is all about device yield and performances!

- 25% higher yield on large SiC MOSFETs
- Up to 20% lower resistance per device reducing energy losses
- BPD-free for improved reliability
- 200 mm scalability to accelerate SiC adoption

### Existing and future applications

- Electric mobility
- On-board chargers
- Traction inverter system
- Fast charging stations
- Inverters: industrial, renewable energy

### “Smart Cut™ SiC” product family roadmap from 2022

**Timeline**

- **200 mm Low resistivity Smart Cut™ SiC**
- **150 mm Low resistivity Smart Cut™ SiC**
- **150 mm Smart Cut™ SiC**
A reality today

6-INCH ENGINEERED SiC SUBSTRATE

FROM SiC BULK

→

TO ENGINEERED SMART CUT™ SiC

→

TO POWER DEVICES
From substrate crystal and surface defects to post epitaxy killer defects

- Killer defect
- Low impact defect
- Reliability defect
- Innocuous defect

Backgrinding, sorting, handling

Process

Ted, Carrot Triangl., SF, Down falls, Growth conditions

Substrate

MP, TED, BPD, TSD, Inclusions, µ scratches, LTV, TTV, SFQR, Bow, Warp

Post-epi defects are driving the fabrication yield

Low crystal defectivity, improved surface finishing, ultra flat substrate required to reach high yield

Source: Soitec

Source: H.Das et al (ON Semi) MSF 2019 Vol. 963, pp 284-287
Increased reliability, leading to increased die yield

- **Basal Plane Dislocations (BPD) free surface:**
  - Improvement of crystal quality by Soitec’s proprietary process.
  - For 20mm² devices, more than 98% of dies will be BPD free

- **Benefits for device manufacturers:**
  - No conversion layer
  - Drift epitaxy cost reduced by 10% for 1200V devices
  - No incoming wafer sorting needed
  - Increased wafer usage
  - No screening during process needed
  - Higher wafer-to-device yield

Source: Soitec
Demonstrated compatibility with full manufacturing process

- Smart Cut™ SiC substrates validated by EU partner through full JBS Diode manufacturing process
  - From drift epi to tested devices
- Equivalent performance than bulk SiC substrate from major vendor

Forward characteristics of JBS diode

Source: Soitec
Low resistivity receiver substrate

- Low resistivity Smart Cut™ SiC receiver substrate
  - 40% of standard SiC
  - Tighter on wafer distribution demonstrated

- Combined with low bonding interface specific resistance
  - Smart Cut™ SiC Substrate targeted Ron.A: < ⅓ of standard SiC

Low resistivity of Smart Cut™ SiC is a major differentiator for advanced MOSFETs
Current-density gain of Smart Cut™ SiC

- Smart Cut™ SiC substrate enables
  - to get >20% current gain on diodes => higher current rating product with same design and technology or
  - Die size reduction up to 15% => more good dies per wafer => lower die cost + lower switching losses or
  - High electrical performance with no back grinding => higher manufacturing yield and lower technology cost => lower die cost

True for both SiC diodes and MOSFETS
• Industry starting to move to 200 mm from 2022
• Smart Cut™ allows rapid product scalability to 200 mm
• Soitec line fully compatible with both sizes
SmartCut™ SiC for Greener, Faster, Better Power Electronics

50x bulk SiC wafers/boule

PVT-grown SiC boule

Standard SiC Wafering

Conventional SiC substrate

500x Smart Cut™ SiC wafers/boule

Handle Substrates

Smart Cut™ Process

~90% less energy per wafer
Power GaN epiwafer Solution
Power GaN switching device market will surpass $1B in 2025

- Fast charging applications for consumer are driving the GaN power market today
- New GaN product generations will penetrate data centers, industrial variable speed drive and EV markets (OBC, DC/DC, traction inverters) from 2025 onwards
GaN epiwafer production line at Soitec Belgium

- Industry-standard 150 mm & 200 mm HVM MOCVD reactors
- Full suites of high volume inspection and metrology capabilities

Source: Aixtron
Source: Soitec
Source: Soitec

Source: Soitec
Source: Aixtron
Soitec’s 200 mm GaN/Si structures for power switching

Product features:

- D-mode and E-mode GaN/Si structures produced on state-of-the-art HVM MOVCD tools
- **200V** and **650V** rated variants on 200 mm Si substrates
- In-situ SiN passivation as high-quality gate dielectric or surface passivation
- Customization of top layers for differentiation on the epistucture level
Excellent breakdown and negligible trapping with Strained Superlattice (SSL) Buffers

SSL-concept: alternating layers with compressive and tensile stress

- Soitec’s SSL provide sufficient breakdown margin in today’s 650V applications
- No dynamic Ron degradation up to 600V and elevated temperatures

Source: Soitec

Source: INREL-Npower Project, Farid Medjdoub, CNRS
Soitec’s product roadmap for GaN power switching

**TODAY**
- 200 mm GaN/Si
- 900V SSL buffer
- D- and E-mode

**FUTURE**
- 200 mm GaN/Si
- Up to 1200V SSL buffer
- Optimized D- and E-mode

- 200 mm substrates
- 600V up to 1200V SSL buffer
- Vertical devices
- Use of Smart Cut™ substrates

Source: YesvGaN consortium
1. Evolutive: Enabling low-cost vertical GaN transistors

- Drain contact on substrate back side
- Low specific on-resistance
- High blocking voltage
- Low substrate cost
- Current flow

Source: YesvGaN consortium

2. Development of new standards by leveraging Smart Cut™ technology

Utilize engineered Smart Cut™ GaN substrates optimized for thick, high-quality GaN epitaxy
- CTE-matched: will enable defect-free thick epilayers
- Elimination of parasitic substrate effects: reduction of device cross-talk
- Optimised thermal management

Soitec welcomes partners in the US/Power America ecosystem to participate in next gen. GaN technology development activities!
Conclusion
Conclusion

- GaN and SiC power devices adoption will continue to proliferate with the demand for energy efficient systems in energy generation, industrial and automotive industry.

- Through the optimization of the top layer and base substrate, Smart Cut™ SiC tackles the key challenges for further SiC adoption
  - Re-use of donor wafer ⇒ Increased availability of high quality substrates
  - Increased overall manufacturing yield ⇒ Lower manufacturing costs
  - Lowest Ron.A figure ⇒ Increased system efficiency

- Smart Cut™ SiC offers the fastest path to the high volume deployment of 200mm SiC substrates

- Soitec is establishing partnerships across the value chain for GaN and SiC in USA.
Thank you

Follow us on:

Facebook Soitec
Twitter @Soitec_FR / @Soitec_EN
LinkedIn Soitec

For more information, visit us at:
www.soitec.com
SOITEC PROPRIETARY
Any unauthorized reproduction, disclosure, or distribution of copies by any person of any portion of this work may be a violation of Copyright Laws, could result in the awarding of Damages for infringement, and may result in further civil and criminal penalties. All rights reserved. Copyright ©2021 SOITEC.