High-voltage SiC-Based Power Conditioning System Development for Grid Applications

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Power America WBG Devices and Applications Short Course

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PCS Development Outline

- Background
- 10 kV Device Characterization
- Driving and Protection
- Isolated Power Supply
- Control
- PCS Design and Testing
- Grid Supporting Function and Validation

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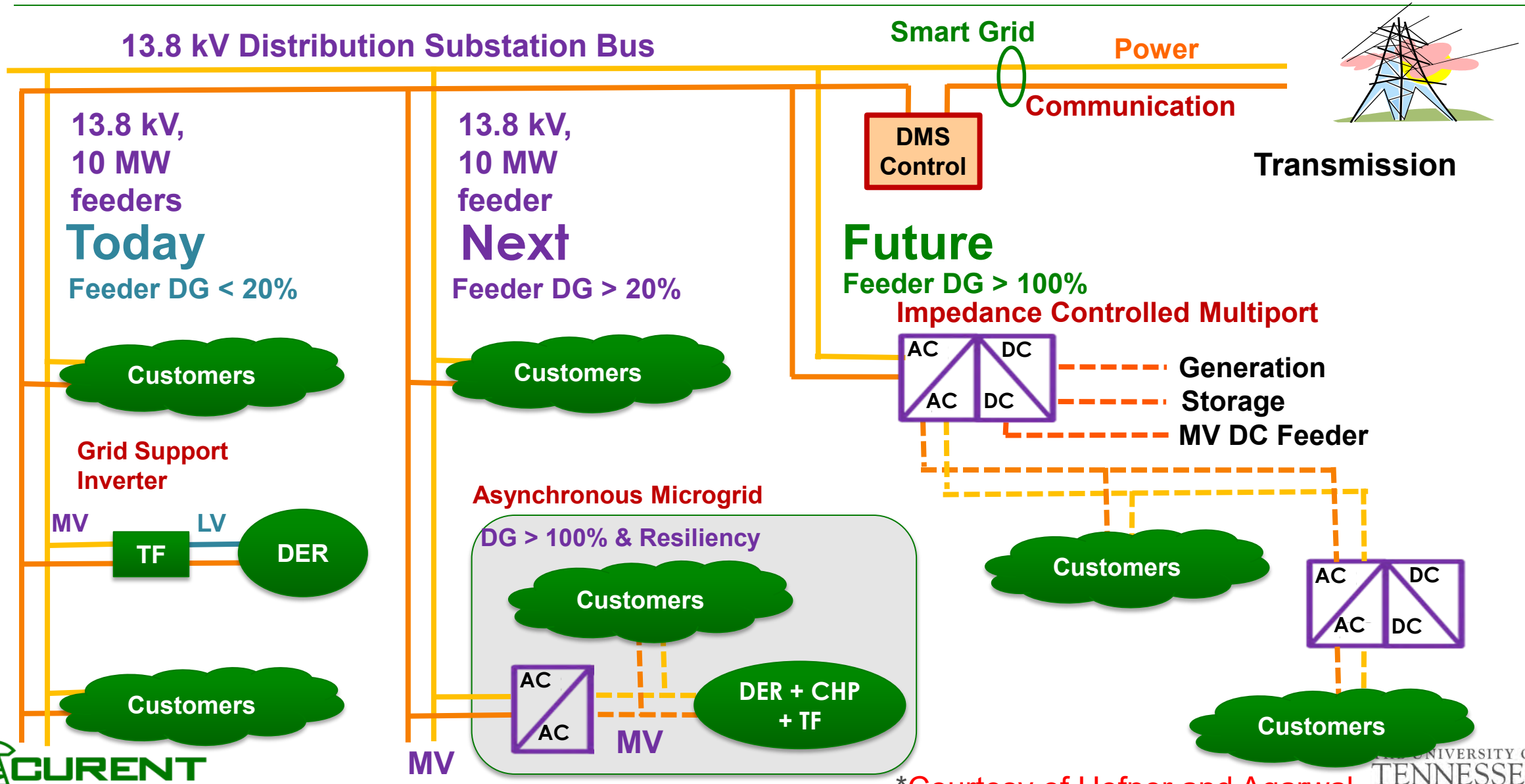
High Penetration of Distributed Energy Resources (DER)

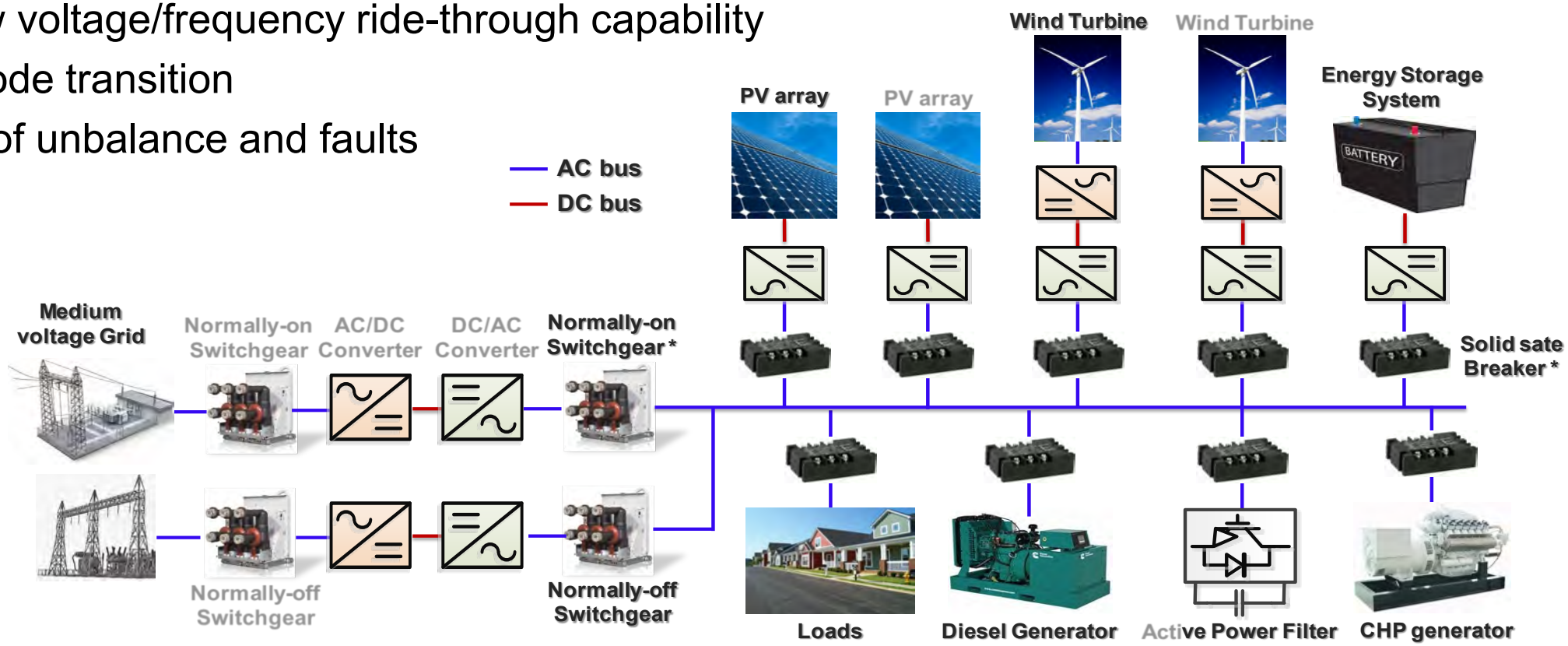


*Courtesy of Hefner and Agarwal

Asynchronous Microgrid

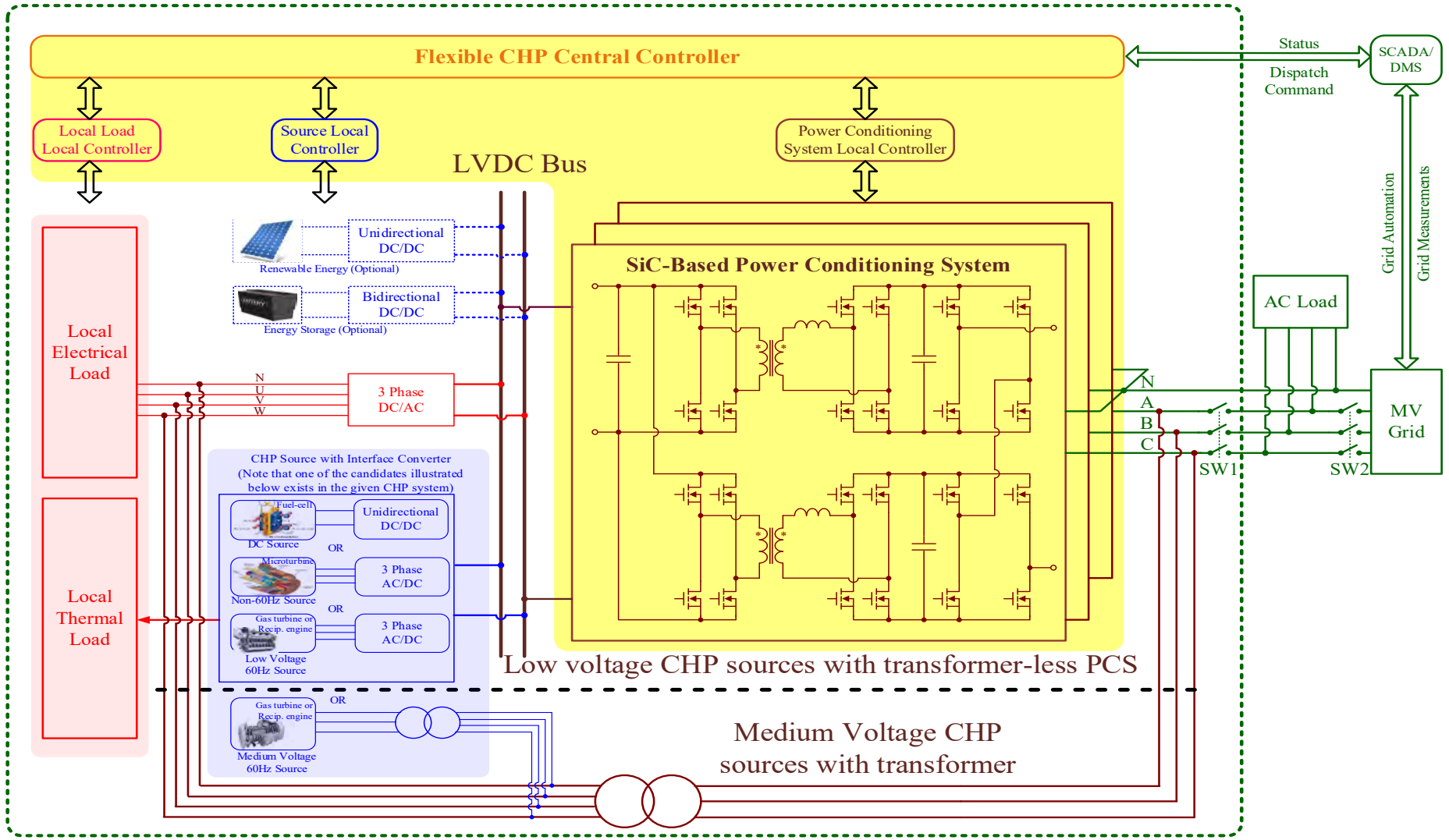
Asynchronous MG connects to an AC distribution grid through a microgrid power conditioning system (PCS)

- easier integration of renewable energy sources (RES)
- better low voltage/frequency ride-through capability
- easier mode transition
- isolation of unbalance and faults

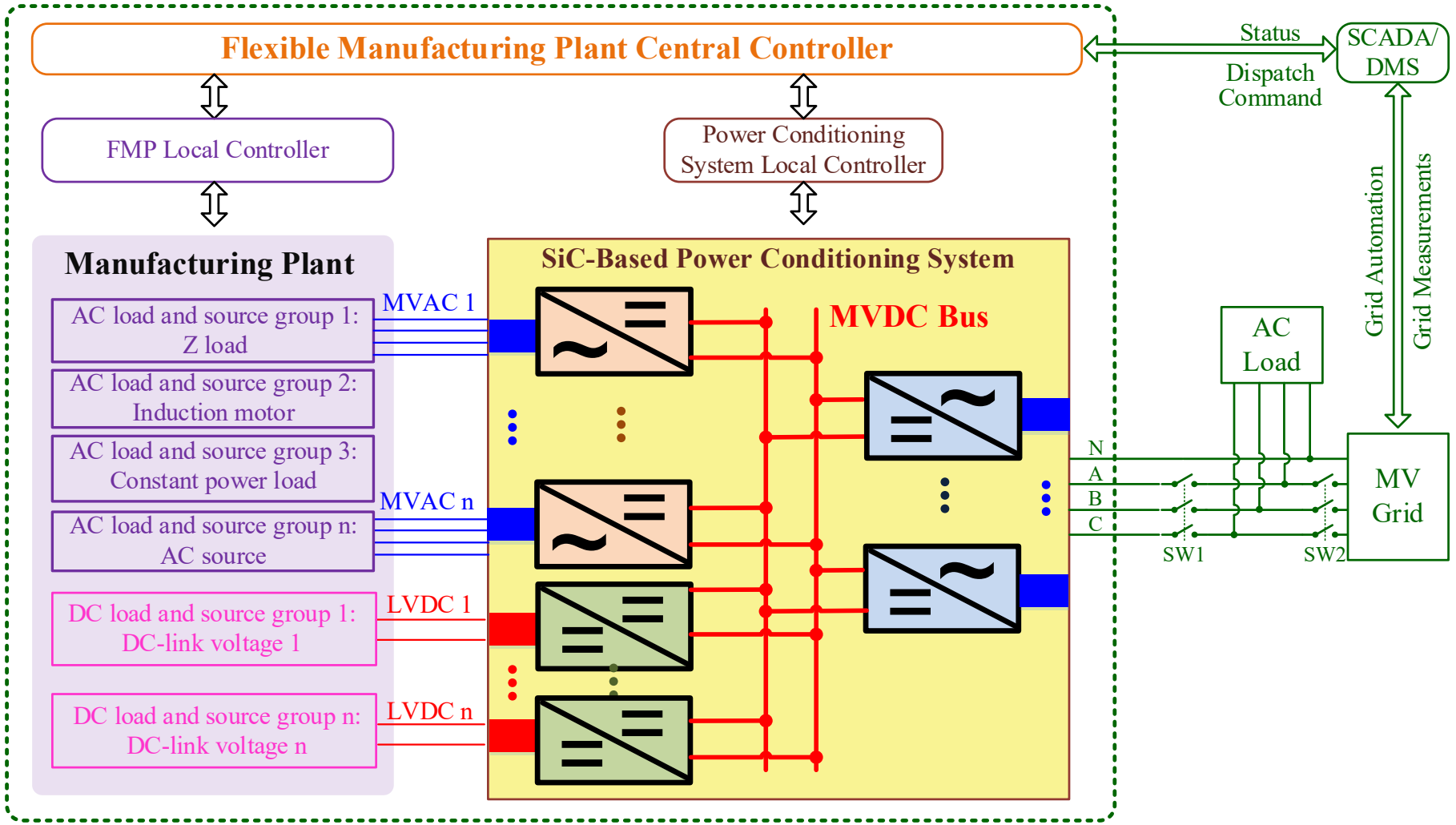


* Switchgear and solid state breaker can be replaced by other equipment with same functions

Flexible Combined Heat and Power (F-CHP)

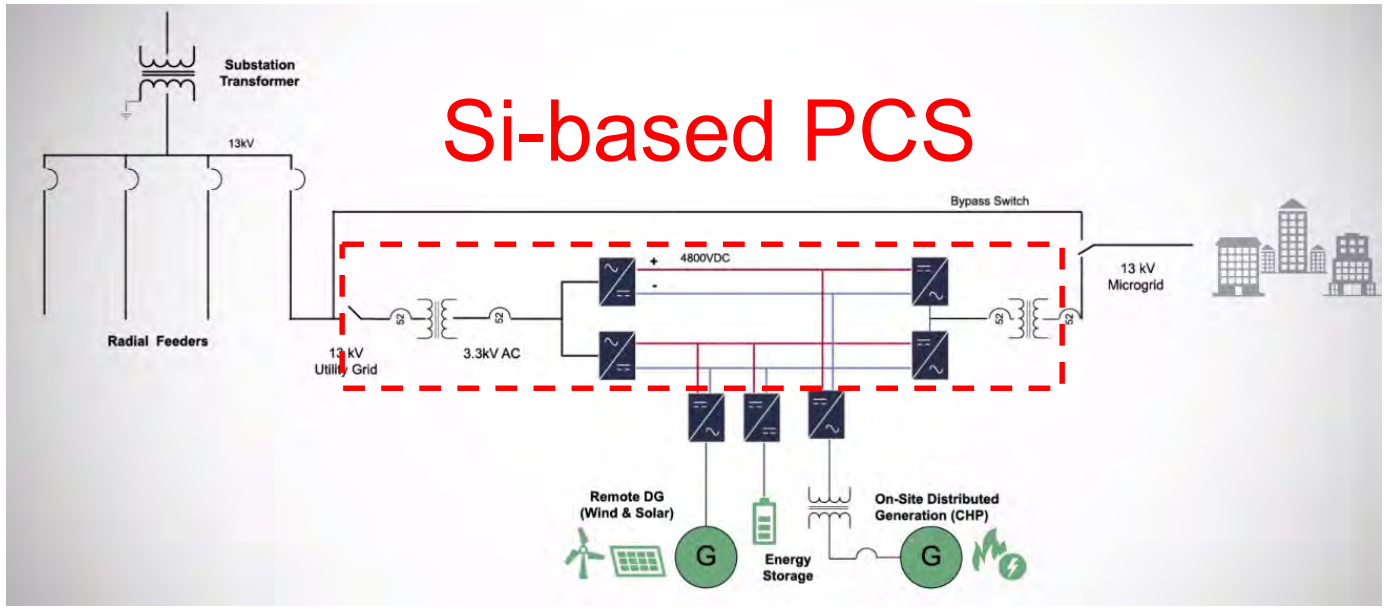


Flexible Manufacturing Plants (FMP)



Issues & Challenges with Si-based PCS

Si-based commercial PCS solution available (Pareto Energy)



- bulky and heavy 60 Hz transformer
- efficiency hit due to high loss of Si devices and bulky passives
- limited system-level benefits due to low control bandwidth

MV PCS Design Challenges and Needs

SiC based converter Issues due to fast switching, high dv/dt & di/dt, high voltage, high power; unique grid application requirements

Converter

- Device characterization
- Gate drive & protection
- Parasitics impact
- Control
- Passives & filters (dv/dt, di/dt, EMI etc.)
- Insulation (dv/dt, lightning and switching overvoltage)
- Thermal management

Scaling

- Device module series and paralleling
- Converter stacking and paralleling
- Modular topology

Grid Condition Tolerance

- Faults
- Unbalance
- Grounding
- Fault detection and protection coordination

Grid Support

- Frequency and voltage support
- Inertia emulation
- Low voltage ride through
- Stability enhancement
- Active filtering
- Black start

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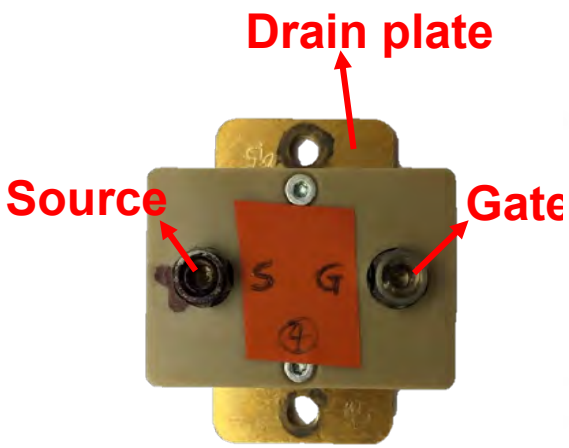
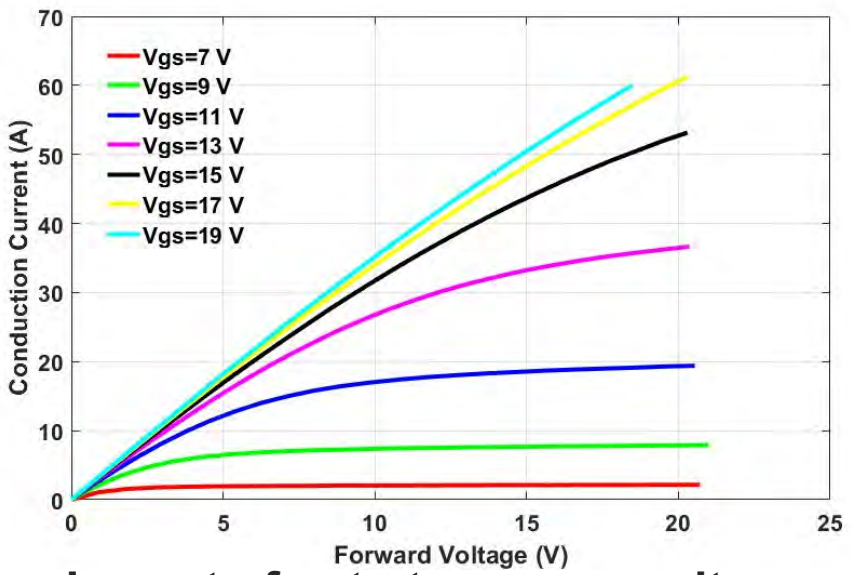
10 kV SiC Discrete MOSFET

❑Static Characteristics

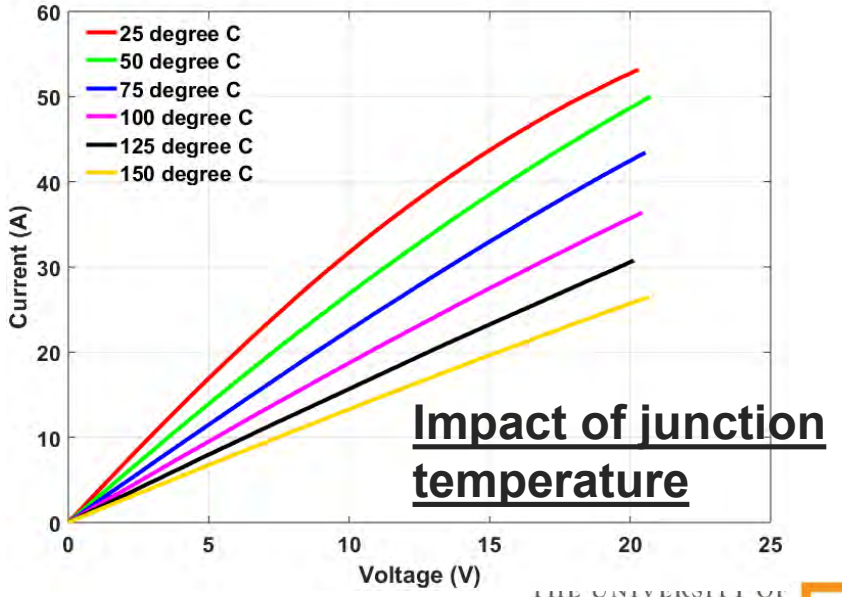
- Wolfspeed 3rd-Gen 10 kV/350 mΩ SiC MOSFET with non-isolated package and no Kelvin source
- Body diode can be used as the freewheeling diode
- On-resistance increases rapidly as temperature rises (750 mΩ at 150 ˚C), and it reduces slightly as Vgs increases if Vgs is higher than 13 V
- On-resistance is almost the same whether it is in forward or reverse conduction mode
- **Selected on-state V_{gs}: 15 V; hence lower short circuit current can be achieved**



Wolfspeed 10 kV/350 mΩ SiC MOSFET



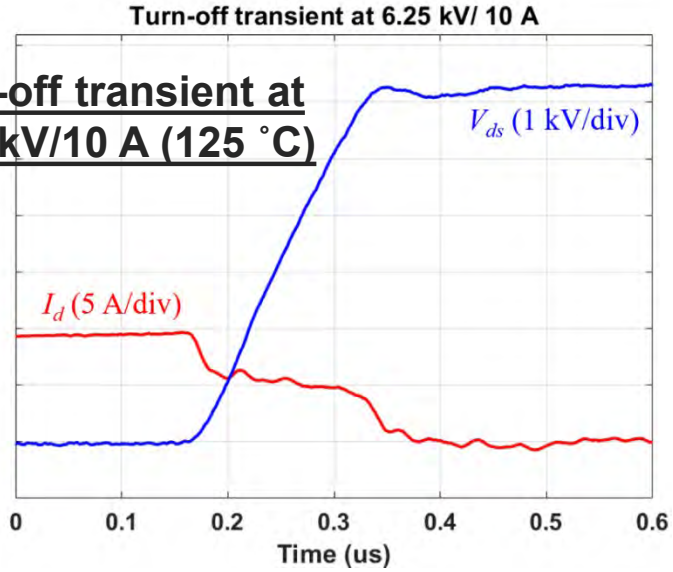
Impact of gate-to-source voltage

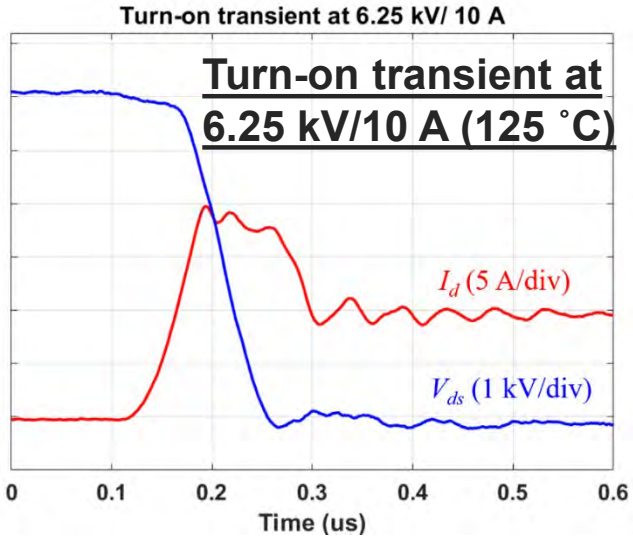


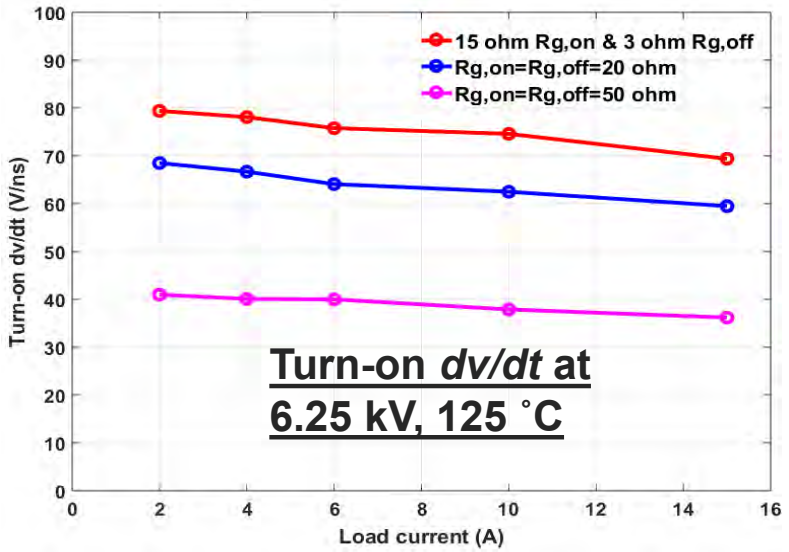
Impact of junction temperature

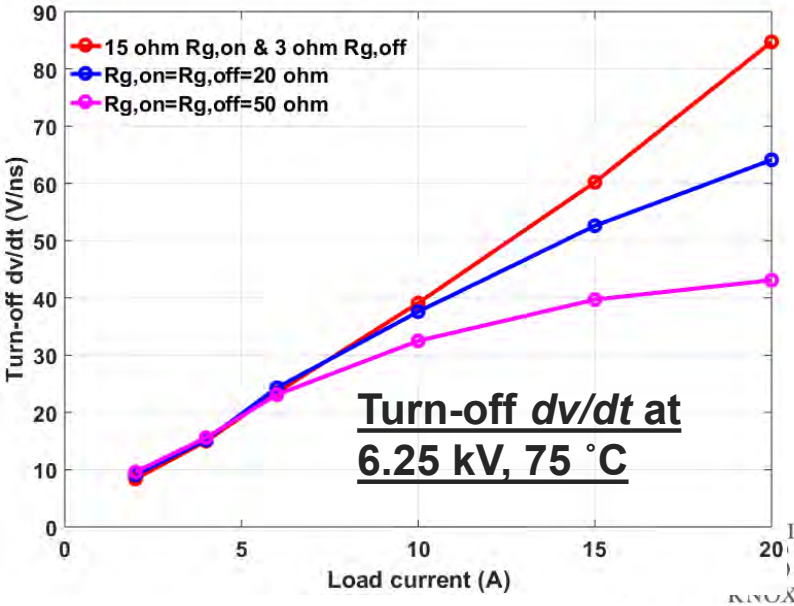
10 kV SiC Discrete MOSFET

❑DPT Waveforms







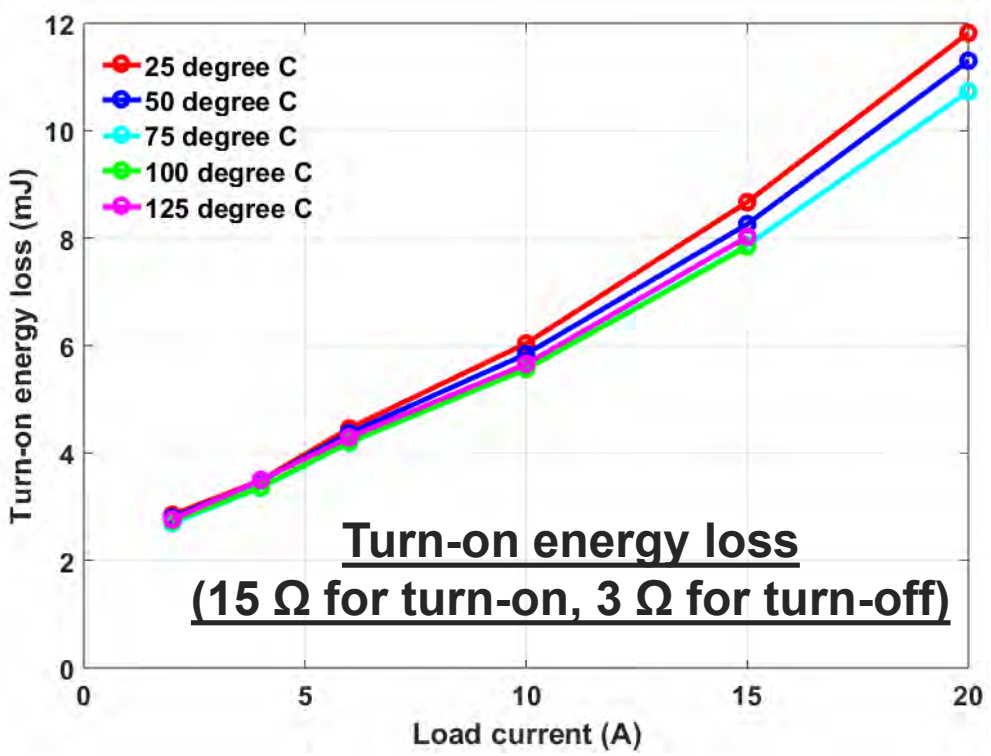


- Larger gate resistance slows down the turn-on transient
- Turn-off transient dominated by capacitive charging process, and hence not a strong function of gate resistance, especially at low current
- Gate resistance selection: 15 Ω for turn-on and 3 Ω for turn-off to limit dv/dt to 100 V/ns

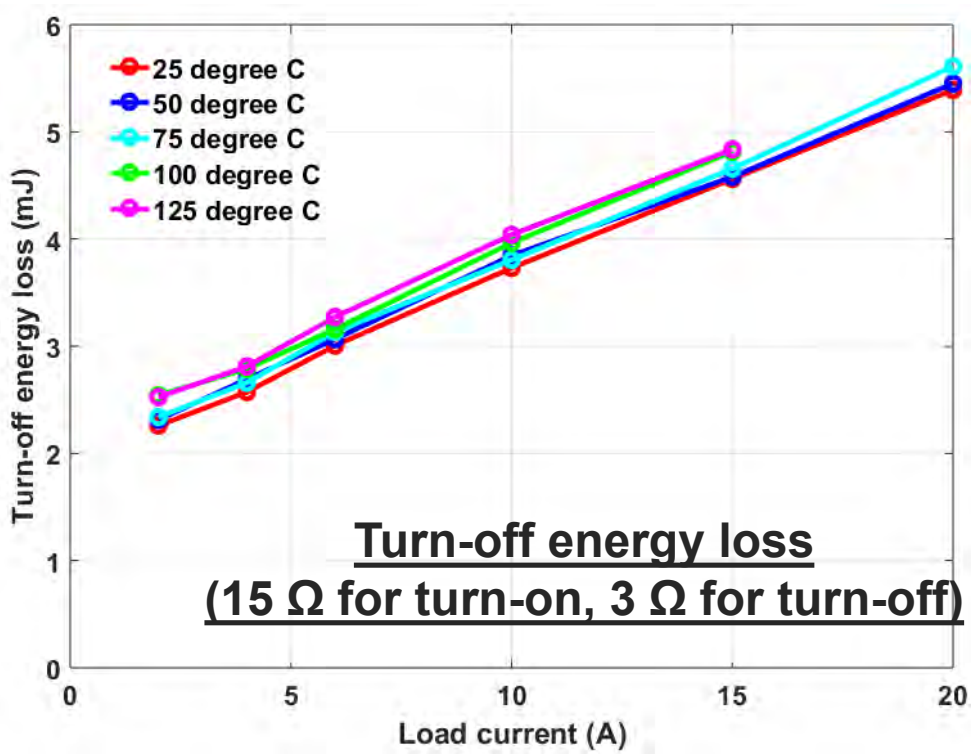
10 kV SiC Discrete MOSFET

❑Impact of Junction Temperature on Switching Losses

- Higher junction temperature leads to higher turn-on dv/dt and lower turn-on energy loss
- Turn-off transient is not a strong function of junction temperature, since it is dominated by capacitive charging process



Turn-on energy loss
(15 Ω for turn-on, 3 Ω for turn-off)

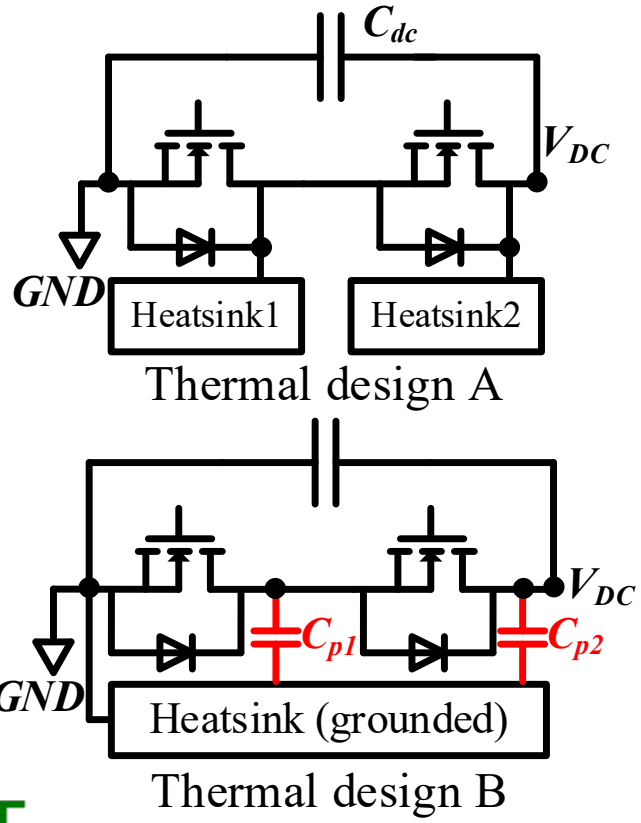


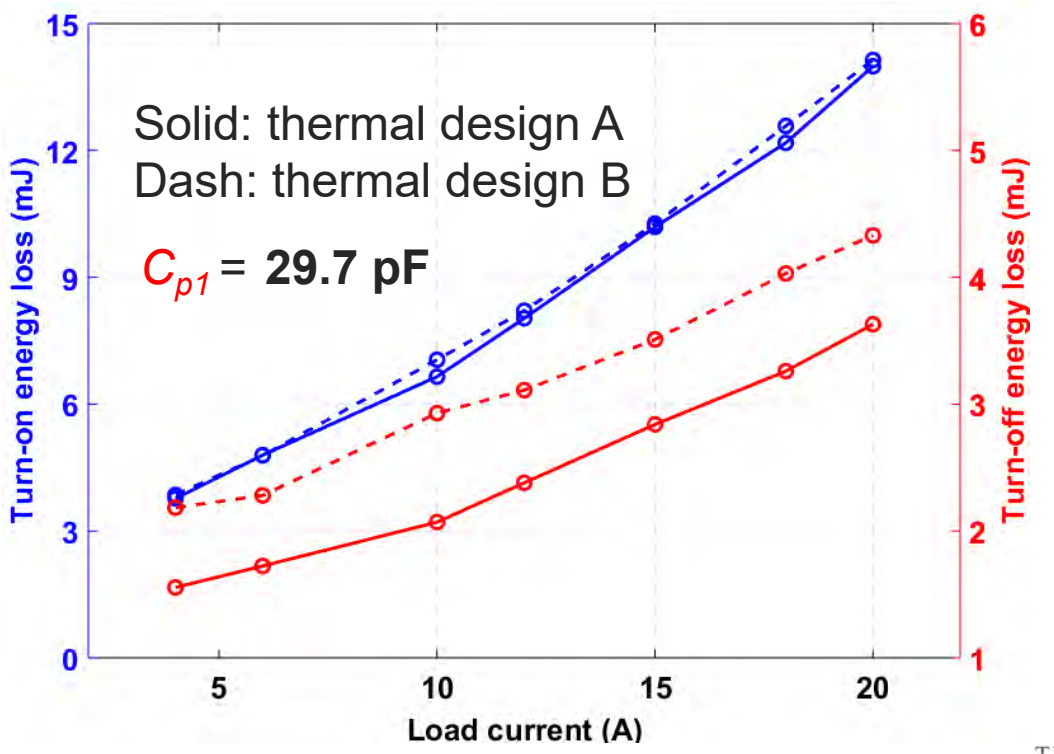
Turn-off energy loss
(15 Ω for turn-on, 3 Ω for turn-off)

10 kV SiC Discrete MOSFET

❑Impact of Heat Sink Parasitic Capacitance on Switching Losses

- Parasitic cap due to thermal design B significantly slows down the turn-off transient, with little impact on the turn-on transient
- Thermal design A can effectively reduce switching energy loss, especially at low current

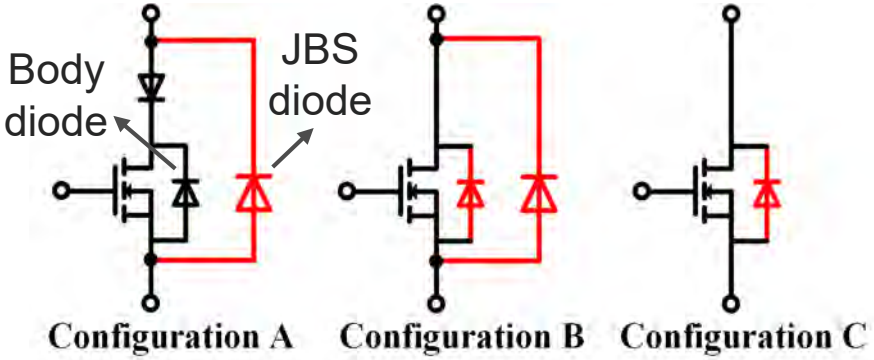




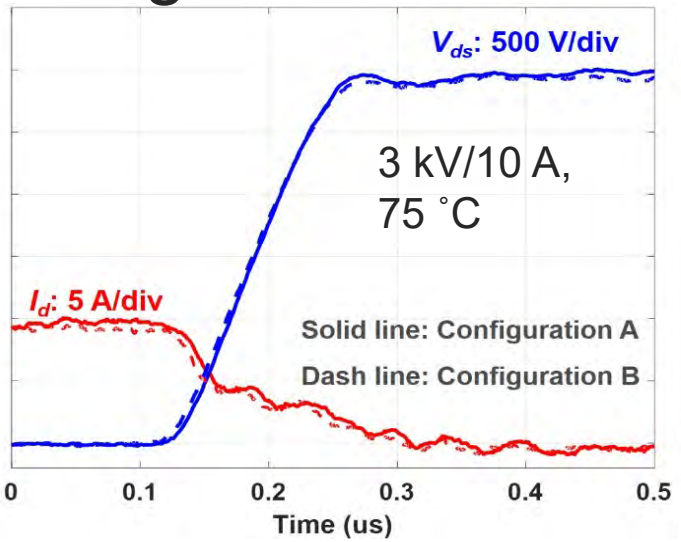
10 kV SiC Discrete MOSFET

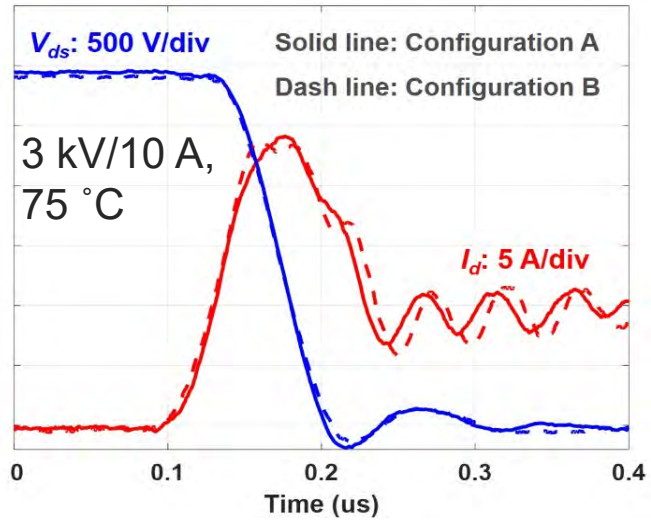
❑Impact of Body Diode on Switching Losses

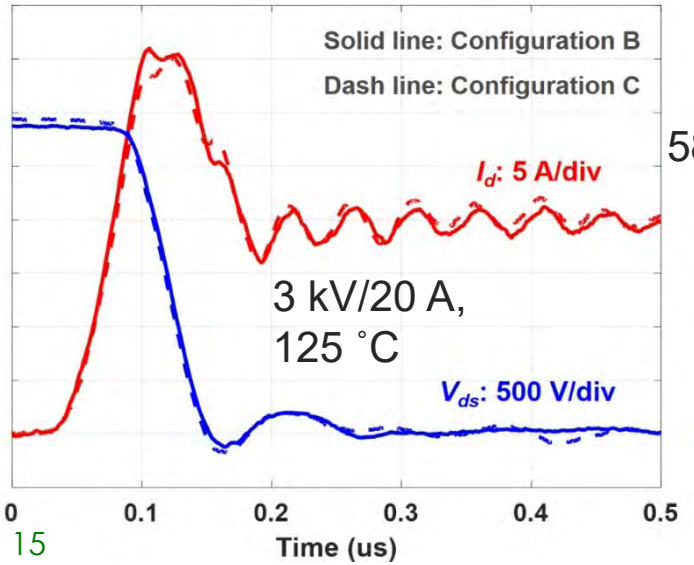
- Three device configuration compared
- Configuration A and B have nearly the same switching performance
- Body diode: negligible reverse recovery
- Like JBS diode, body diode has negligible reverse recovery
- Origin of negligible reverse recovery: negligible minority carrier injection

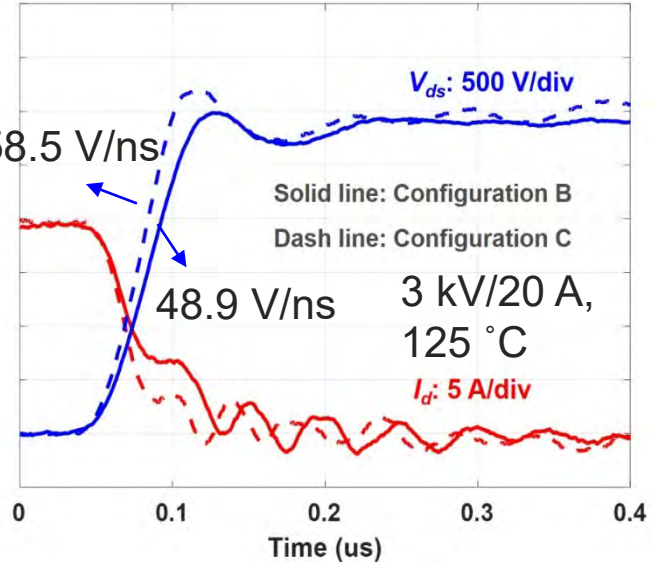


In red: freewheeling diode in the device configuration





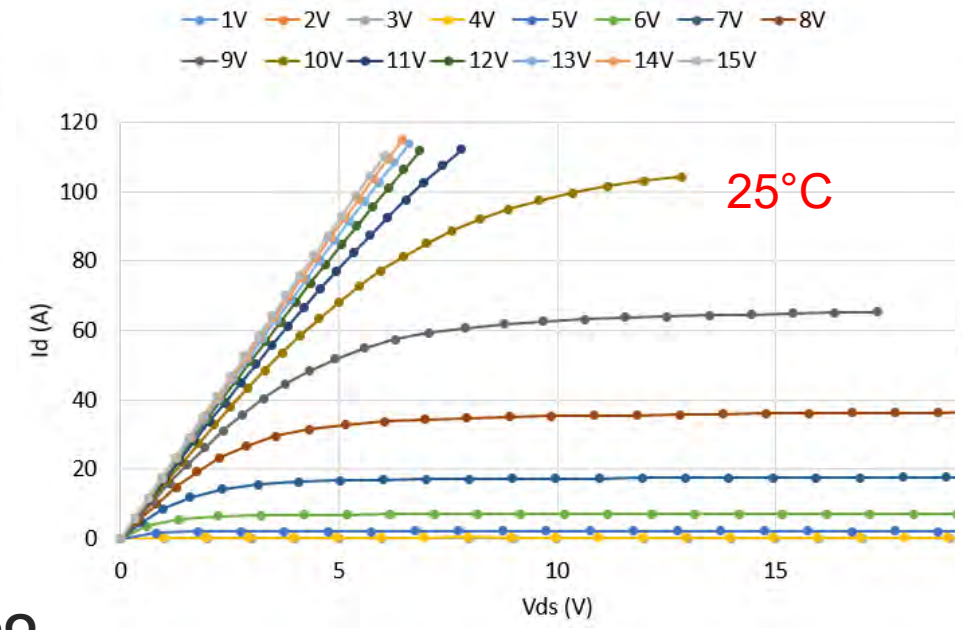


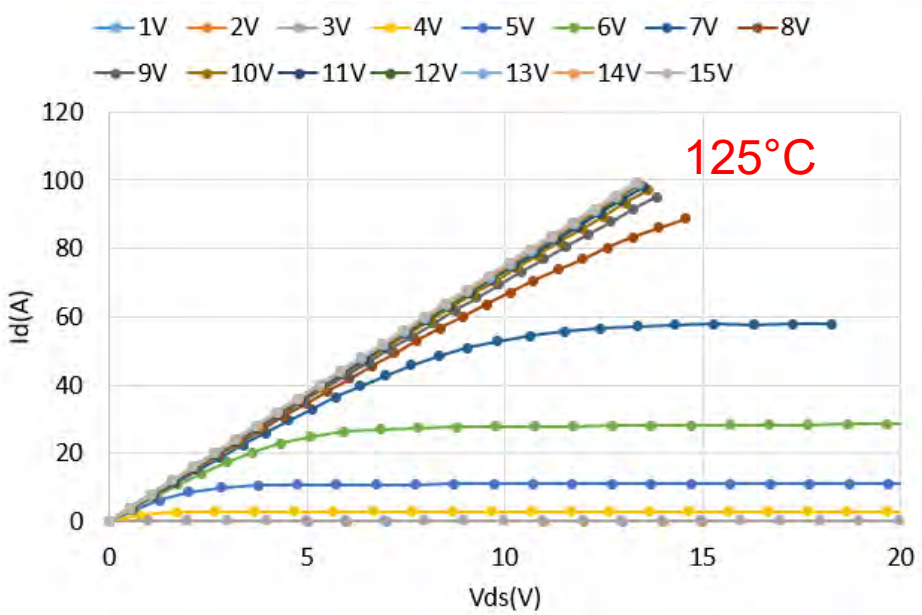


10 kV SiC MOSFET XHV-9 Module

❑Static Characteristics

Wolfspeed 10 kV/50 mΩ SiC MOSFET (XHV-9 Module)

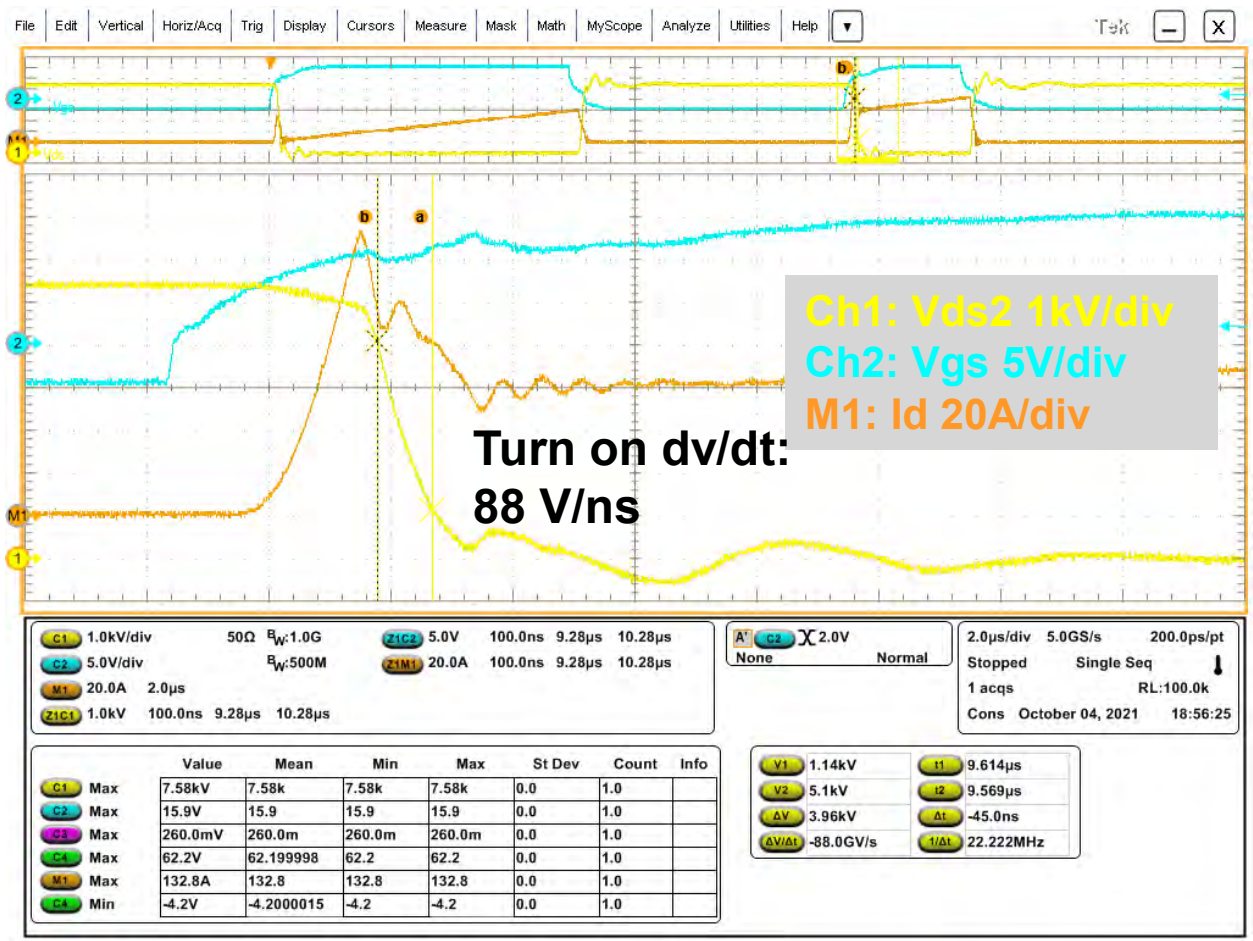


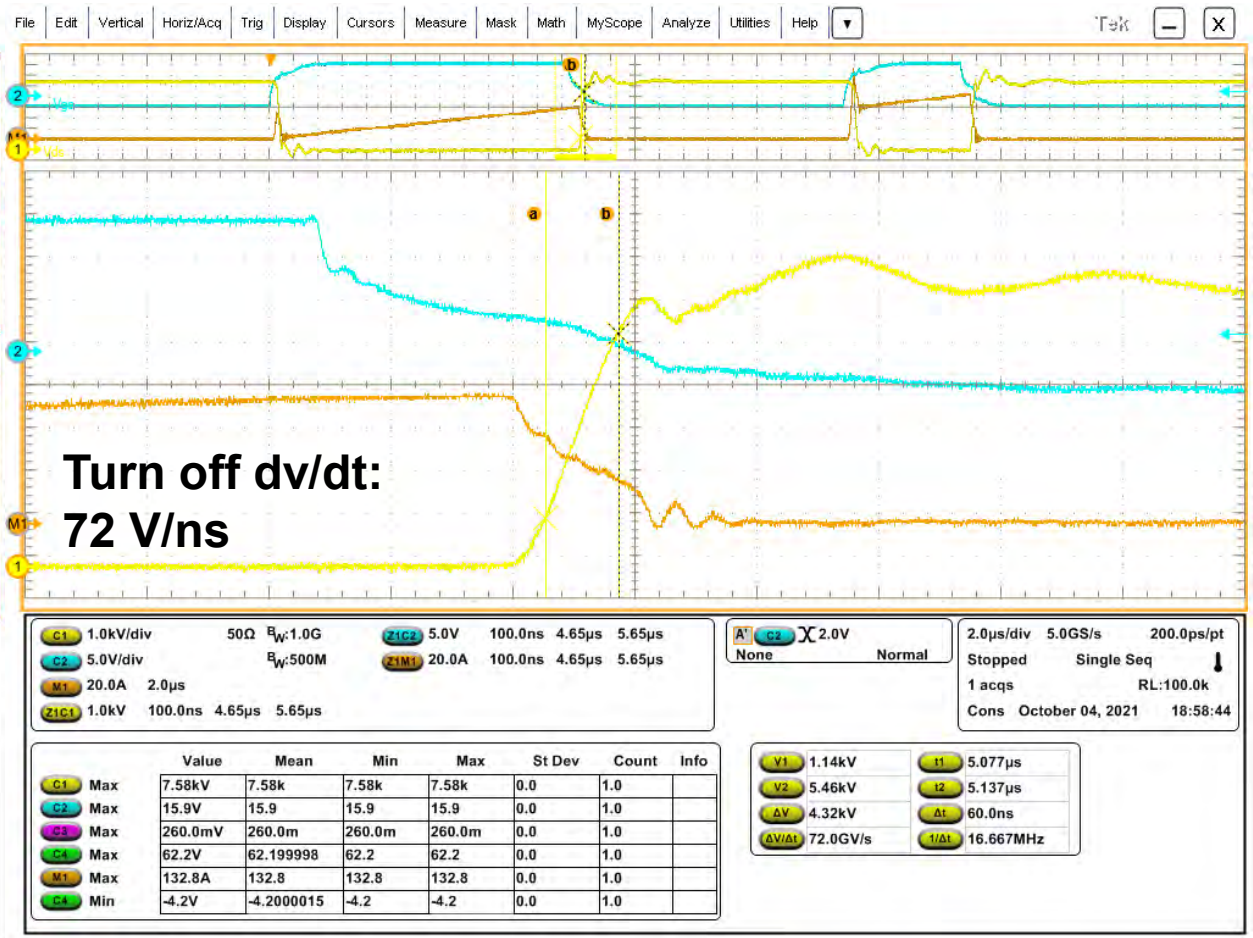


forward conduction curve

10 kV SiC MOSFET XHV-9 Module

❑Dynamic Characteristics





DPT at 6.5 kV-60A condition @25°C (with 2 Ohm gate resistance)

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Gate Drive Design and Protection

❑Design Considerations

- Main consideration and challenge: realize fast switching speed and robust continuous operation with **6.5 kV insulation voltage** and ***dv/dt* up to 100 V/ns**

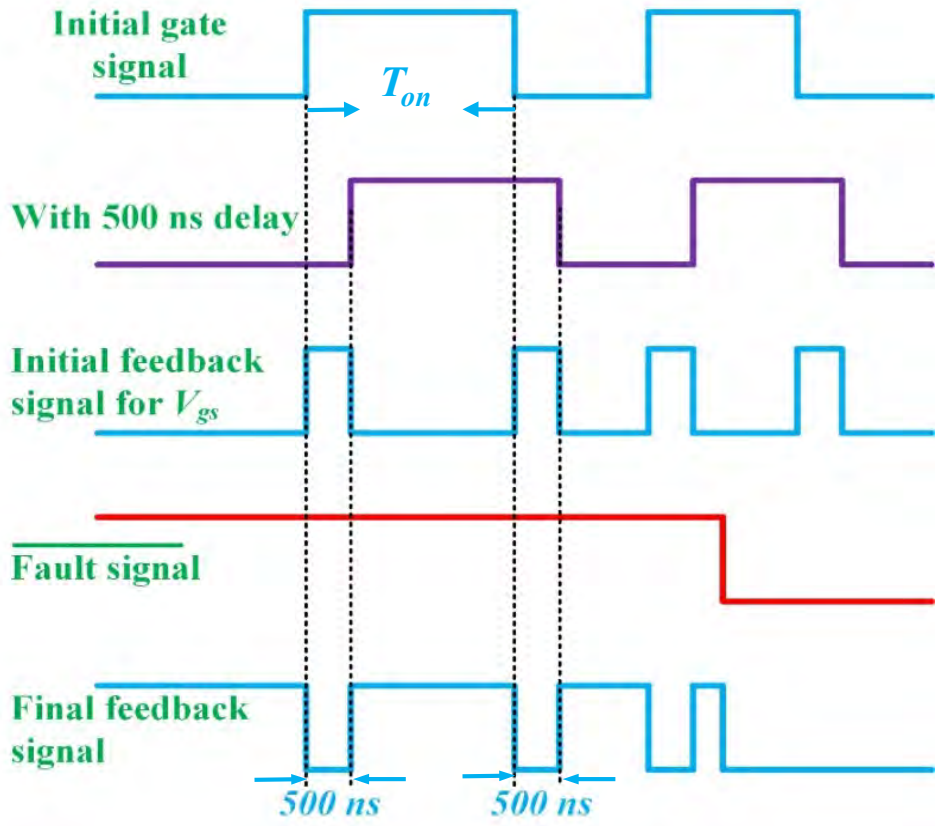
Specification	Target	Design result
Driving voltage	Maximum: +20 V; Minimum: -5 V	-5 V for off state; 15 V for on state
Peak driving current	> 8 A	9 A
Rise and fall times	< 30 ns	22 ns rise time; 15 ns fall time
Short circuit protection	< 1.5 us response time	< 1.3 us response time
Status feedback	Feedback signal sent back to controller in every switching cycle	Feedback signal generated for every rising or falling edge of gate signal
Dead time insertion	Dead time realized with hardware	500 ns dead time realized in the gate drive

Gate Drive Design and Protection

❑Power Stage and Signal Feedback

- **Power stage**
  - Driving voltage: 15 V/-5 V;
  - Gate resistance: 15 Ω for turn-on; 3 Ω for turn-off
  - Anti-cross-talk circuitry not needed since the 10 kV/20 A SiC MOSFET has much larger C_{gs}/C_{gd} than 1.2 kV SiC MOSFETs

- **Signal feedback to the controller**
  - Status feedback to monitor communication and gate driver
  - Acknowledge every rising or falling edge with 500 ns LOW signal
  - Report the fault once the overcurrent protection is triggered

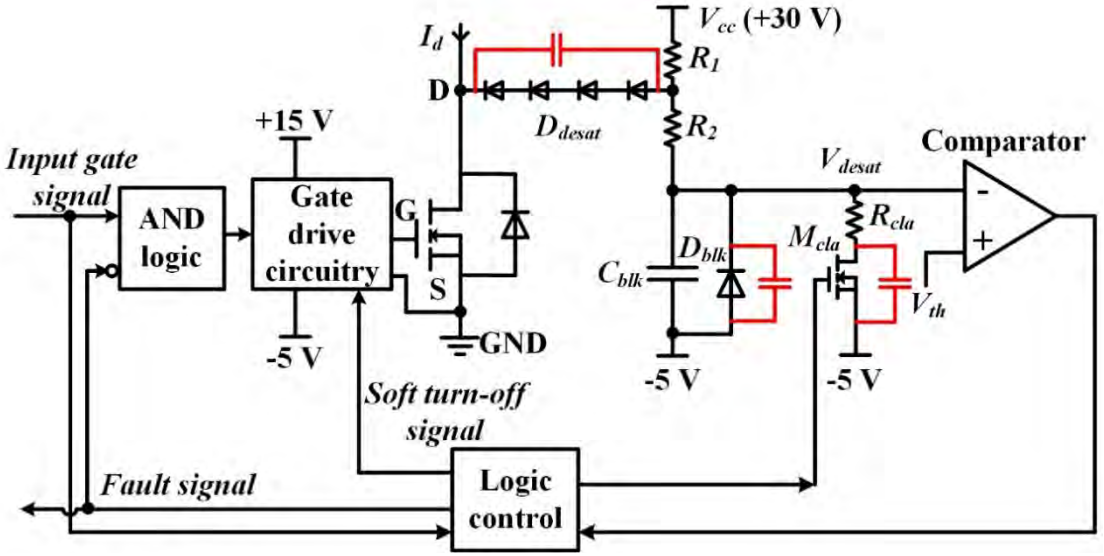


Generation scheme of final feedback signal

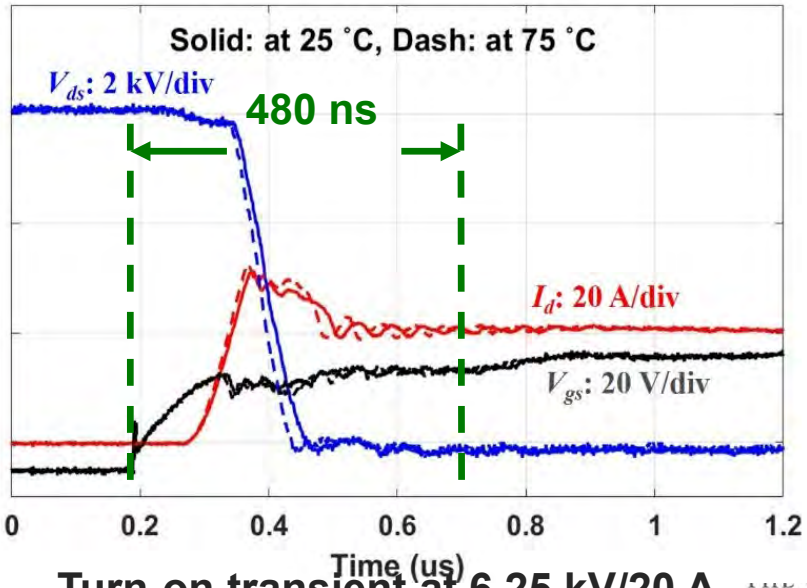
Gate Driver Design and Protection

❑Desat Protection

- Desat diode: four 3.3 kV SiC diodes in series to withstand the high voltage and achieve small parasitic capacitance
- Clamp V_{desat} at -5 V in off state to avoid false triggering during turn-off transient
- Blanking time: 1.22 us (requirements: >550 ns considering noise immunity, and <1.5 us considering device capability)
- Protection threshold value: 20 A at 125 ˚C; 42.85 A at 25 ˚C



Desat protection circuitry scheme

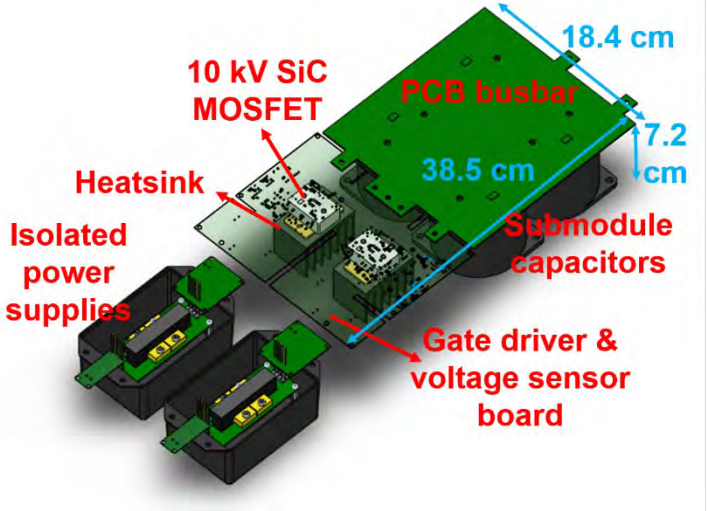


Turn-on transient at 6.25 kV/20 A

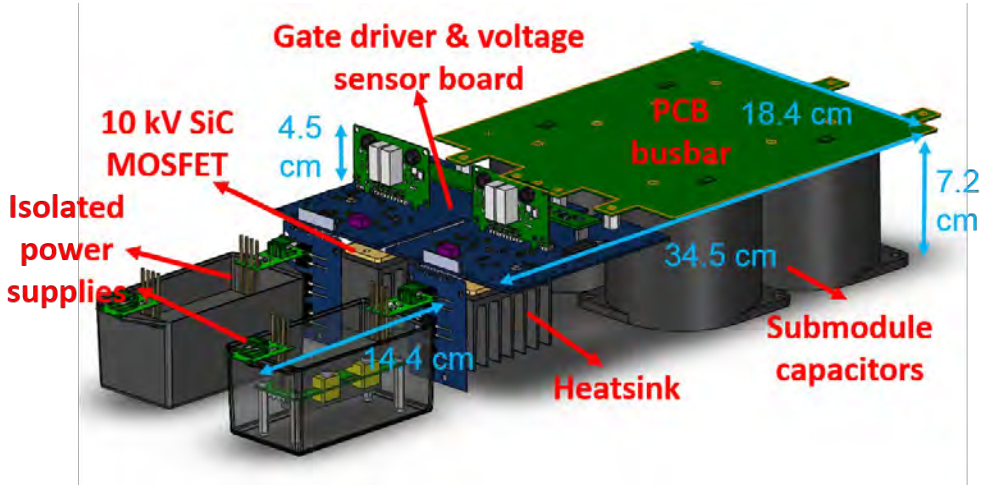
Gate Driver Design and Protection

❑MMC Submodule

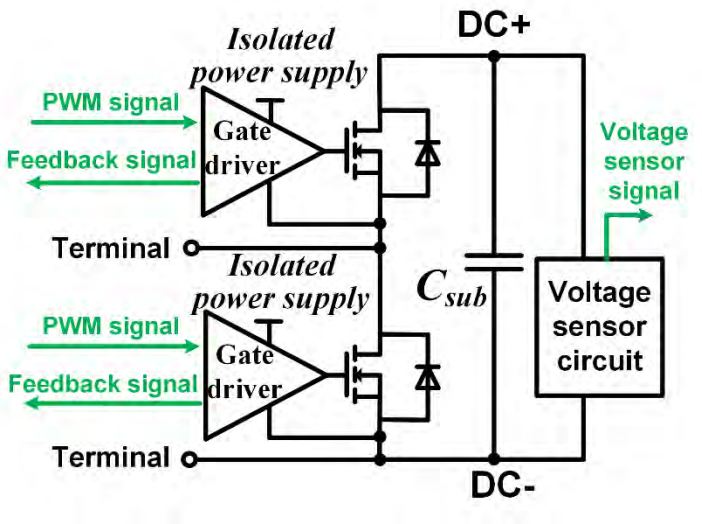
- Half bridge topology: two 10 kV/20 A SiC MOSFETs
- Key components: gate driver, isolated power supply, voltage sensor, etc
- Two iterations: submodule v2.0 is more compact, modular, and robust
- Insulation design
  - Clearance requirements in IPC-2221B followed
  - Creepage requirements in UL60950-1 followed



MMC submodule v1.0



MMC submodule v2.0

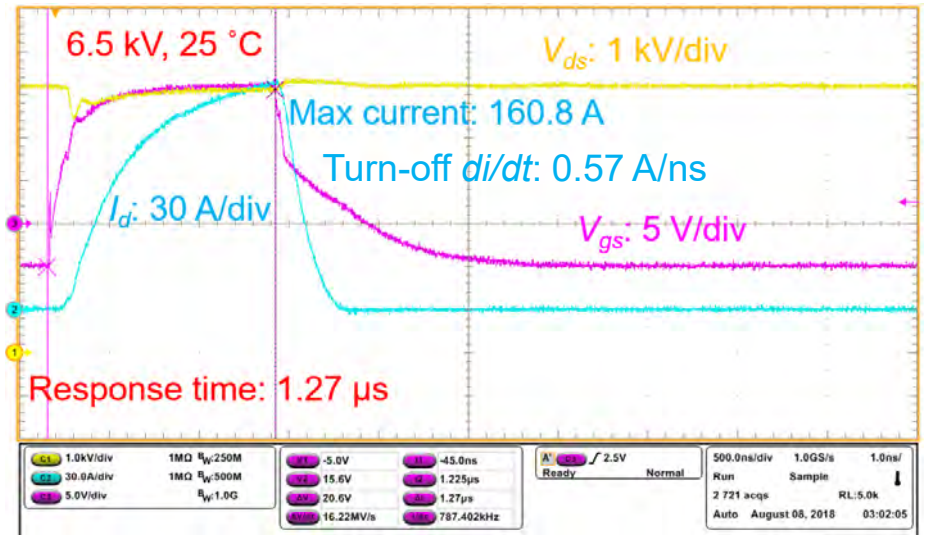


Architecture of MMC submodule

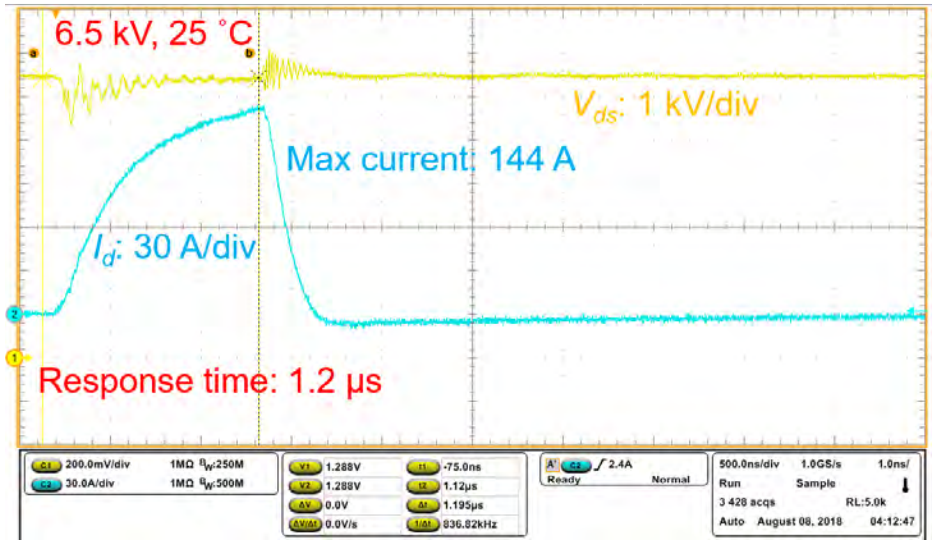
Gate Driver Design and Protection

❑Short Circuit Test

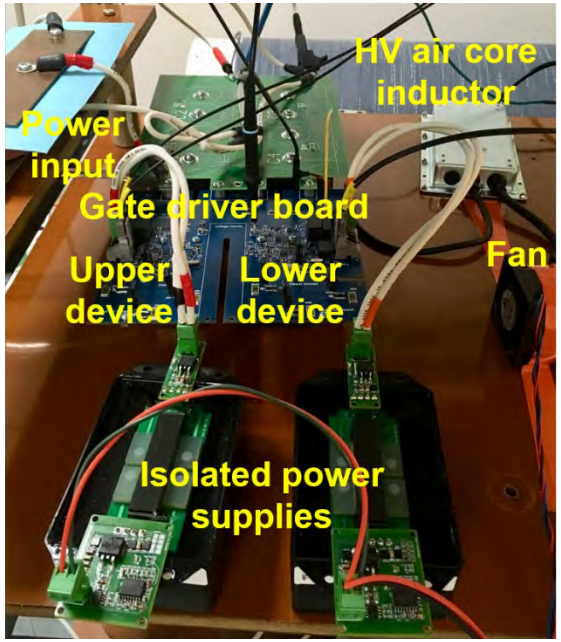
- **Hard switching fault (HSF) short circuit test**
  - Worse case for desat protection in terms of response time, compared to fault under load (FUL) short circuit fault
  - All protection specifications met at DC-link voltage up to 6.5 kV



HSF test of lower MOSFET



HSF test of upper MOSFET

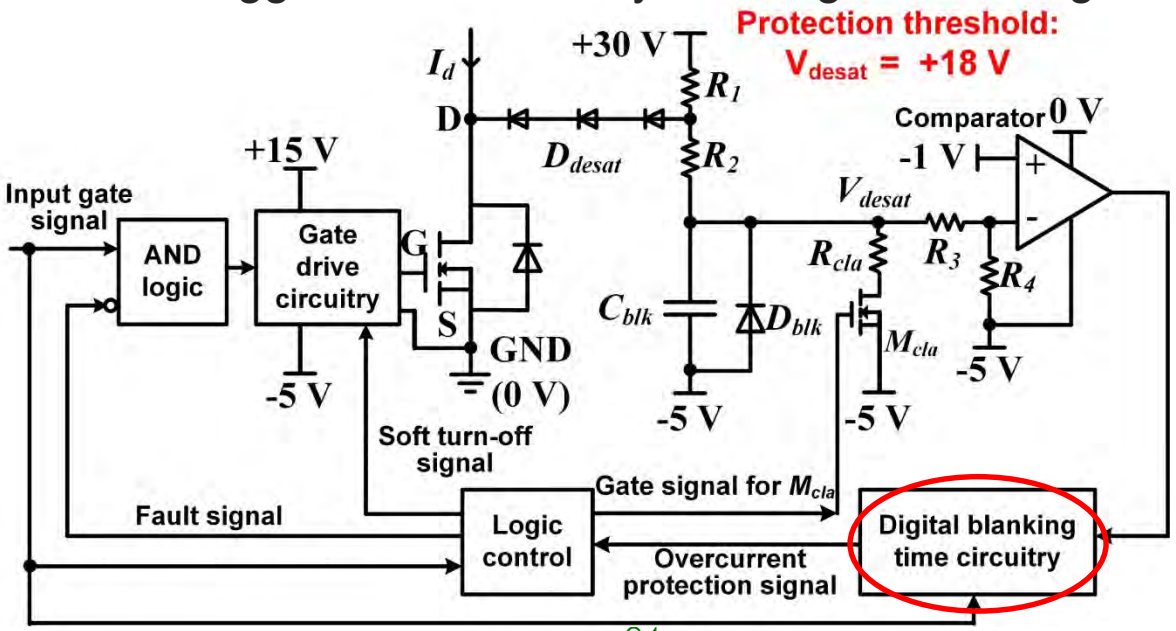


Short circuit inductance: 1.22 µH

Gate Driver Design and Protection

❑Improved Desat Protection

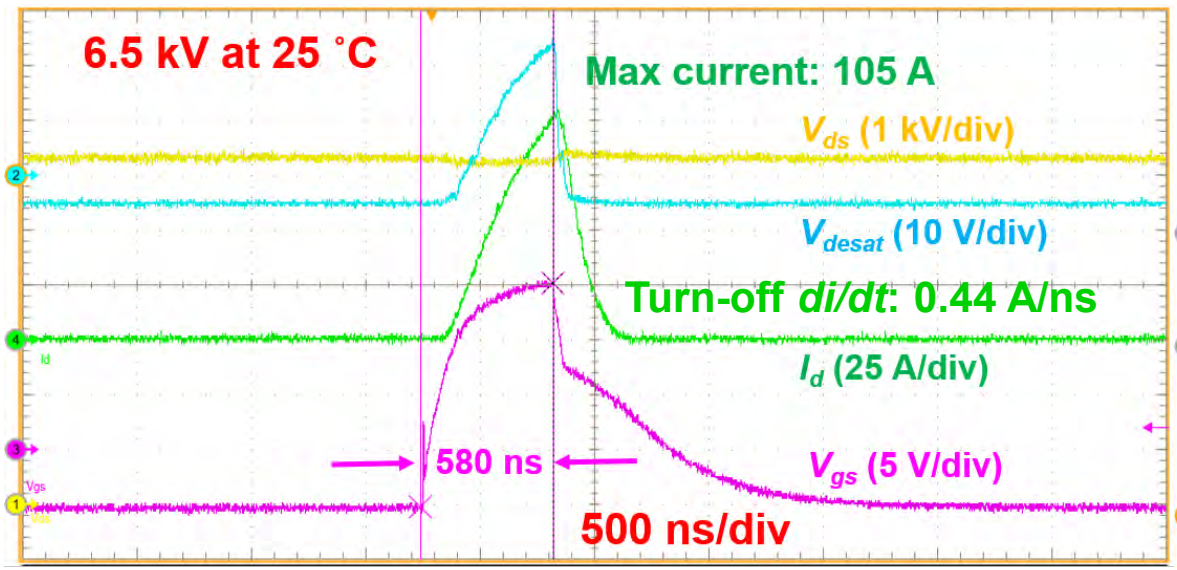
- Fundamental idea the same as the conventional desat protection
- 550 ns blanking time required to avoid false triggering
- 600 ns blanking time realized by digital ICs, instead of a large blanking capacitor Cblk
- 600 ns digital blanking time; Cblk independent of blanking time
- R1 reduced from 6.49 kΩ to 3.25 kΩ; Cblk reduced from 75 pF to 12 pF
- FUL fault: much short response time can be achieved
- HSF fault: protection triggered immediately after digital blanking time expires



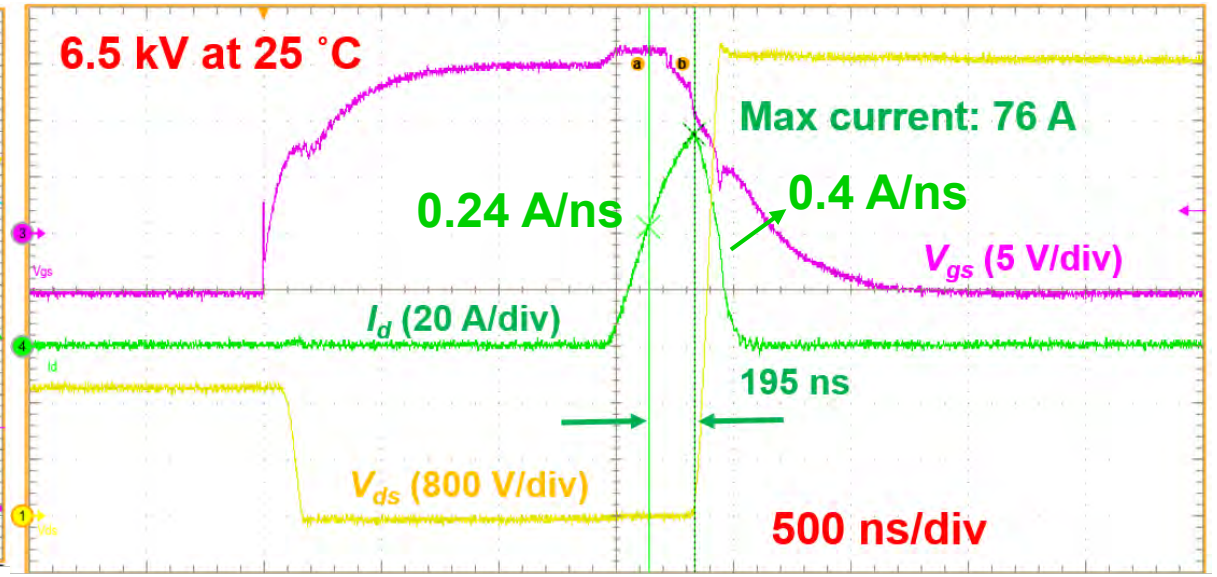
Gate Driver Design and Protection

❑Short Circuit Test with the Improved Desat Protection

- Short circuit inductance under HSF fault: 171 nH
- Measured digital blanking time: 580 ns
- Response time under HSF fault: 340 ns
- Response time under FUL fault: 195 ns



HSF fault



FUL fault

Response time measured based on 42.5 A threshold current of overcurrent protection

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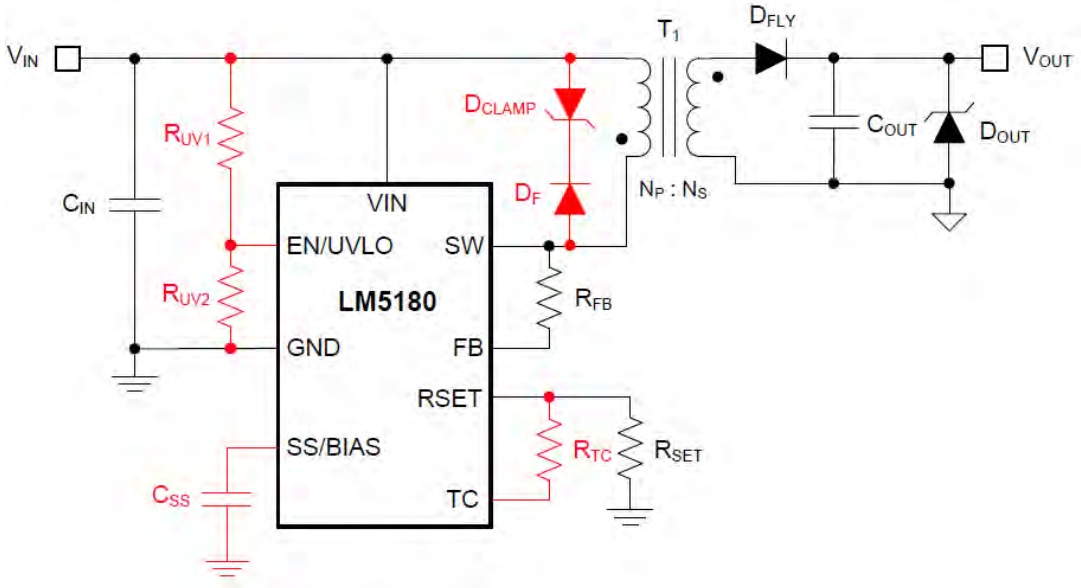
High Voltage Isolated Power Supply

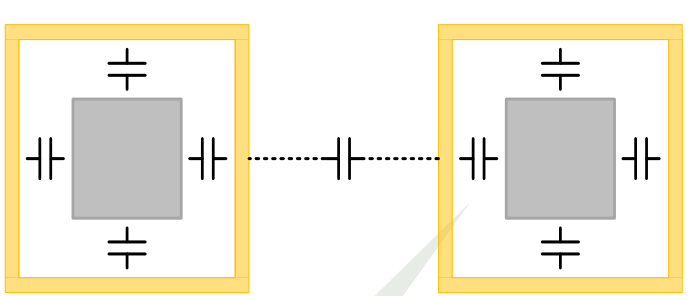
❑Topology

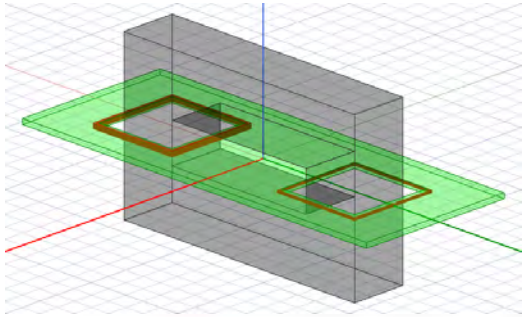
- PSR Flyback DC/DC converter
- Eliminate the need for a third winding for output voltage regulation
- UVLO, primary OCP, and thermal protection are integrated

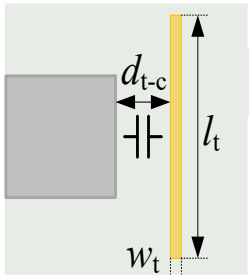


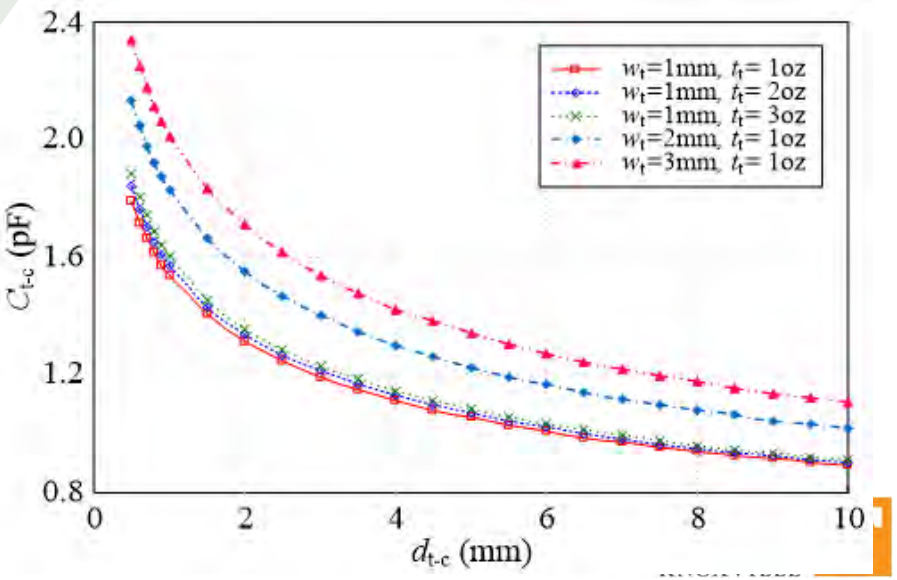
❑Low-Interwinding Capacitance Design

- Reduce the trace's width-to-thickness ratio
- Choose the optimal winding-to-core distance
- Reduce winding turns





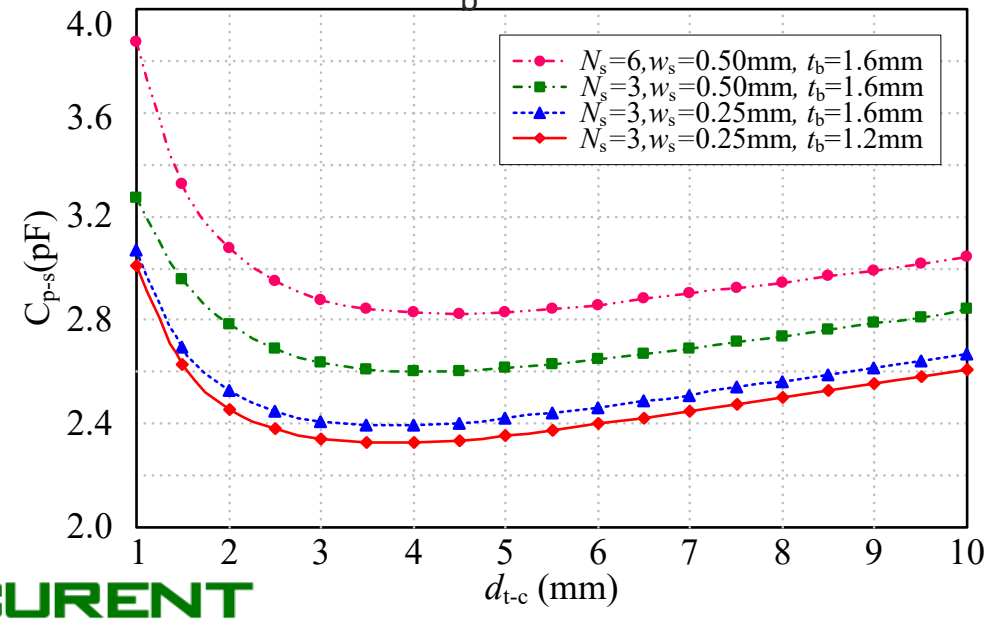




High Voltage Isolated Power Supply

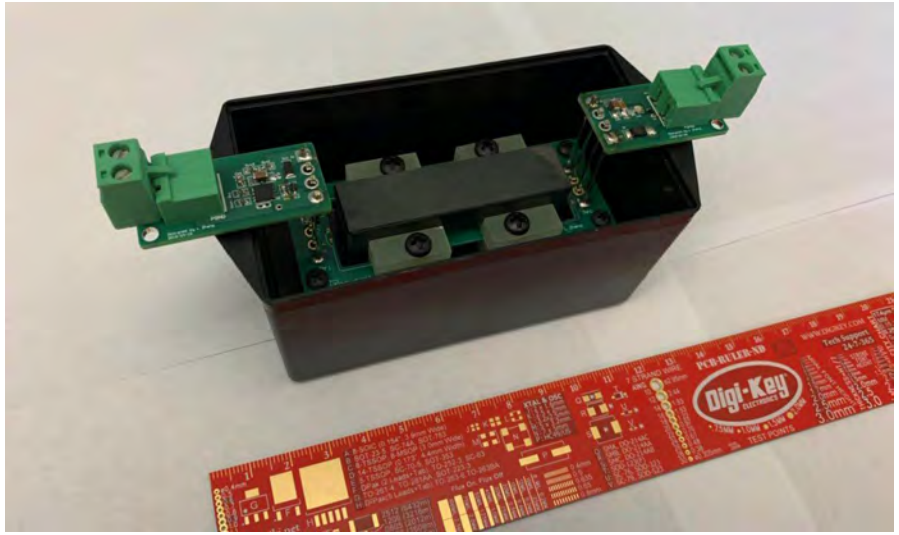
❑ HV Isolated Transformer Design

- High insulation capability
- Low coupling capacitance
- High *dv/dt* immunity
- Primary Turns N_P = 6; Secondary Turns N_S= 3
- Primary Winding Width = 0.50 mm
- Secondary Winding Width w_s = 0.25 mm
- Board thickness t_b=1.2mm



❑ Designed Power Supply

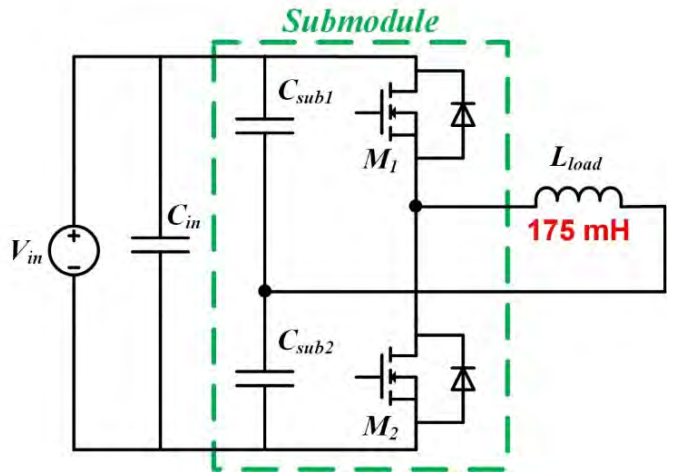
- High efficiency over a wide range (up to 80%)
- precise output voltage control (no-load: 24.08V; full load: 24.00V)
- ~1.85 pF parasitic capacitance
- >15 kV RMS partial discharge inception voltage



Submodule Continuous Test

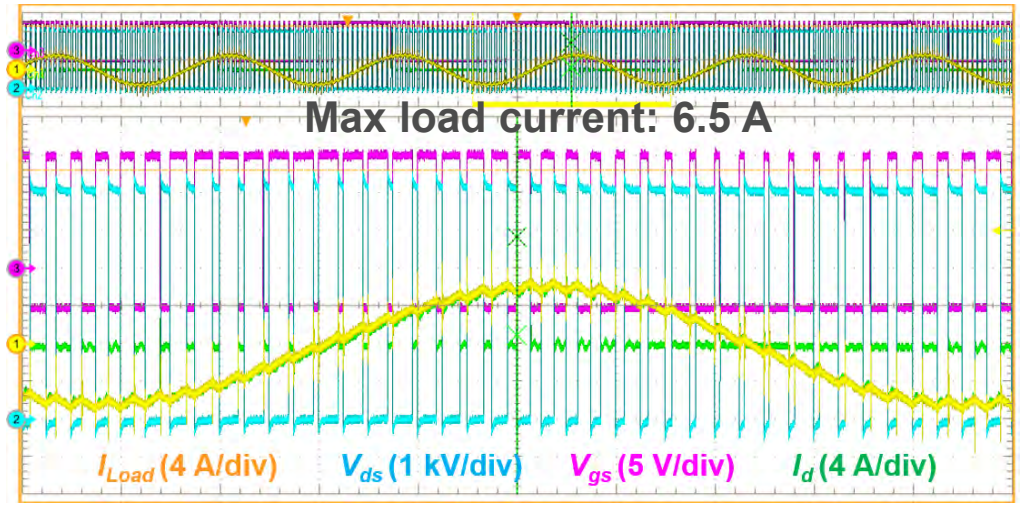
❑AC-DC Continuous Test

- Bipolar PWM modulation (modulation index: m)
- Fundamental frequency f_{line}: 300 Hz
- Switching frequency: 10 kHz
- Rated peak current of load inductor: 9 A
- Successful operation at 6.5 kV DC bus voltage

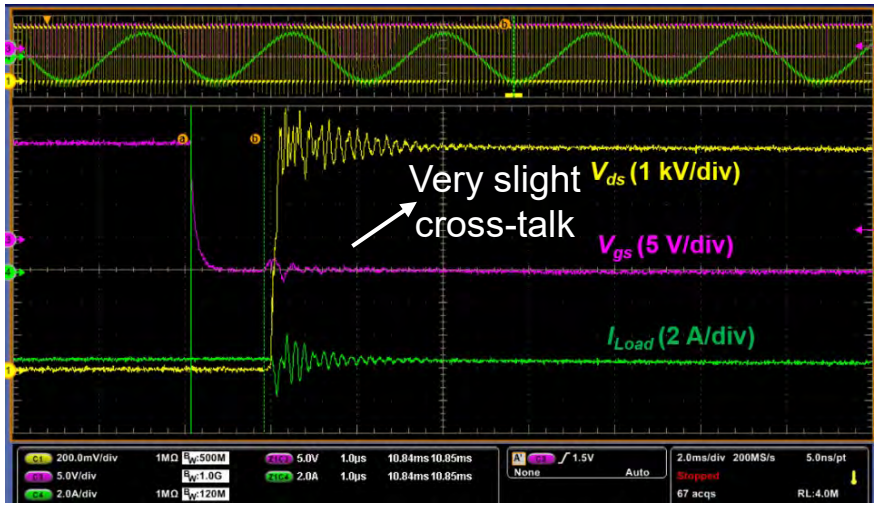


Peak AC load current:

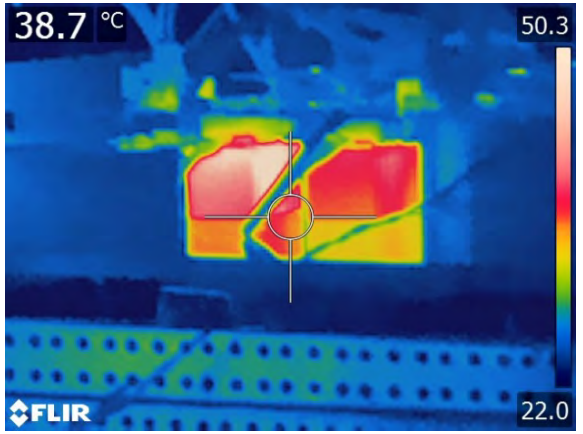
$$I_{out} = \frac{0.5mV_{in}}{2\pi f_{line} L_{load}}$$



Continuous test at 6 kV



Continuous test at 6.5 kV



Thermal image

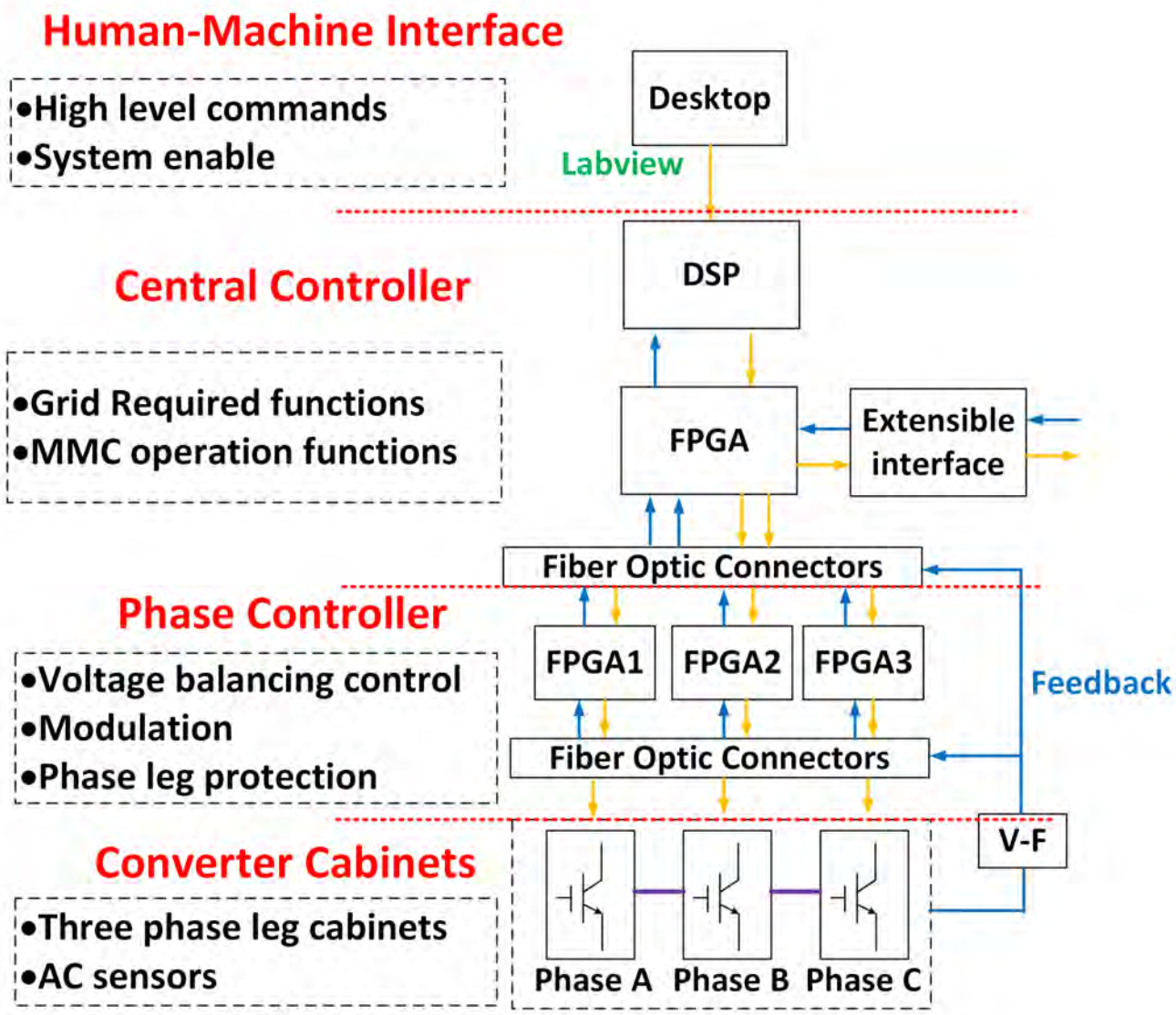
PCS Development Outline

- Background
- 10 kV Device Characterization
- Driving and Protection
- Isolated Power Supply
- **Control**
- PCS Design and Testing
- Grid Supporting Function and Validation

Control

❑MMC-based PCS Control Structure

- The controller design follows IEEE standard 1676-2010.
- Modular design approach is applied
- Fiber-optic cables are used to link controllers and submodules to improve the noise immunity capability and support medium voltage operation
- Extensible interface board is designed for future full PCS back-to-back operation.



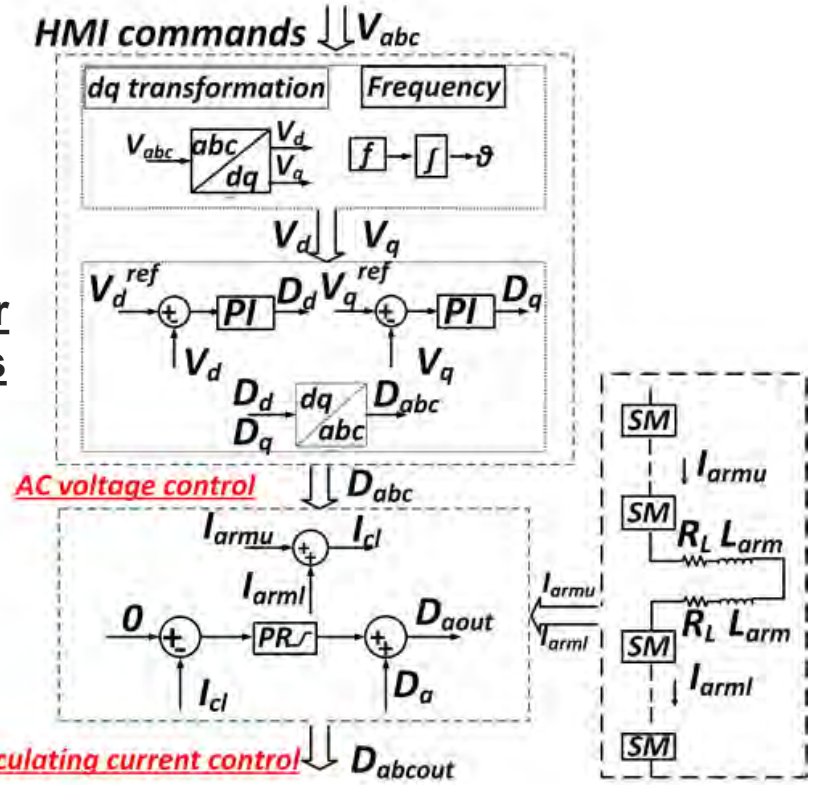
PCS control architecture design

Control

❑Central Controller

- Receive commands (start/stop) from HMI
- Execute grid functions, such as microgrid voltage and frequency regulation, and MMC operation functions: 2nd-order circulating current control)

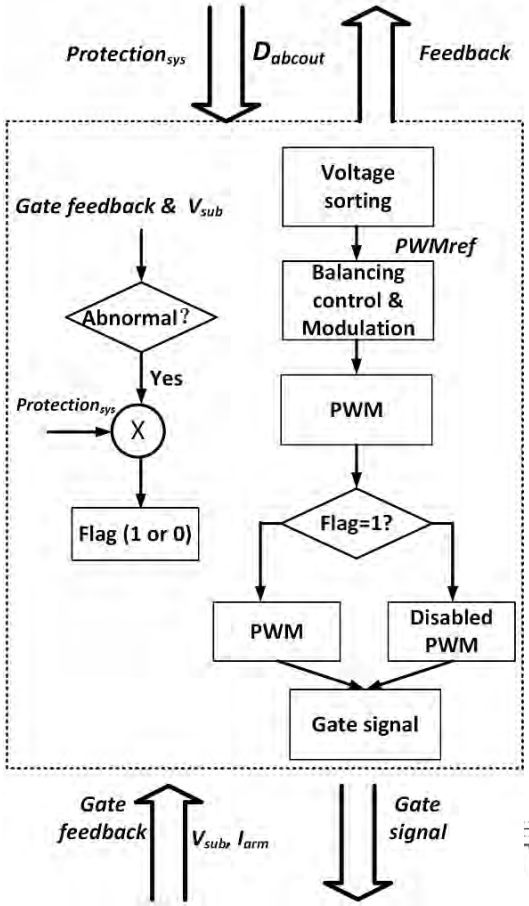
Central controller functions



❑Phase Controller

- PWM modulation and voltage balancing control
- Monitor gate drive operation signals and execute protection

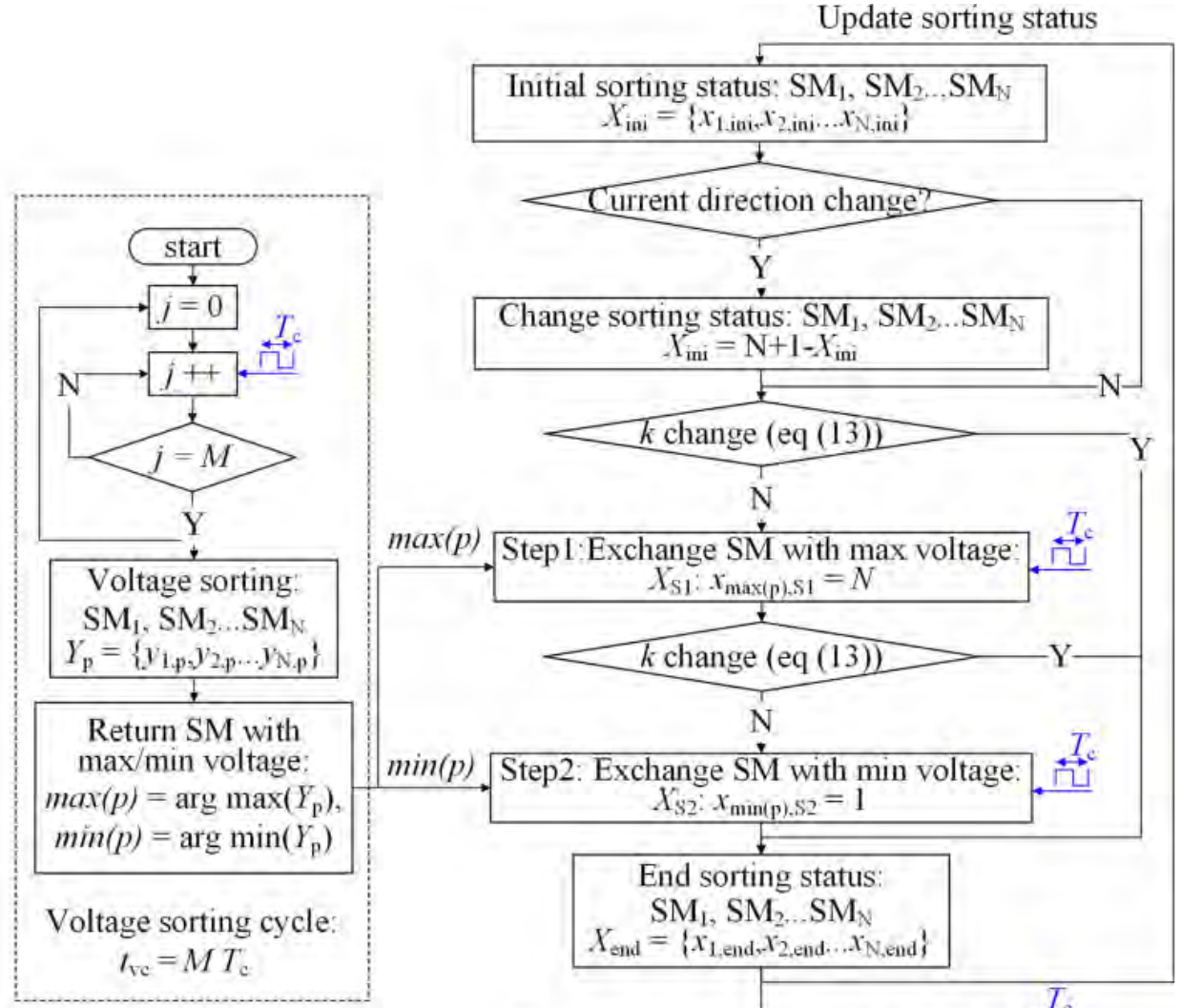
Phase controller functions



Control

❑Modulation for dv/dt Reduction

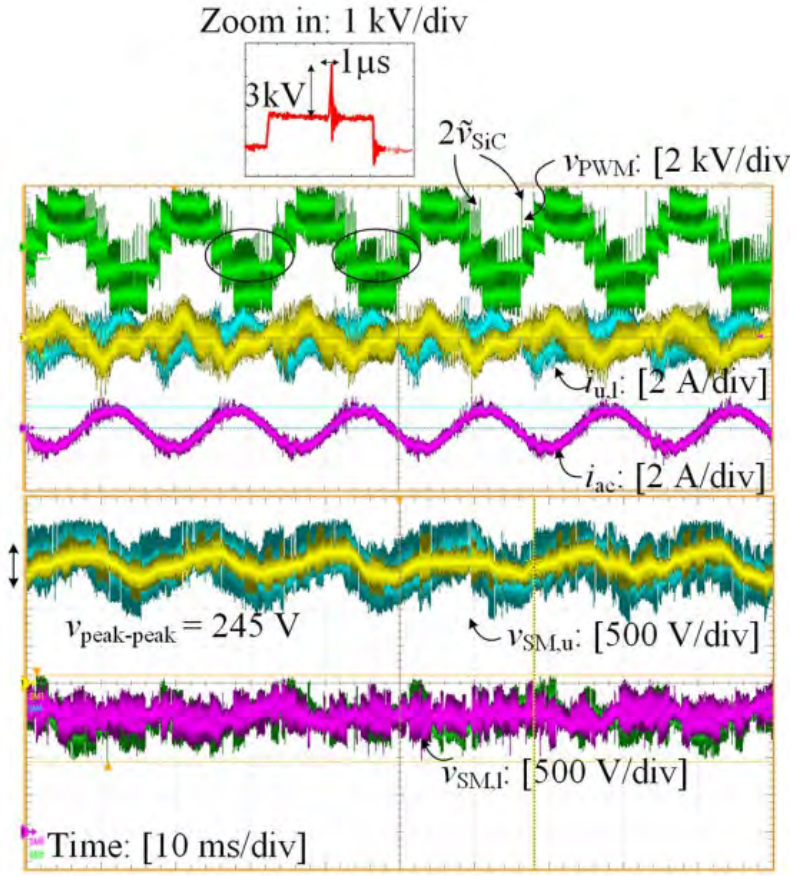
- A modified nearest-level PWM is applied for the modulation and voltage balancing control
- Each submodule has three modes:
  - Inserted mode
  - Bypassed mode
  - PWM mode
- **Only two submodules switch modes in a control cycle for dv/dt reduction**



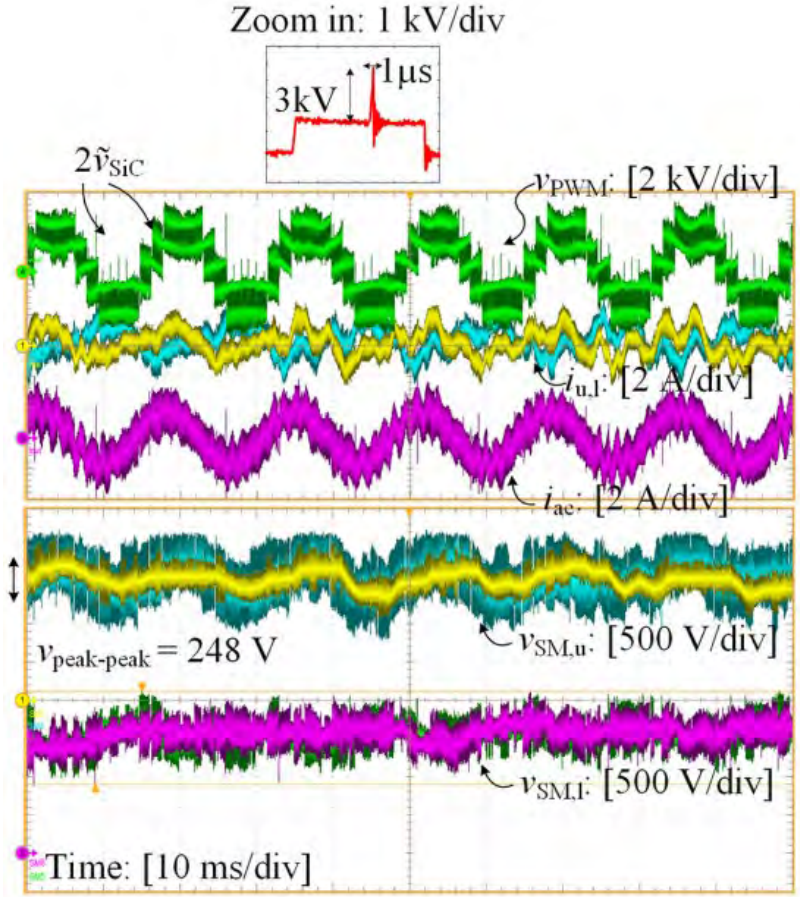
Modulation strategy

Control

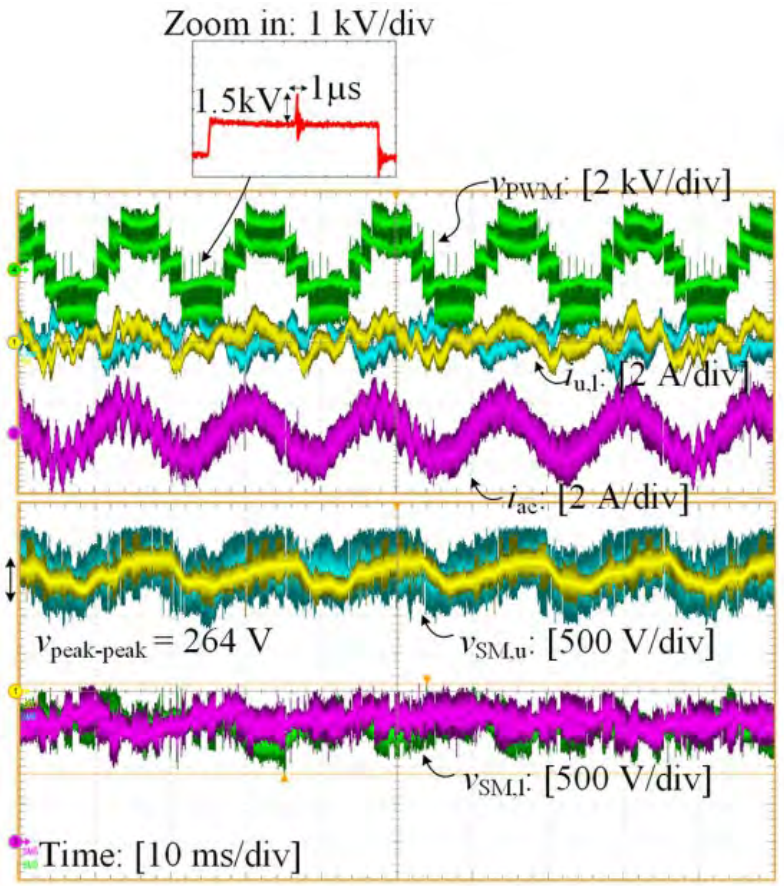
- Dv/dt Reduction Validation (6 kV DC-link voltage)



Carrier-phase-shifted pulsewidth modulation (3kV/μs)



Nearest-level modulation (3kV/μs)



Proposed modulation (1.5 kV/μs)

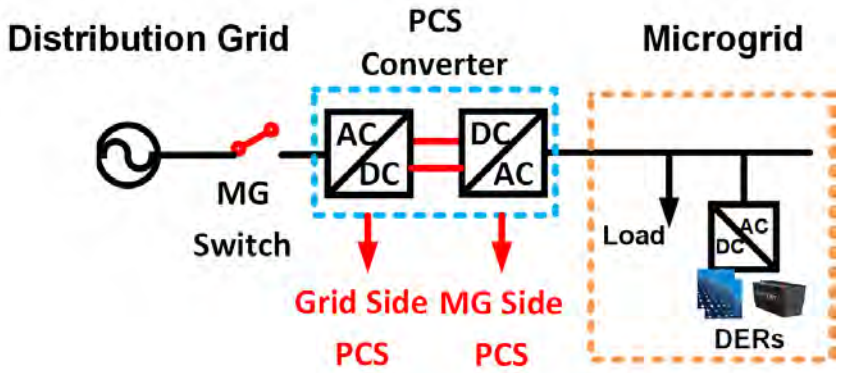
PCS Development Outline

- Background
- 10 kV Device Characterization
- Driving and Protection
- Isolated Power Supply
- Control
- **PCS Design and Testing**
- Grid Supporting Function and Validation

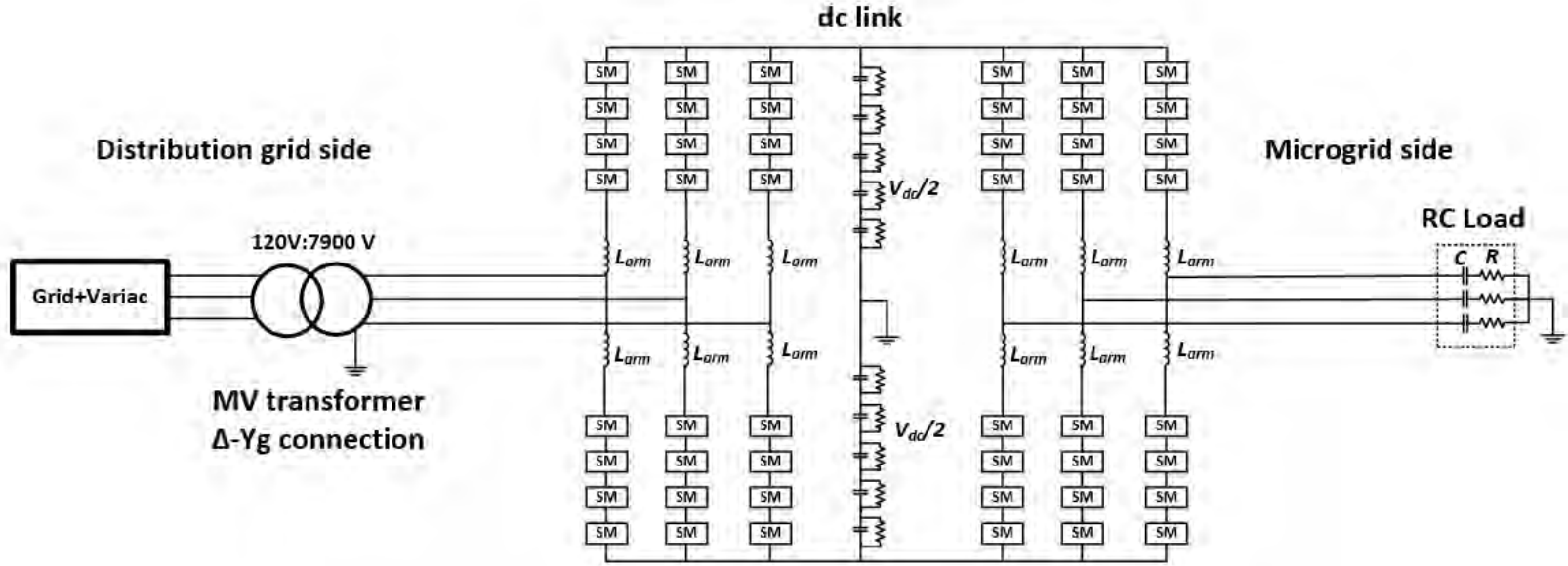
ASMG PCS Design and Testing

❑ ASMG PCS

- The overall objective is to develop an asynchronous microgrid (ASMG) PCS module employing 10 kV SiC MOSFETs with >10 kHz equivalent switching frequency to deliver at least 100 kVA power at a required ac voltage level of 13.8 kV, achieving the efficiency, density, and grid support functions.
- MMC topology based back-to-back PCS module interfacing distribution grid and asynchronous microgrid



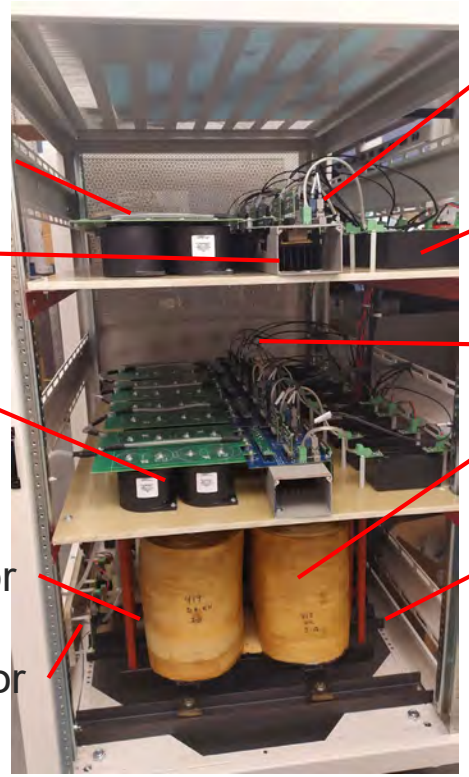
ASMG PCS



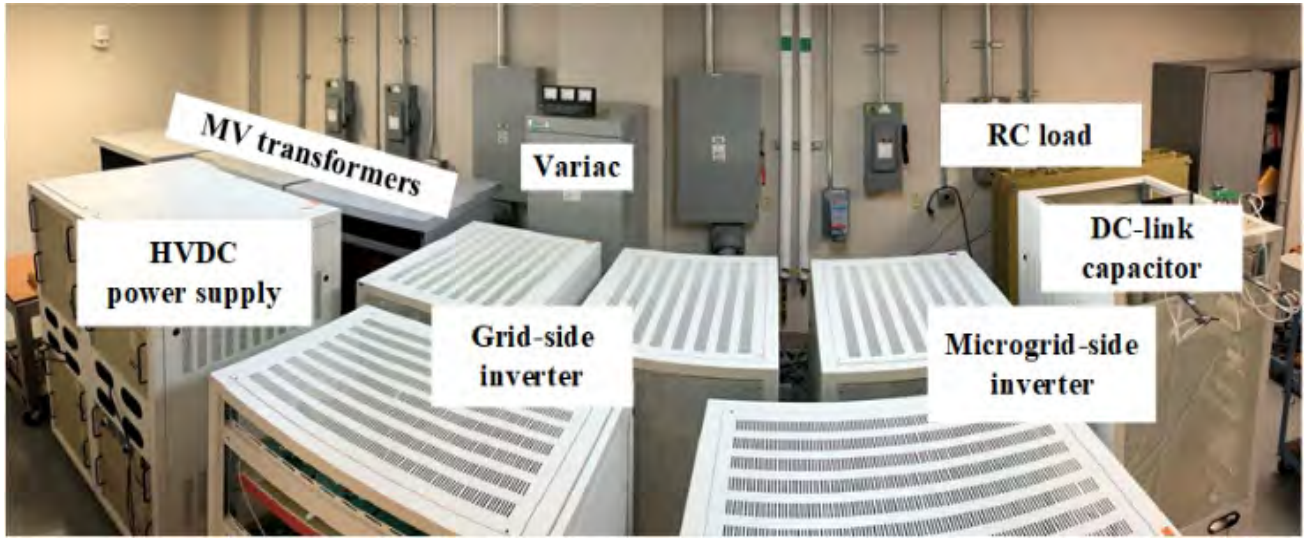
MMC based back-to-back PCS module test scheme

ASMG PCS Design and Testing

❑PCS Hardware and Test Setup



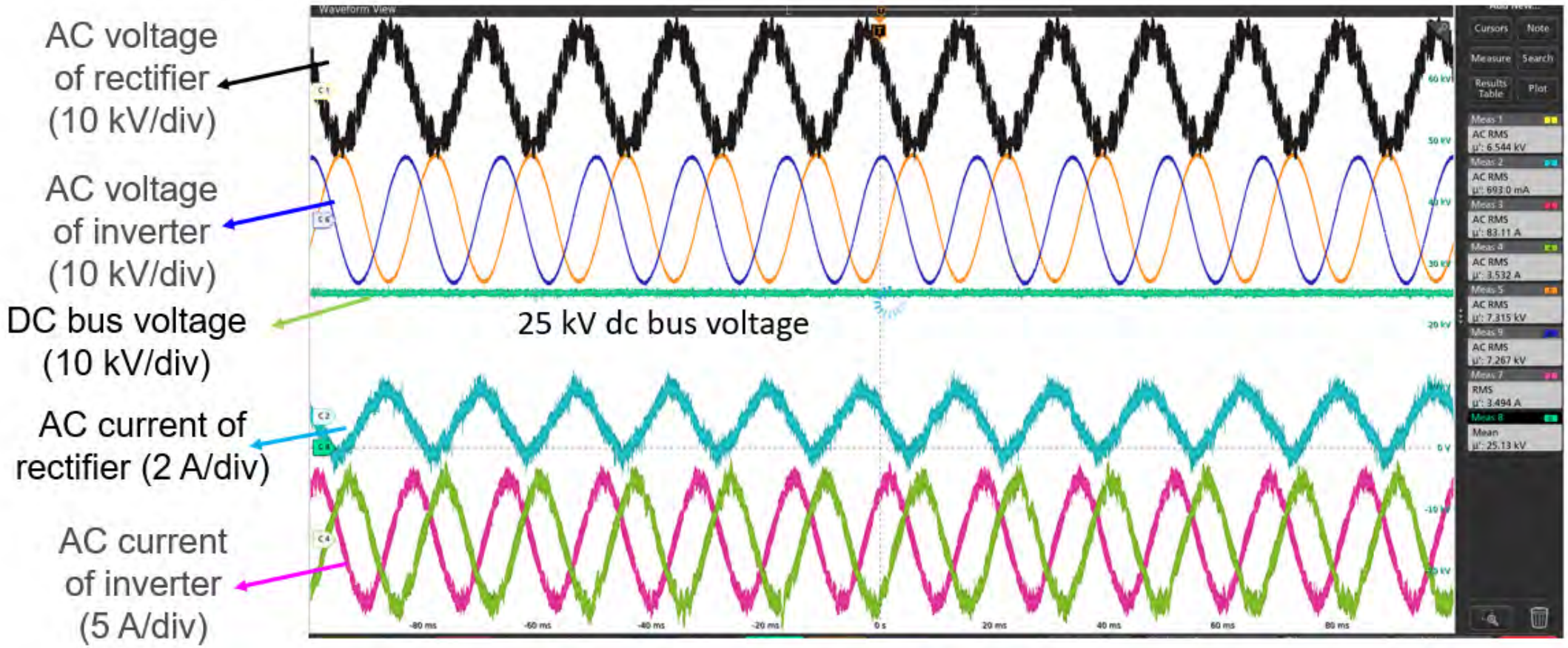
One phase-leg cabinet



Test set-up of the back-to-back PCS module

ASMG PCS Design and Testing

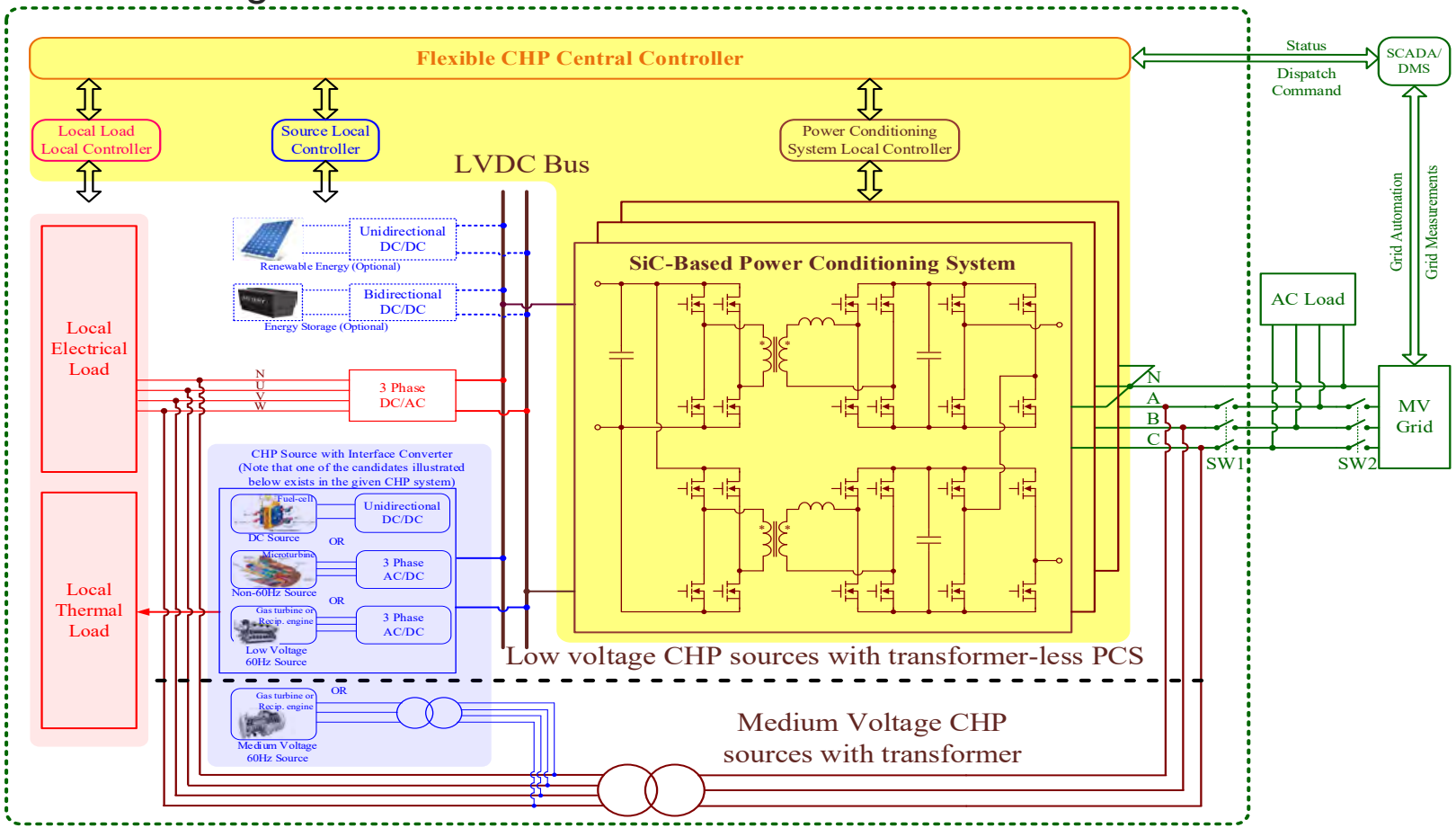
- Full power test of the PCS module
  - Operation of back-to-back PCS module successfully achieved at 25 kV DC bus voltage
  - Control implemented to suppress 180 Hz common mode current



F-CHP PCS Design and Testing

❑The Flexible CHP (F-CHP) System Configuration

- Enabled by power electronics converters, aims at providing cost-effective dispatchable generation and flexible grid support services, benefiting both the grid and the F-CHP system owner
- Two operation modes: grid-connected mode and islanded mode



F-CHP PCS Design and Testing

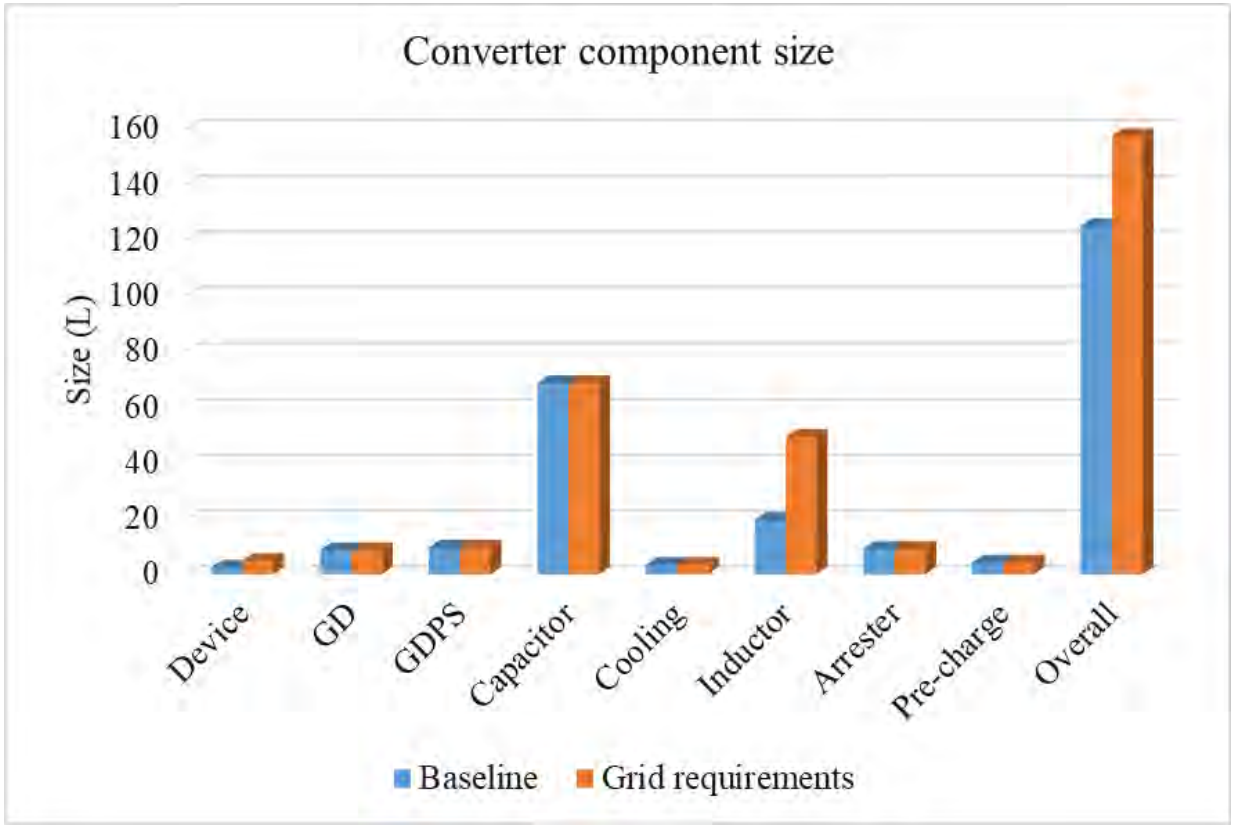
❑Converter Design Considering Grid Requirements

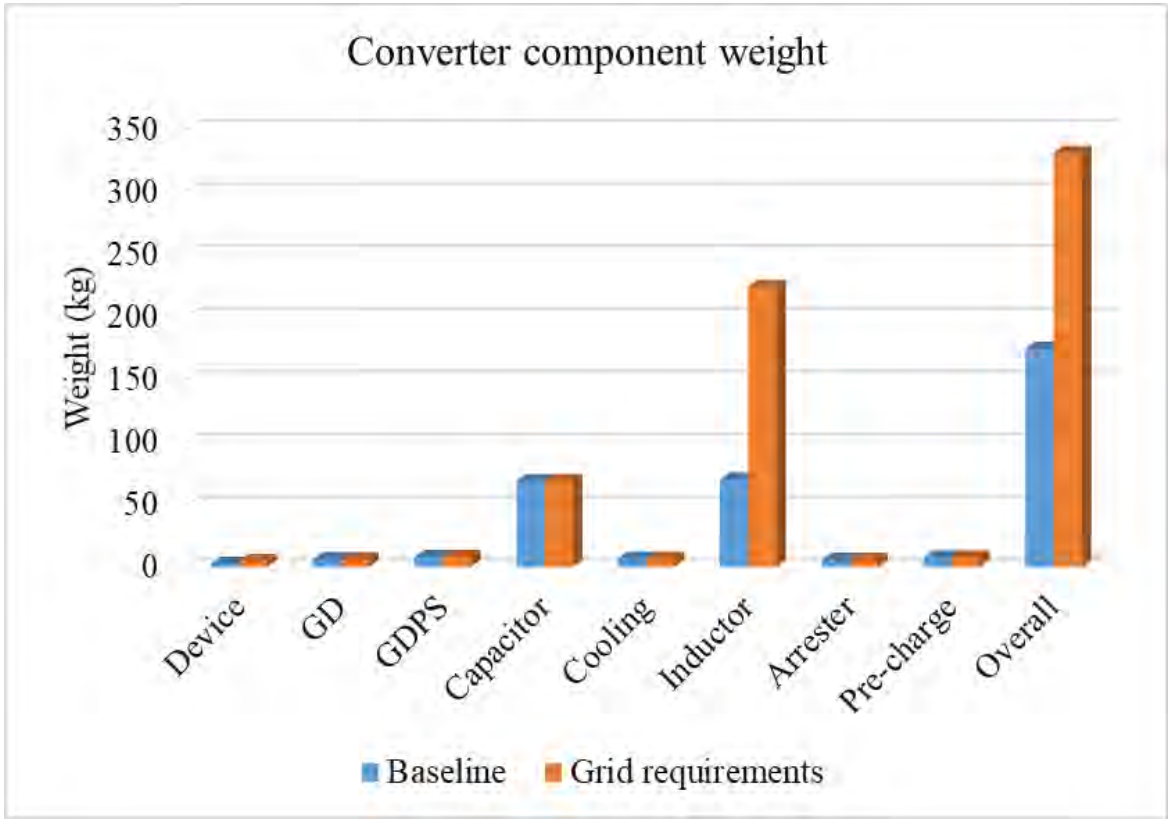
Requirements	Requirement details	Impact on converter design
Voltage ride through	▪ Ride through low voltage down to 0 and high voltage up to 1.2 p.u.	▪ Inrush current, which can be effectively limited by the PWM mask function, e.g., 2 p.u. ▪ The MV dc-link voltages increase to 6.67 kV to accommodate the 1.2 p.u. ▪ Power control coordination between the dc/dc stage and the dc/ac stage and between the PCS converter and other resources on the LV dc bus
Grid faults	▪ Follow VRT if the voltage is lower than 1.2 p.u. ▪ If the voltage is higher than 1.2 p.u., temporarily stop working, and fully back to online in 3 s when the grid voltage is recovered	▪ Inrush current, up to 5 p.u., and DC-link overvoltage, up to 9.3 kV ▪ Extra braking circuit, to reduce the DC-link overvoltage to 8 kV during the fault period, and to quickly discharge the DC-link after the fault is clear to restart the converter within 1 s
Frequency ride through	▪ Ride through low frequency down to 50 Hz and high frequency up to 66 Hz	▪ No inrush and large DC-link overvoltage ▪ Need larger DC-link capacitance to limit the dc-link voltage ripple when operating at the lowest fundamental frequency
Grid voltage angle change	▪ Ride through 20 electrical degrees of positive-sequence phase angle change and up to 60 electrical degrees of individual phase angle change	▪ Inrush current exists due to the voltage suddenly changes, but can be effectively limited by the PWM mask function ▪ Dc-link voltage variation, but no need for hardware change
Lightning surge	▪ Keep operation	▪ Inrush current, up to 5 p.u. ▪ DC-link overvoltage, which is not too large thanks to the short period ▪ Converter internal component insulation need to consider the potential of the neutral point during the lightning transient

F-CHP PCS Design and Testing

❑Converter Design Considering Grid Requirements

- Compared to the size and weight of the baseline design, the converter size and weight increases around 26% and 90%,respectively, after considered the grid requirements





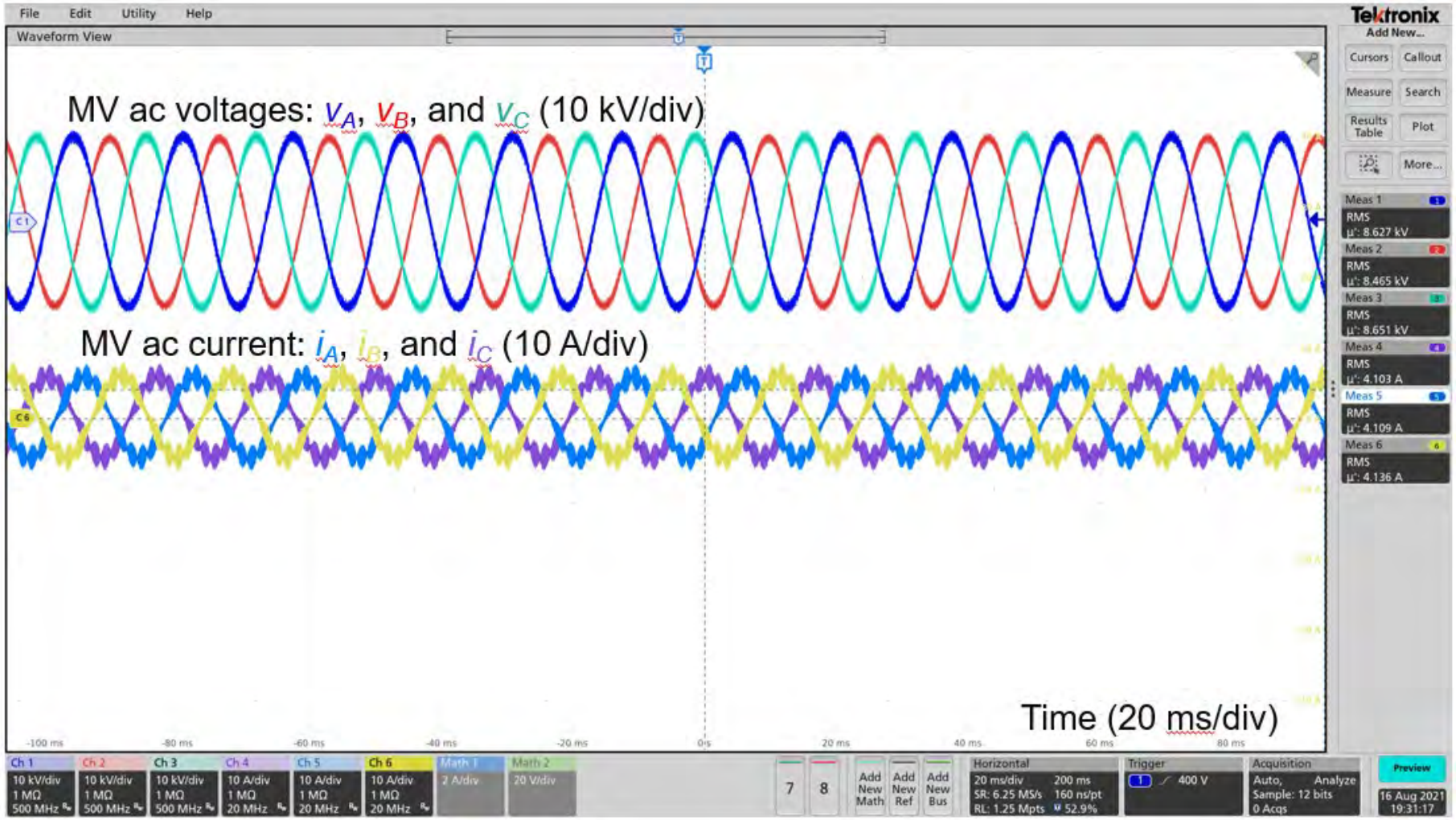
F-CHP PCS Design and Testing

- 13.8 kV/100 kW PCS Prototype for the F–CHP System

Three-phase PCS converter hardware pictures

F-CHP PCS Design and Testing

- Full Rating Test
  - **Line-to-line voltage:** 14.9 kV RMS (13.8 kV × 108%)
  - **Power:** 106 kVA



PCS Development Outline

- Background
- 10 kV Device Characterization
- Driving and Protection
- Isolated Power Supply
- Control
- PCS Design and Testing
- **Grid Supporting Function and Validation**

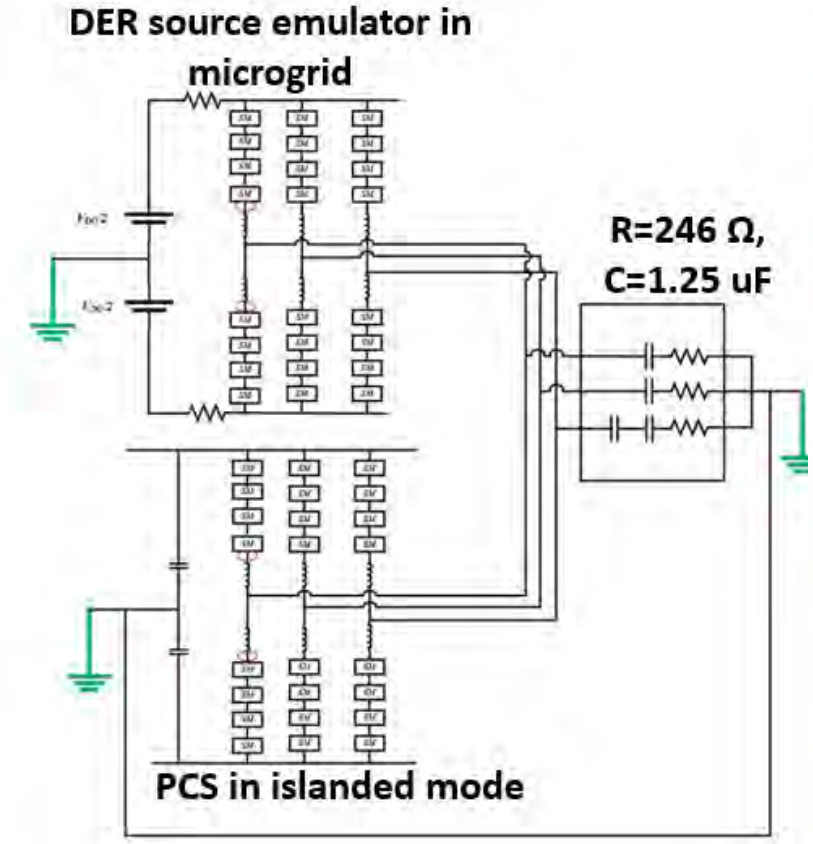
ASMG PCS Grid Support Function

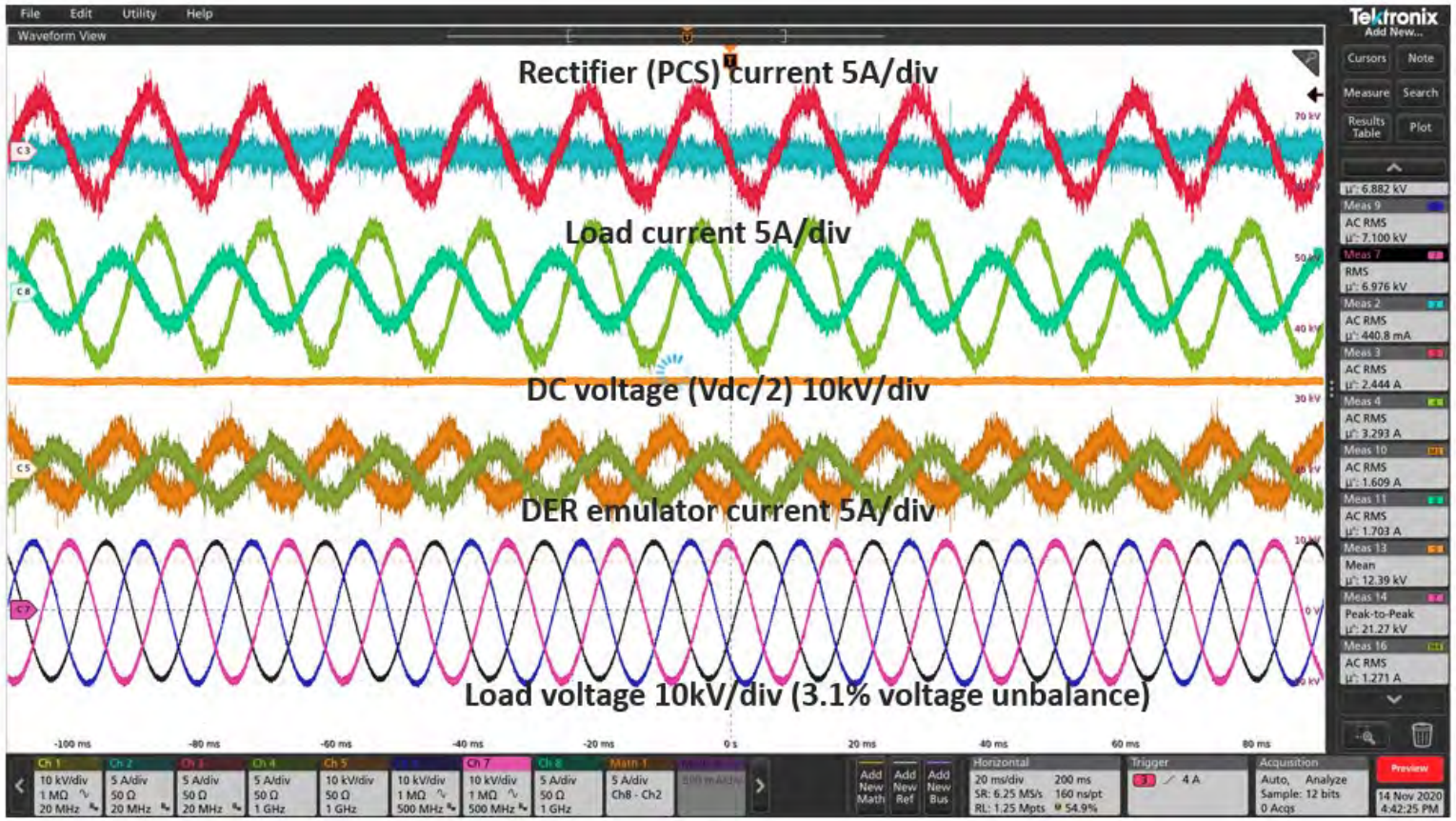
❑Grid Support Function Summary

Algorithm Types	Algorithm	Algorithm Descriptions
Steady-state functions	Grid-connected operation supporting	• Grid side PCS: DC voltage and ac current regulation • Microgrid side PCS: ac voltage and frequency control
	Islanded operation supporting	• Microgrid side PCS: DC voltage regulation and reactive power compensation
	Unbalanced load supporting	• Microgrid side PCS: unbalanced load support
PCS fault ride through	Grid side fault ride through in grid-connected mode	• Grid-side PCS: regulating dc voltage at low voltage • Microgrid PCS: working as normal
	Microgrid side fault ride through in grid-connected mode	• Grid-side PCS: working as normal • Microgrid side PCS: limiting output current
	Microgrid side fault ride through in islanded mode	• Microgrid side PCS: regulating dc voltage at low ac voltage and supporting microgrid voltage
PCS grid benefits	Active power filter	• Grid side PCS: filtering grid harmonics
	Grid stabilizer	• Grid side PCS: improving grid harmonic stability

ASMG PCS Grid Support Function and Validation

- Unbalanced load support in islanded mode
  - The DER source is normally three wire and emulated by a MMC for testing
  - The PCS works as the grounding as well as unbalanced load compensator
  - Successfully tested at 25 kV dc voltage

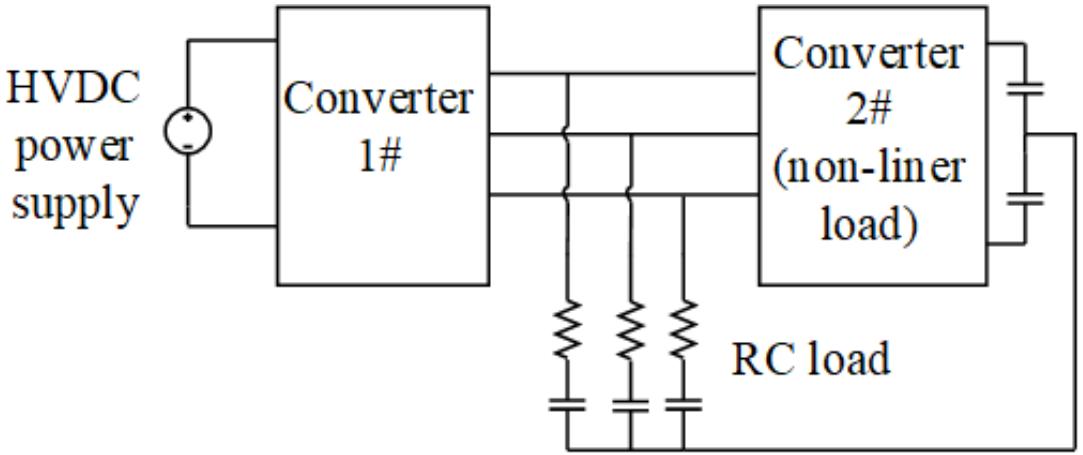


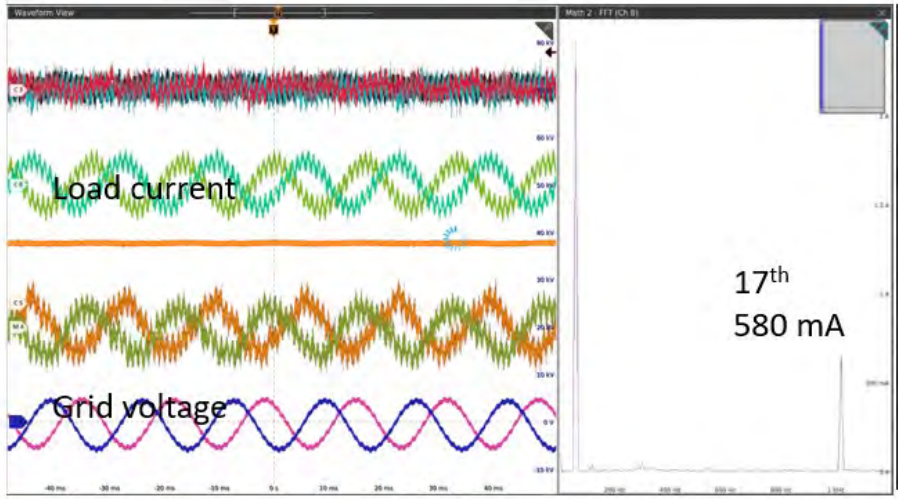


ASMG PCS Grid Support Function and Validation

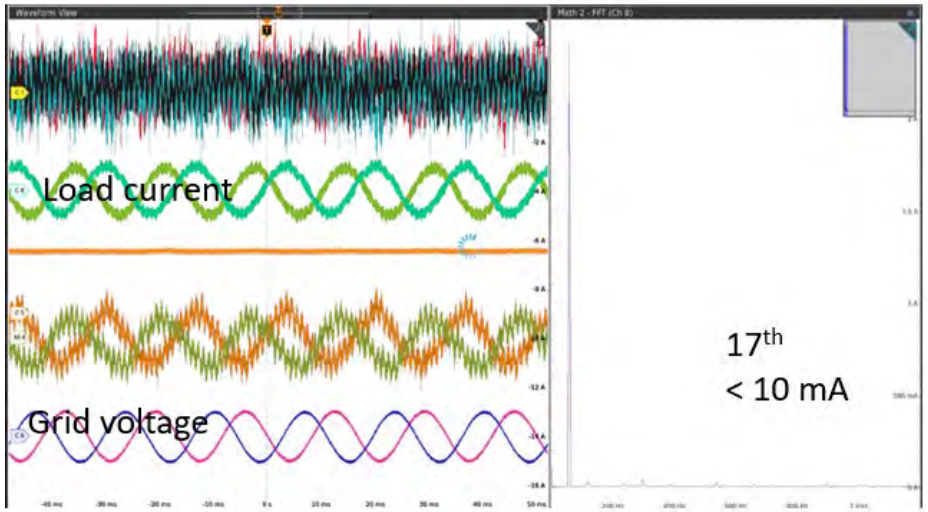
❑Active Power Filter

- Rectifier mode converter injects 17th harmonic current, 0.7 A peak value
- With APF function, grid voltage THD decreases





Without APF function

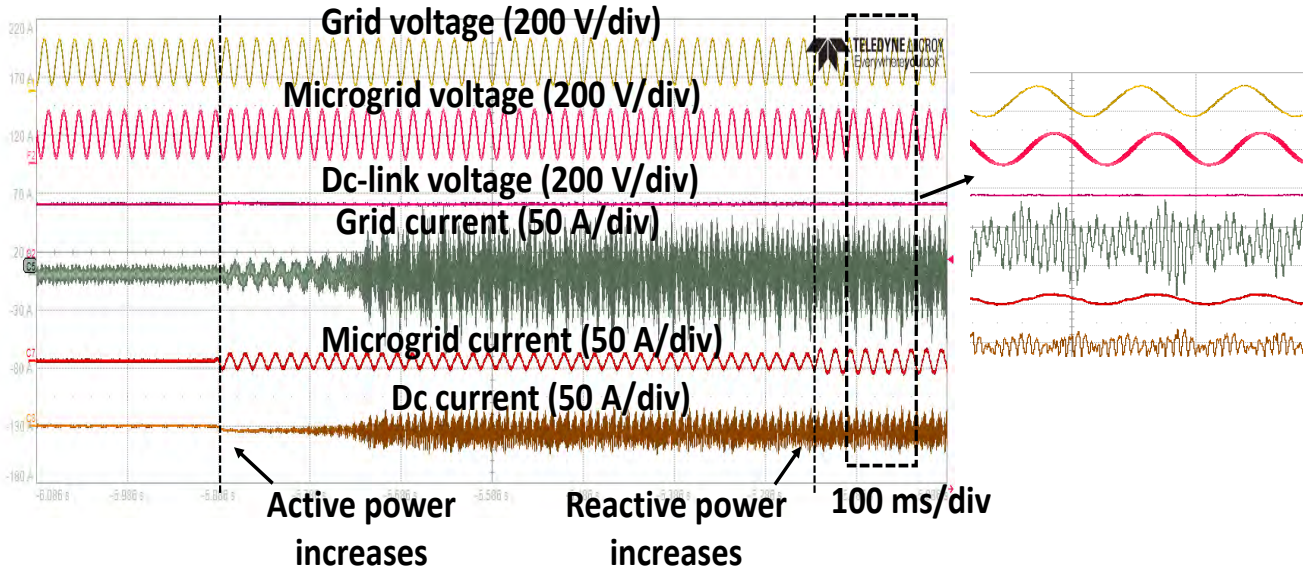


With APF function

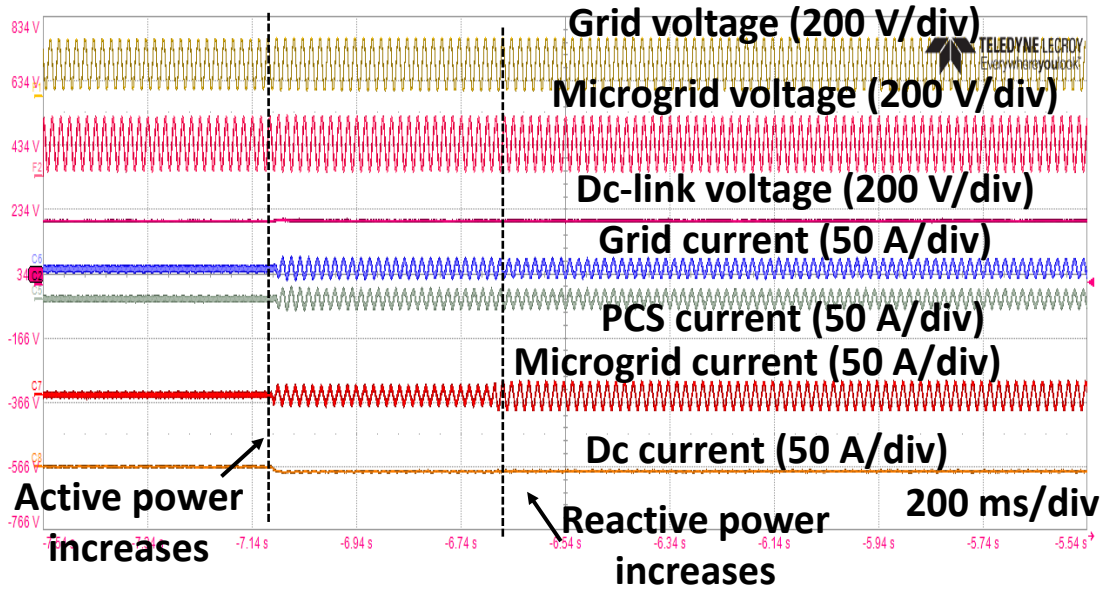
ASMG PCS Grid Support Function and Validation

❑Grid Stability Enhancement (HTB Test)

- SiC-based PCS can further benefit grid stability with its high control frequency
- Grid current becomes unstable with 4 kHz control frequency while no instability issue occurs with 10 kHz control frequency



4 kHz control frequency



10 kHz control frequency

F-CHP PCS Grid Support Function and Validation

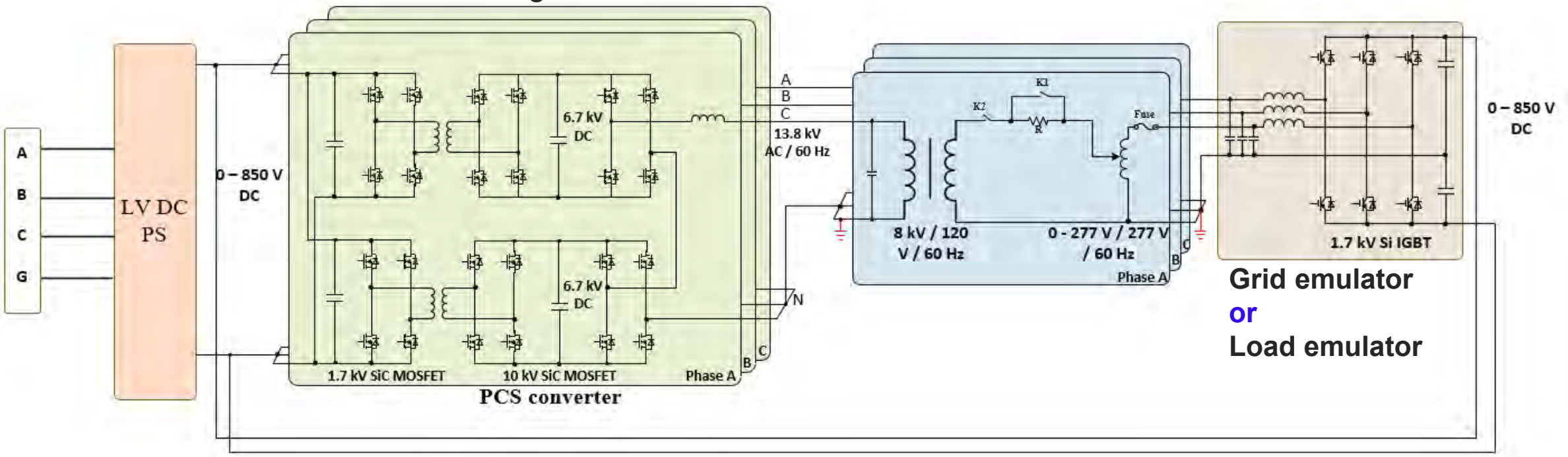
❑Tested Converter Performances and Grid Support Functions

#		Function
1	Converter performance	Full voltage and power rating operation (13.8kV/100kW)
2		Voltage THD ≤5% (Islanded mode, IEEE 519)
3		Current TDD ≤ 5% (grid-connected mode, IEEE 1547)
4		Converter efficiency ~ 96.4%
5		Voltage control bandwidth (300 Hz)
6		Current control bandwidth (1.1 kHz)
7	Grid requirements/functions	Var support (voltage support)
8		Low and high frequency ride through
9		Low and high voltage ride through
10		Mode transition between grid-connected mode and islanded mode
11		Protection (over voltage, under voltage, over frequency, under frequency, etc.)
12		Unbalanced load support in the islanded mode
13		AC grid faults

F-CHP PCS Grid Support Function and Validation

❑Grid Support Function Test Setup

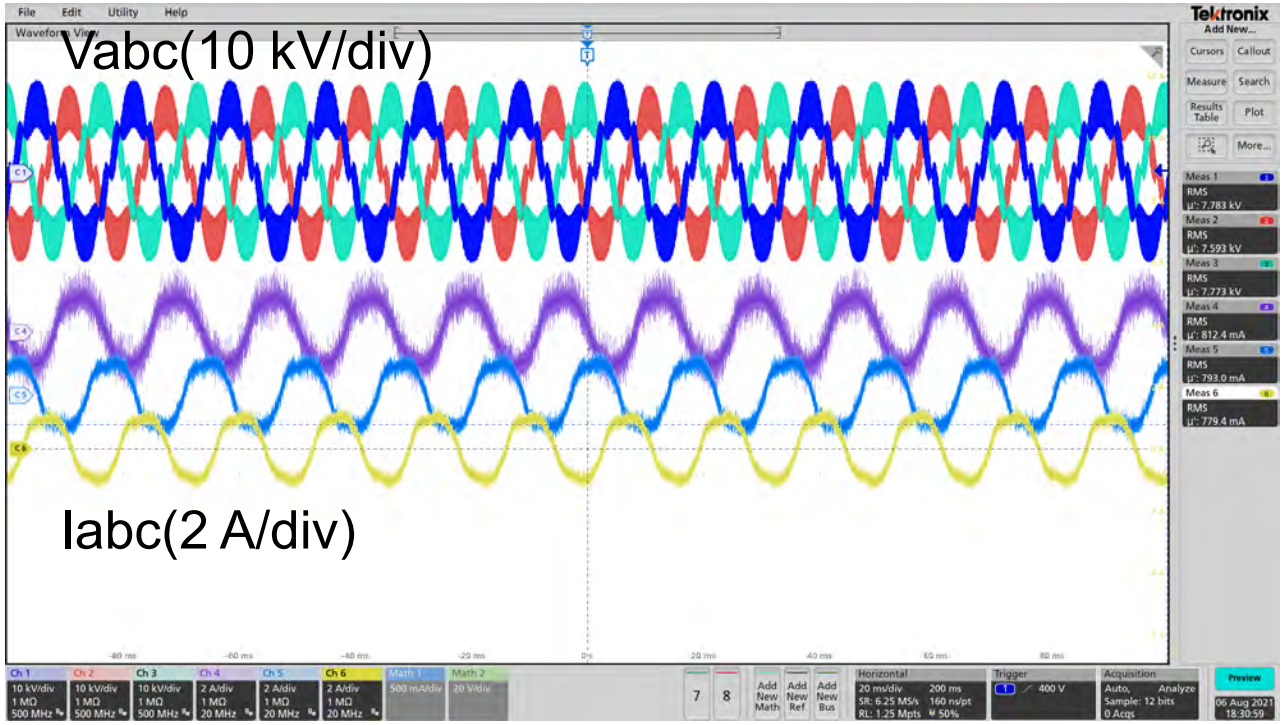
- **Islanded mode operation:**
  - The PCS converter control the AC voltage and frequency, the load emulator consumes power
- **Grid-connected mode operation:**
  - The PCS control the AC-side power, and the grid emulator control the AC voltage and frequency and also emulates different grid conditions



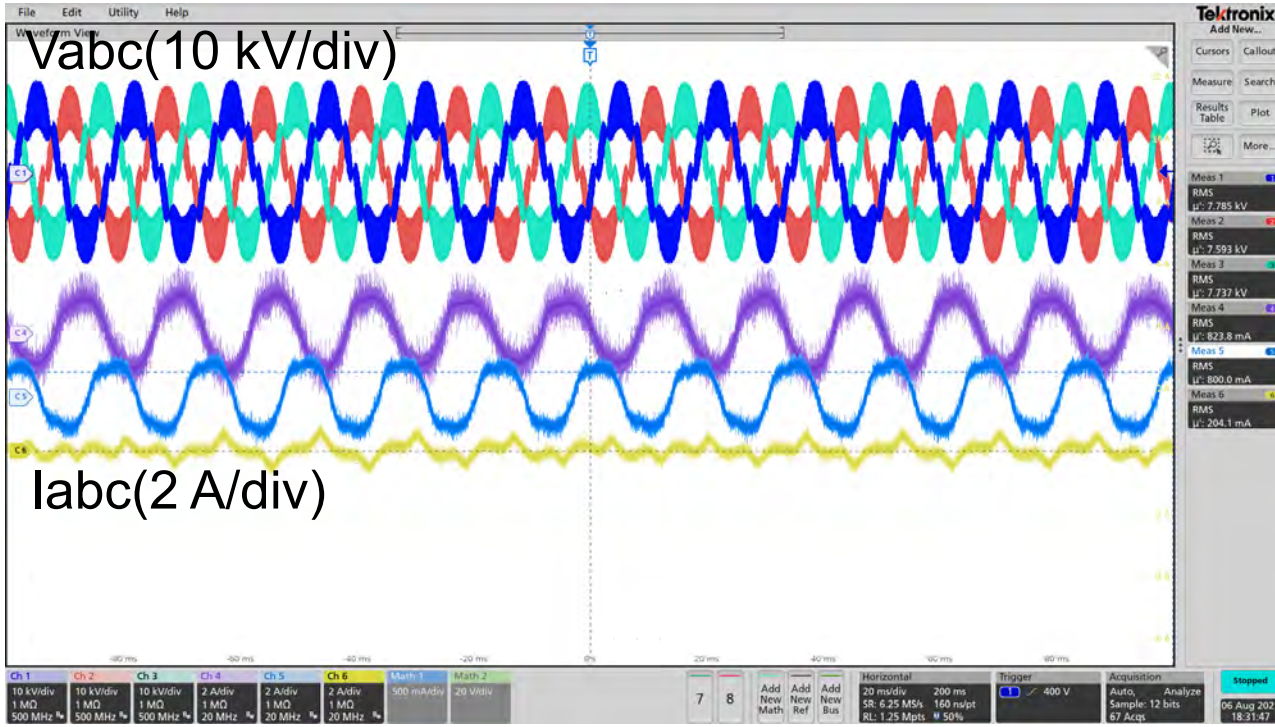
F-CHP PCS Grid Support Function and Validation

❑Islanded Mode Operation

- Balanced and unbalanced AC load support



Balanced AC load support

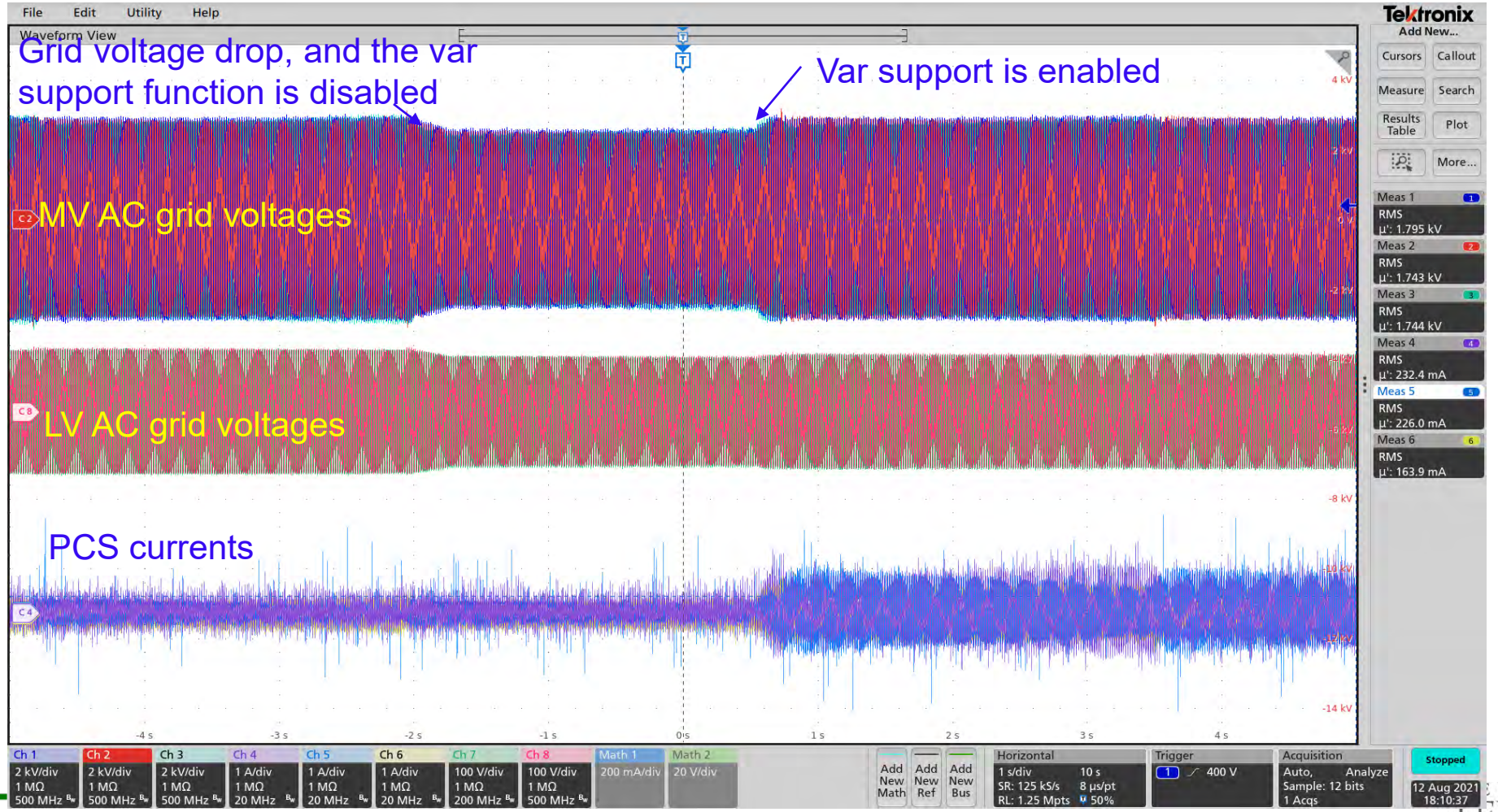


Unbalanced AC load support

F-CHP PCS Grid Support Function and Validation

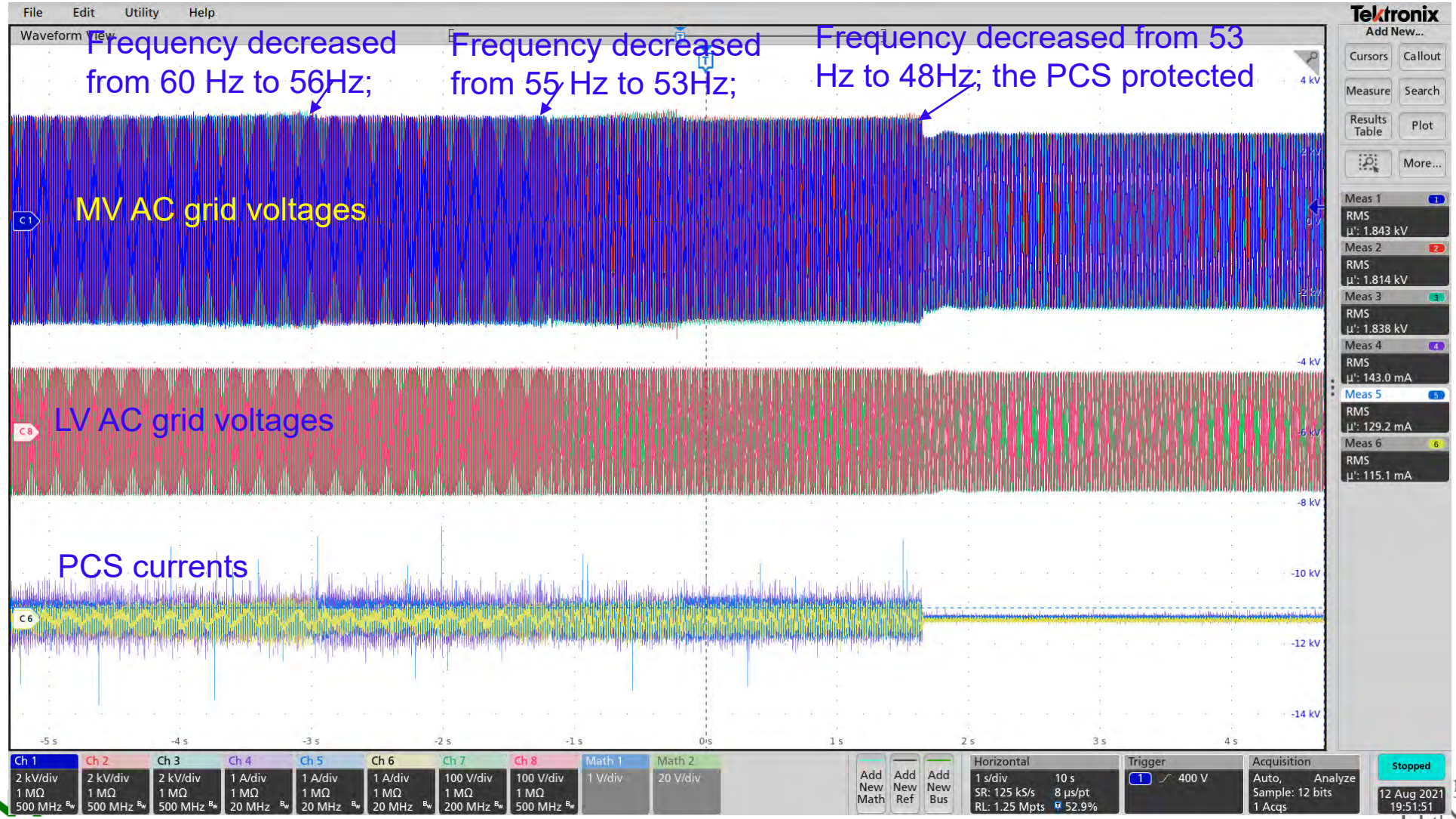
❑Voltage Support

- When the grid voltage changes, the PCS converter will stabilize the voltage by doing reactive power control



F-CHP PCS Grid Support Function and Validation

- Frequency Ride Through



Summary

- The new 10kV SiC MOSFET discrete devices and power modules are characterized, and the dv/dt can reach 100 V/ns
- The noise immunity of the gate drive and protection is critical for MV PCS. A robust gate drive is designed with improved desat protection achieving <350 ns response time under short circuit fault
- The noise immunity and insulation are critical for the isolated power supply. An isolated power supply with low parasitic capacitance (~1.85 pF) and high insulation capability (>15kV RMS) is design and built
- To support the grid, grid requirements are identified and considered in the converter design. The impact of overcurrent and overvoltage conditions are significant
- Two PCS converters for ASMG and F-CHP, respectively, are designed, constructed, and tested, considering different operation modes and grid requirements

Acknowledgements

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