SiC Power Devices: Market, Applications, and Introduction to Fabrication

2021 PowerAmerica Short Course

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PowerAmerica is a Member Supported/Driven Manufacturing Institute Addressing Gaps in WBG Semiconductor Power Technology to Enable Clean Energy Manufacturing, Job Creation, and Energy Savings

Power in membership

PowerAmerica provides a forum for members to improve the performance of SiC and GaN power technology and develop new applications. Our membership network spans the wide bandgap technology ecosystem, from materials to device developers and foundries to module manufacturers to end users, as well as universities that educate and supply the future workforce.

As we continue to grow, so does the diversity of our membership.

As Transitioning to Latest Nodes is Increasingly Expensive, Semiconductor Companies Exploit Alternative Foundry Volume Opportunities

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Number of Semiconductor Manufacturers with a Cutting Edge Logic Fab

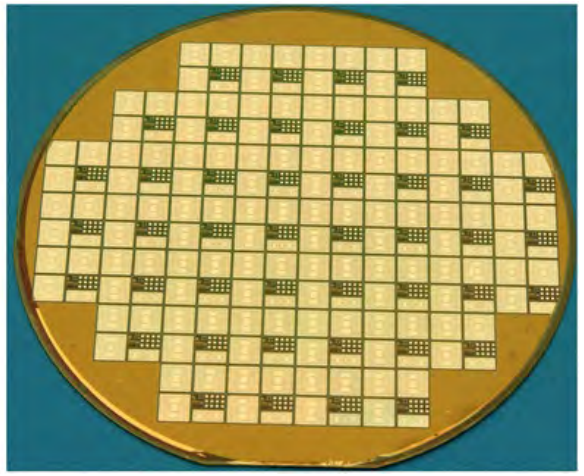
180 nm	130 nm	90 nm	65 nm	45 nm/40 nm	32 nm/28 nm	22 nm/20 nm	16 nm/14 nm	10 nm	7 nm	5 nm
SilTerra X-FAB Dongbu HiTek ADI Atmel Rohm Sanyo Mitsubishi ON Hitachi Cypress Sony Infineon Sharp Freescale Renesas (NEC) Toshiba Fujitsu TI Panasonic STMicroelectronics HLMC UMC IBM SMIC AMD Samsung TSMC Intel	ADI Atmel Rohm Sanyo Mitsubishi ON Hitachi Cypress Sony Infineon Sharp Freescale Renesas Toshiba Fujitsu TI Panasonic STM HLMC UMC IBM SMIC AMD Samsung TSMC Intel	Cypress Sony Infineon Sharp Freescale Renesas Toshiba Fujitsu TI Panasonic STM UMC IBM SMIC AMD Samsung TSMC Intel	Renesas Toshiba Fujitsu TI Panasonic STM HLMC UMC IBM SMIC GlobalFoundries Samsung TSMC Intel	Renesas Toshiba Fujitsu TI Panasonic STM HLMC UMC IBM SMIC GF Samsung TSMC Intel	Panasonic STM HLMC UMC IBM SMIC GF Samsung TSMC Intel	IBM GF Samsung TSMC Intel	SMIC GF Samsung TSMC Intel	Samsung TSMC Intel	Samsung TSMC Intel	Samsung TSMC Intel

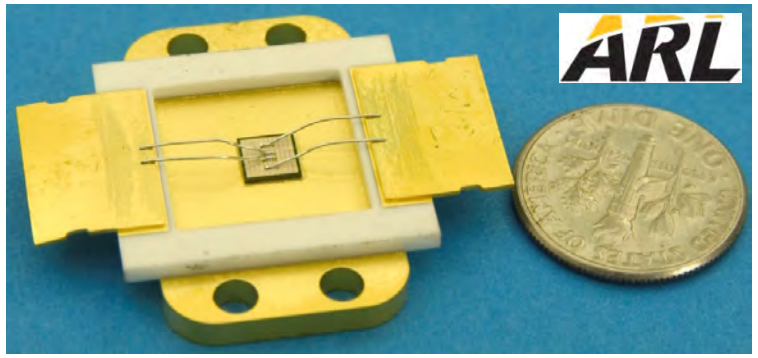
Source: Wikichips

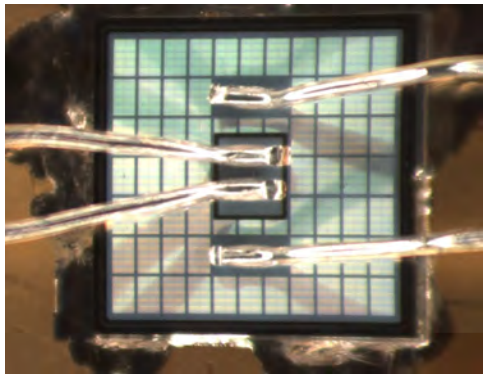
Opportunities Beyond Memory and Logic:

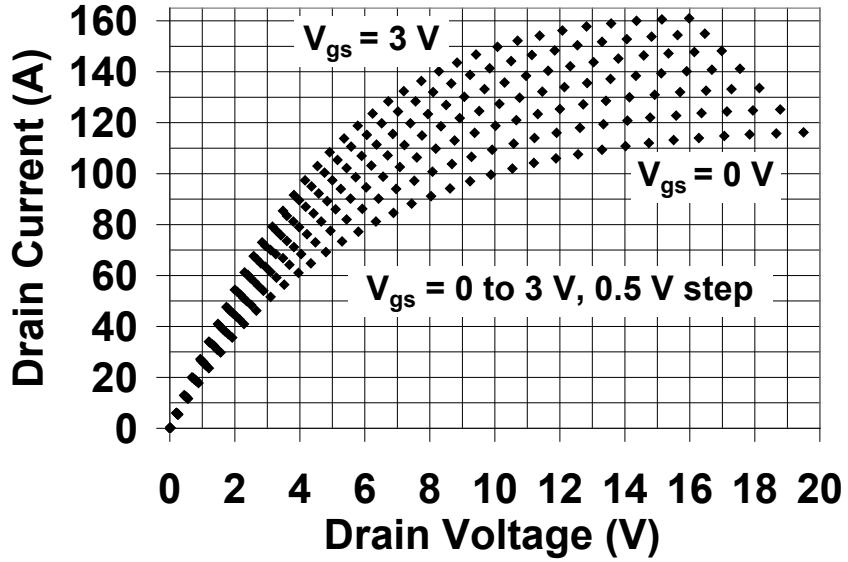
- IoT
- AI
- 5G
- Quantum computing and superconductivity
- Power Devices

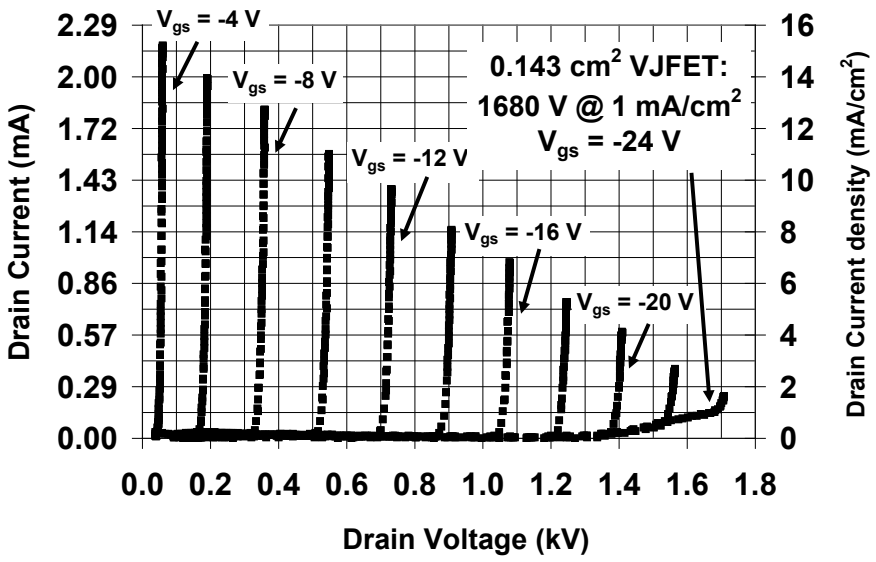
Power Devices are Large Discrete Transistors Capable of Switching High Currents and Blocking High Voltages





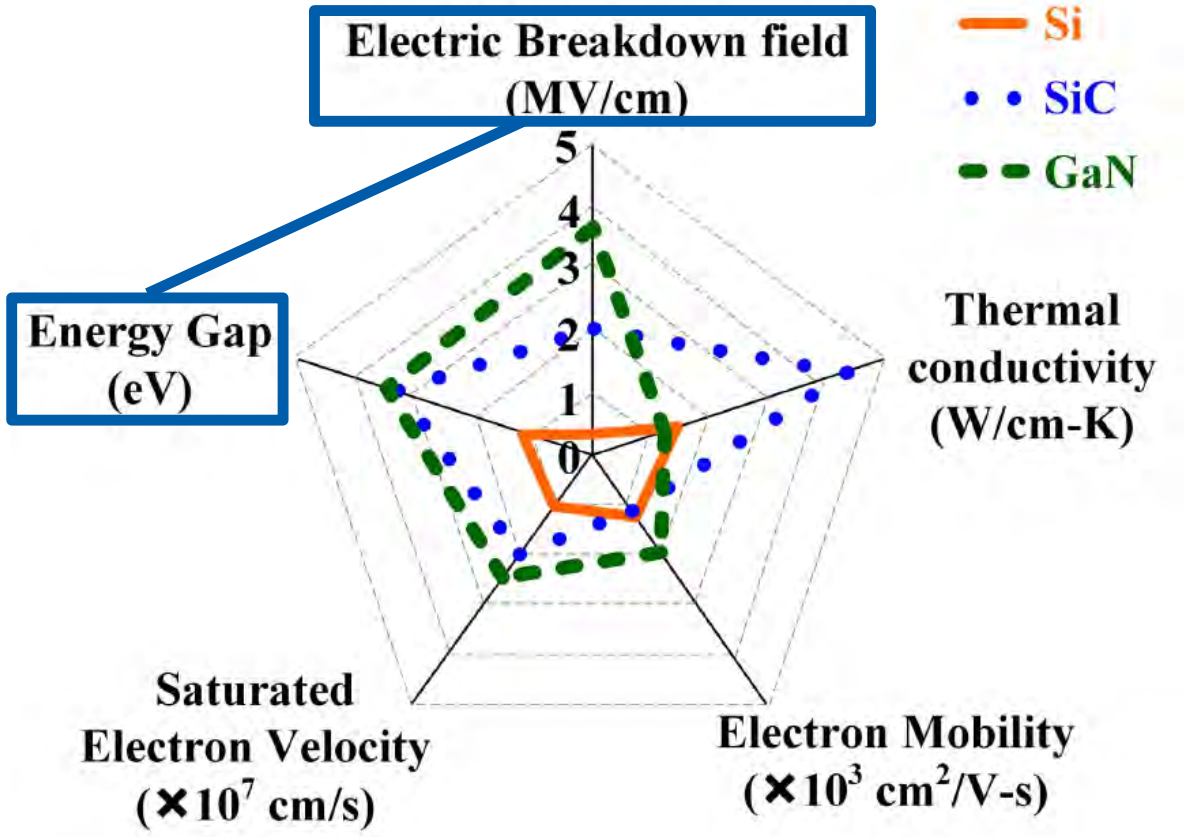






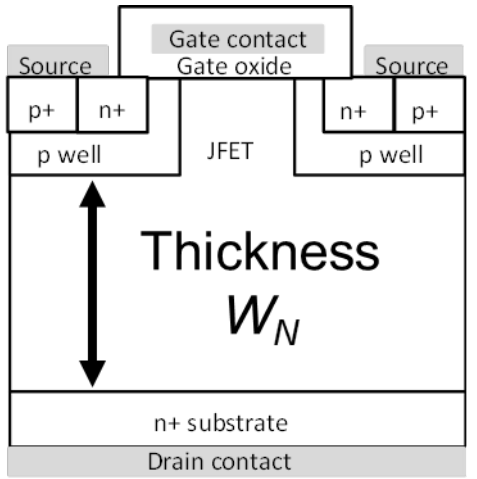
V. Veliadis et al., IEEE Electron Dev. Lett., Vol. 29, No. 10, pp. 1132 – 1134, 2008

GaN/SiC Power Devices Allow for More Efficient and Novel Power Electronics



Device Thickness

$$W_N = \left(\frac{3}{2}\right)\left(\frac{V_B}{E_C}\right)$$



Device Resistance

$$R_{ON,SP} = \left(\frac{3}{2}\right)^3 \frac{V_B^2}{\mu_N \varepsilon_S E_C^3}$$

Large Bandgap and Critical Electric Field allow for high voltage devices with thinner layers: lower resistance and associated conduction losses

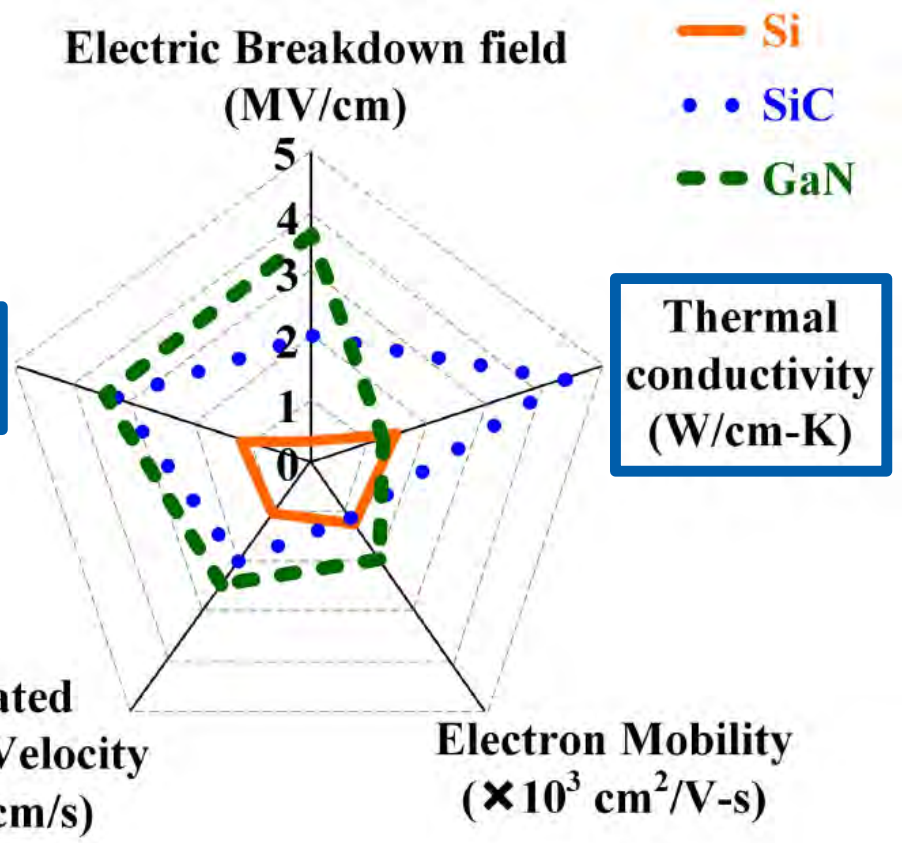
Thinner layer and low specific on-resistance allow for smaller form factor that reduces capacitance: higher frequency operation, reduced size passives

Large SiC Bandgap and Thermal Conductivity Enable Robust High Temperature Operation with Reduced Cooling

$$n_i{}^2 \propto e^{\frac{-E_g}{kT}}$$

Energy Gap (eV)

Si: ~10^{10} cm^{-3}
SiC: ~10^{-9} cm^{-3}



SiC/GaN devices enable **more efficient, lighter, smaller form factor** power electronics operating at high frequencies, and at elevated temperatures with reduced cooling.

Large Bandgap results in relatively low intrinsic carrier concentration: low leakage and robust high temperature operation

Large Thermal Conductivity: high power operation with reduced cooling requirements

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Ultra Wide-bandgap Materials (Ga_2O_3, Diamond, AlN) Can Further Increase the Performance of Power Devices

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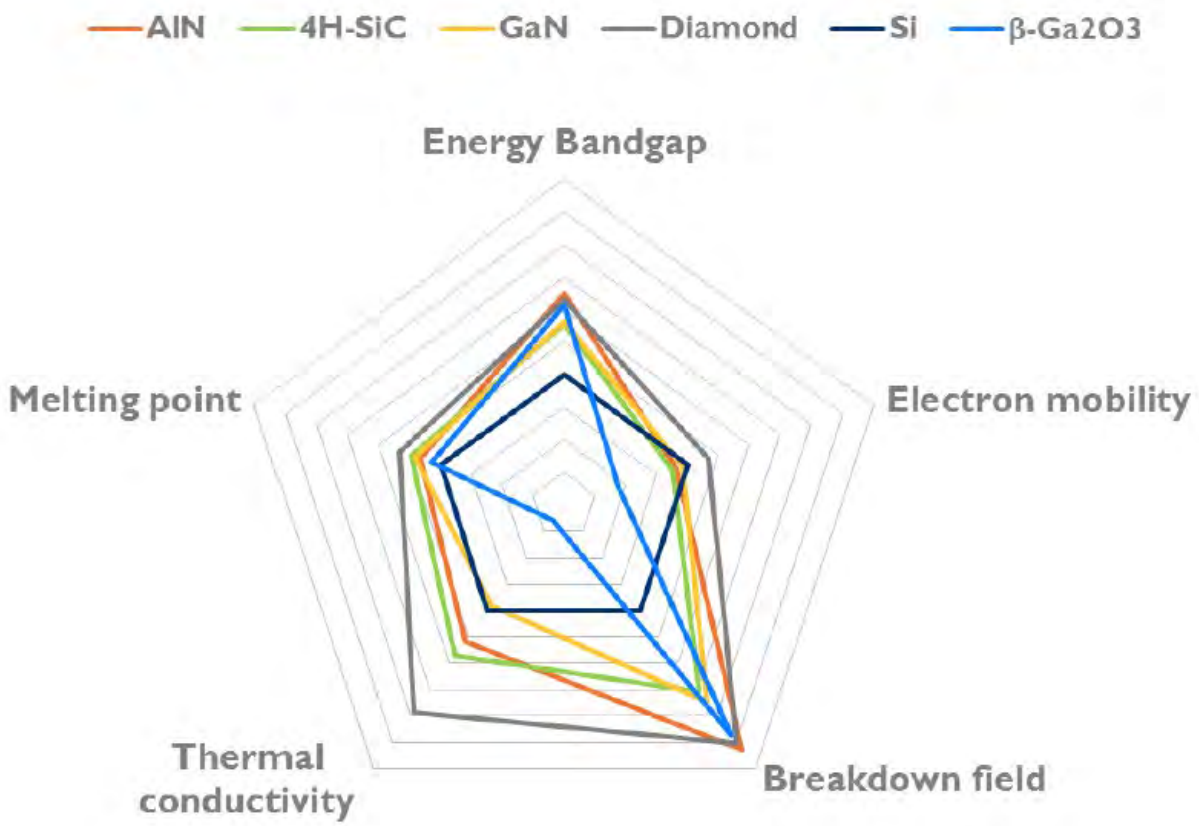
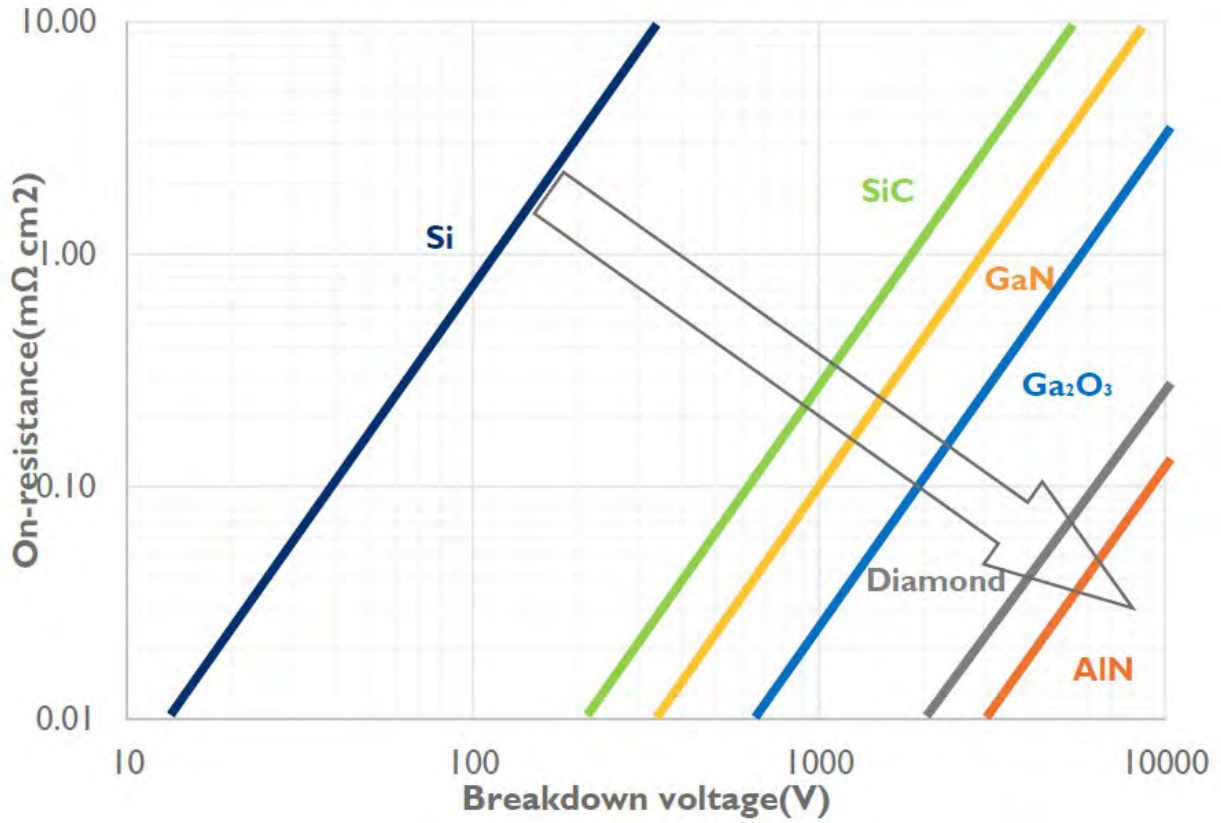
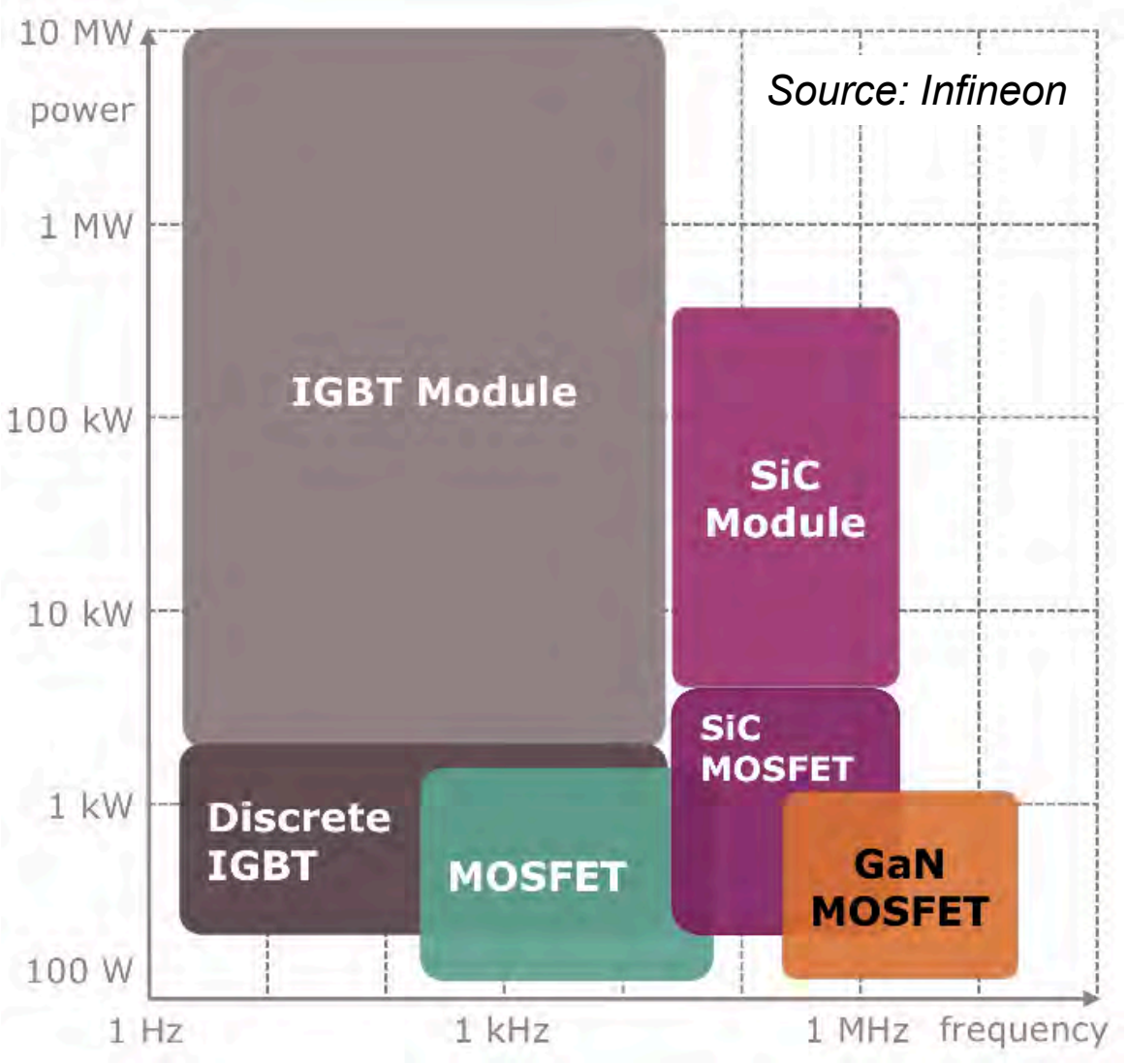
2016 Yole Report



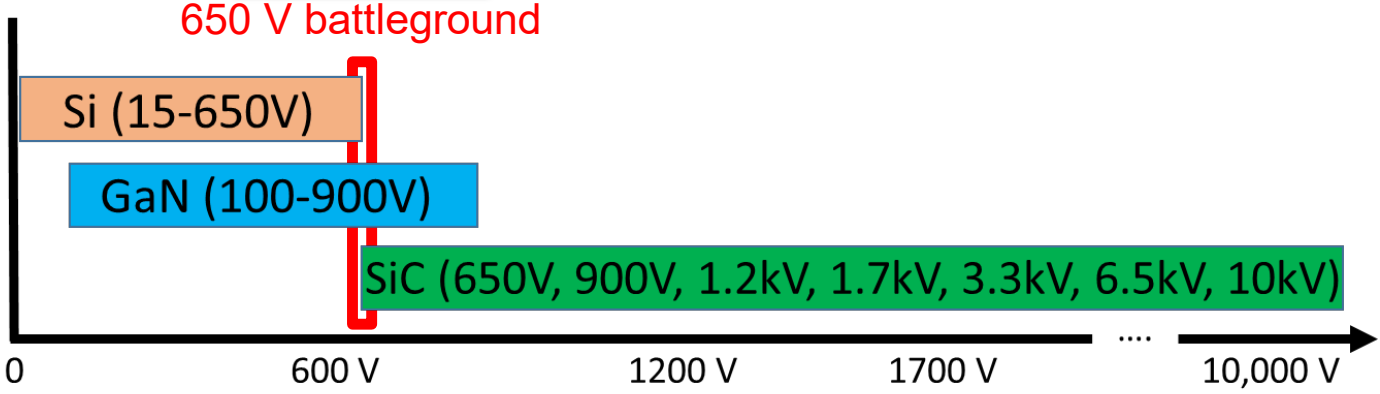


Ultra wide-bandgap materials (Ga_2O_3, Diamond, AlN) have larger Bandgaps and Breakdown-Electric-Fields than those of GaN and SiC

Selection of Si, SiC, or GaN is Application Specific and Driven by Voltage, Current, Frequency, Efficiency, Temperature, and Cost Considerations



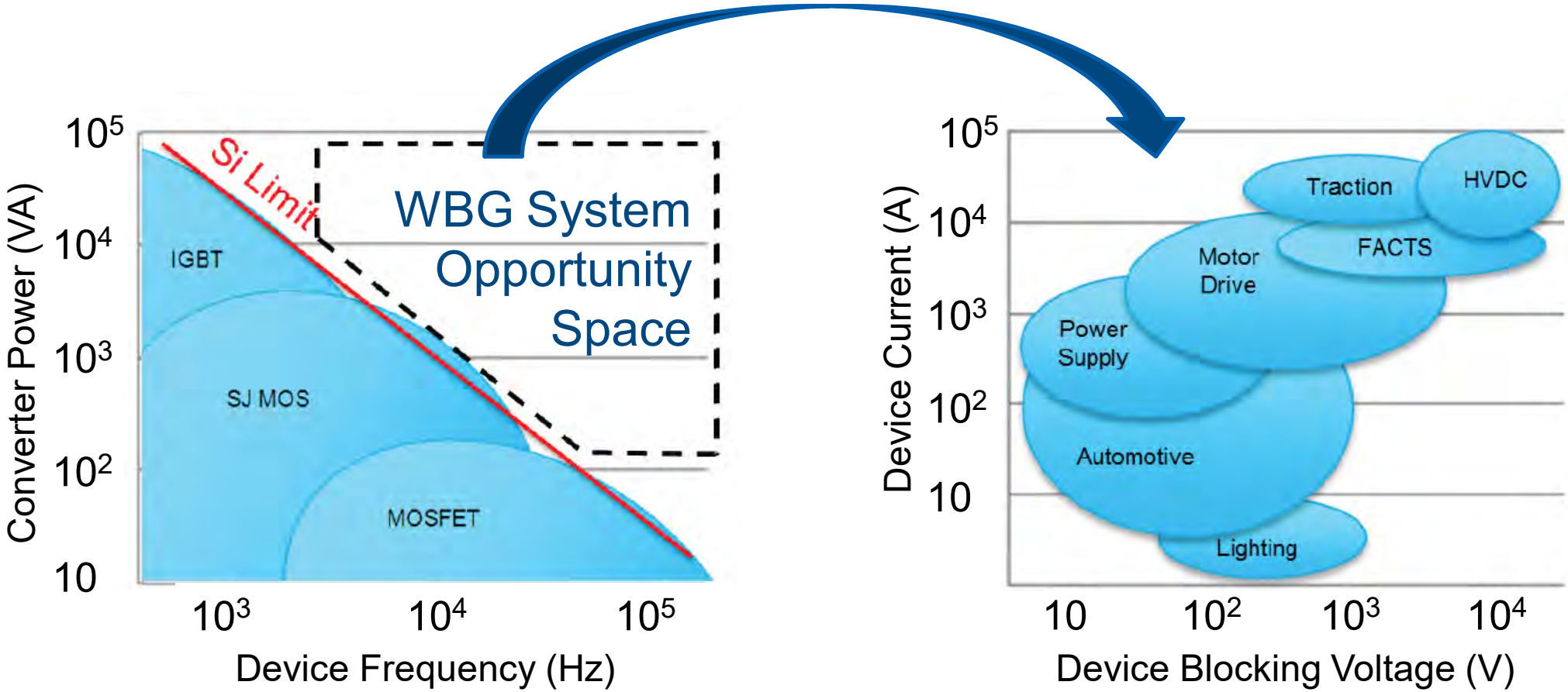
650 V battleground



Si, GaN, and SiC all compete in the lucrative 650 V range:

- *Si* is reliable, rugged, cheap, and capable of high current
- *GaN* offers efficient high-frequency operation at reasonable cost
- *SiC* is efficient and operates at high current and frequency

SiC/GaN Devices Are Uniquely Positioned to Enable Next Generation Power Electronics Growth



Graphs: Isic C. Kizilyalli *et al.*, ARPA-e Report 2018
https://arpa-e.energy.gov/sites/default/files/documents/files/ARPA-E_Power_Electronics_Paper-April2018.pdf

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WBG Power Electronics is a Key Driver of High-Value Manufactured Products

Automotive/Transportation Sector
2nd largest U.S. export market
Power Electronics Drivers: Vehicle Electrification & Automation

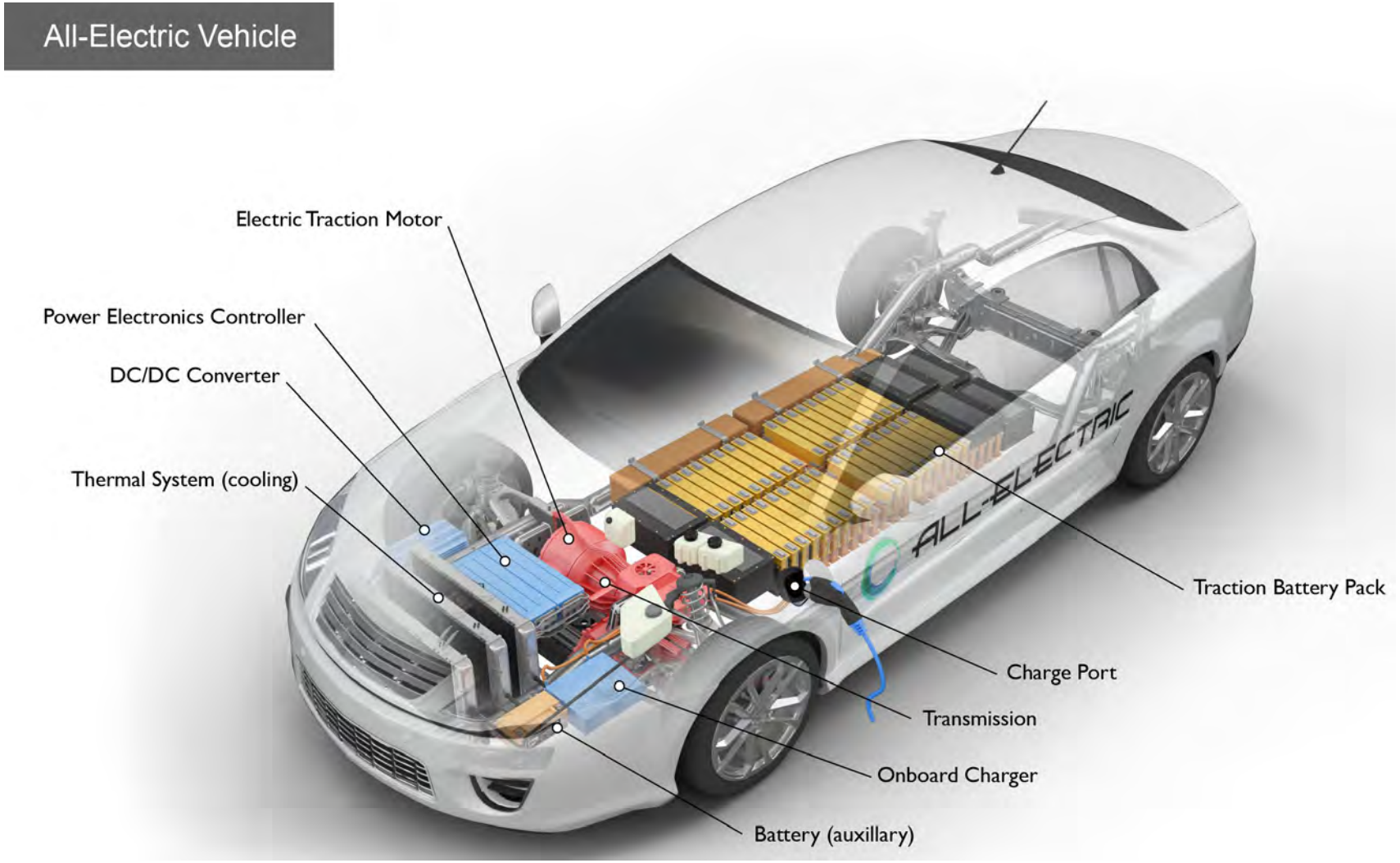
Information Technology Hardware Sector
Power Electronics Drivers: Efficiency & Bandwidth Growth

Grid Infrastructure Sector
Power Electronics Drivers: Reliability, Sustainability, Flexible Resources

Electric Motor Drives
Power Electronics Drivers: Variable Speed Drives, Efficiency, Weight & Volume reduction

Aerospace Sector
Global Market: US$700B
U.S. Exports: at US$120B is the largest US export market
Power Electronics Drivers: Sensors/Radar, Actuation, Propulsion

Vehicle Electrification is a High Volume Opportunity for WBG Power Devices and Electronics



https://afdc.energy.gov/vehicles/how-do-all-electric-cars-work

Electric traction motor: Uses power from the traction battery pack to drive the vehicle's wheels

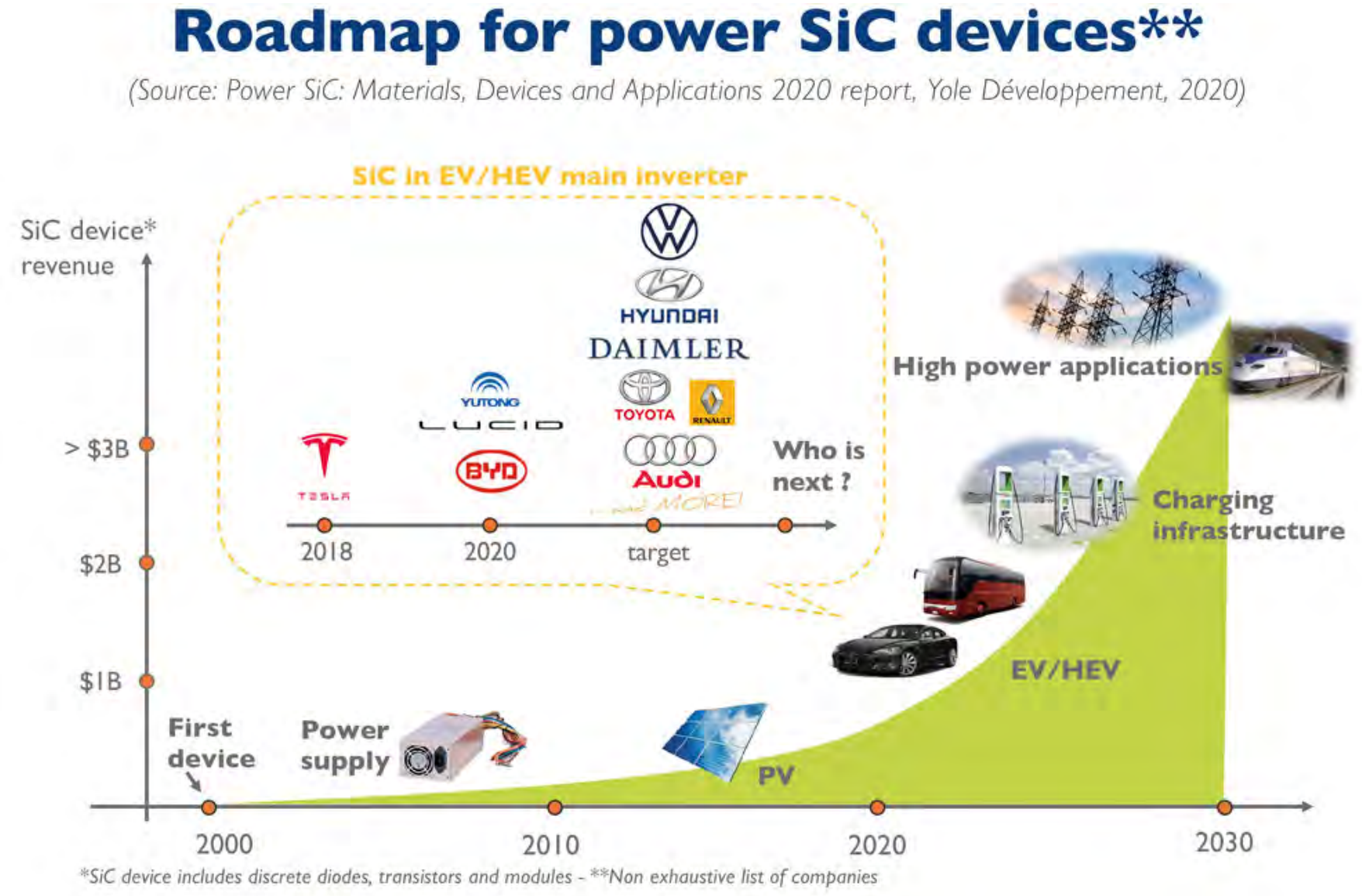
DC/DC converter: This device converts higher-voltage DC power from the traction battery pack to the lower-voltage DC power needed to run vehicle accessories and recharge the auxiliary battery.

Onboard charger: Takes the incoming AC electricity supplied via the charge port and converts it to DC power for charging the traction battery.

Traction battery pack: Stores electricity for use by the electric traction motor.

Battery (all-electric auxiliary): In an electric drive vehicle, the auxiliary battery provides electricity to power vehicle accessories.

The EV/HEV Market is the Strongest Contributor to SiC Growth



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The Range International Information Group Data Center in Langfang China is 585 Thousand Square Meters in Area

Waste Heat Management is Challenging!

Mitigation Approaches:

- Quantum computing
- SiC/GaN
- Artificial intelligence for resource management
- Liquid and immersion cooling technologies
- Materials for ultrahigh density storage

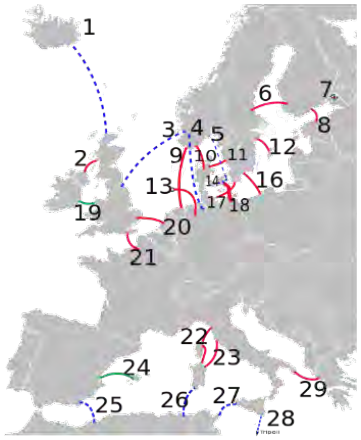
*From 2010 to 2018, global data center energy increased by 6% while compute instances increased by 550%. The energy intensity of global data centers has decreased by 20% annually since 2010, and global data center consumption was 1% of global electricity in 2018.

*Science vol. 367, issue 6481, p. 984, Feb. 2020 V. Veliadis

Advances in Power Electronics and Control Systems Drive Efficient, Flexible, and Reliable Grid

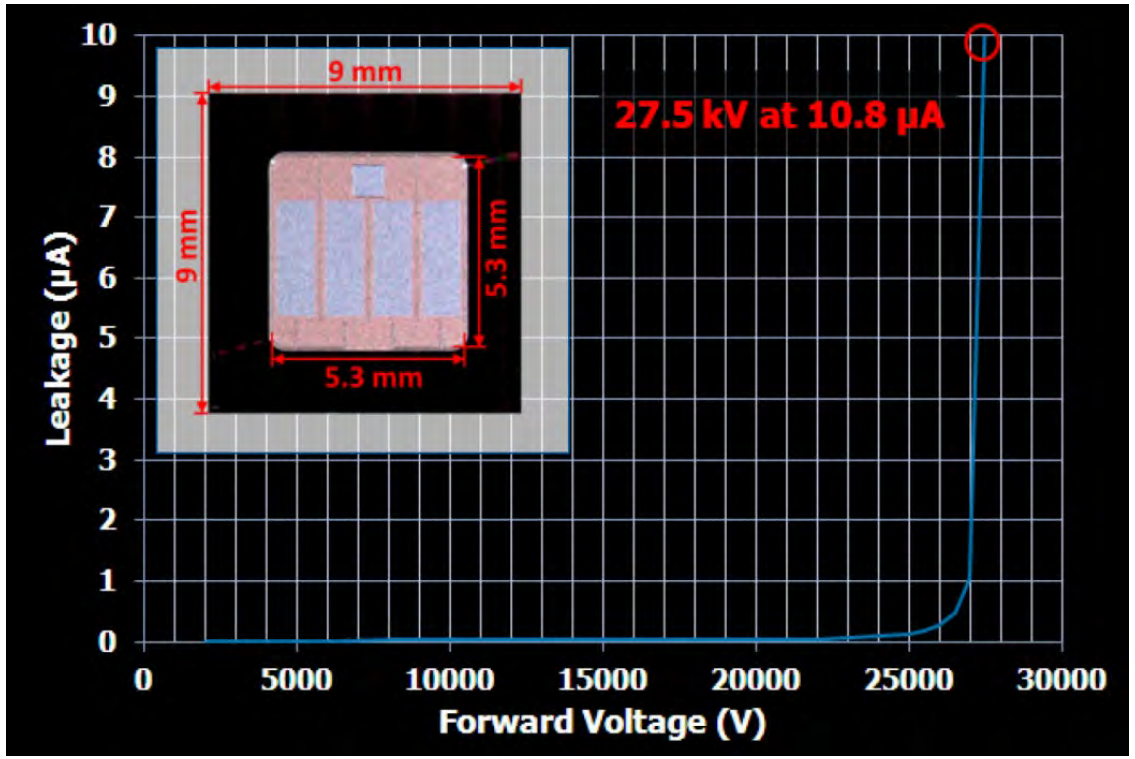
Electric Grid Applications

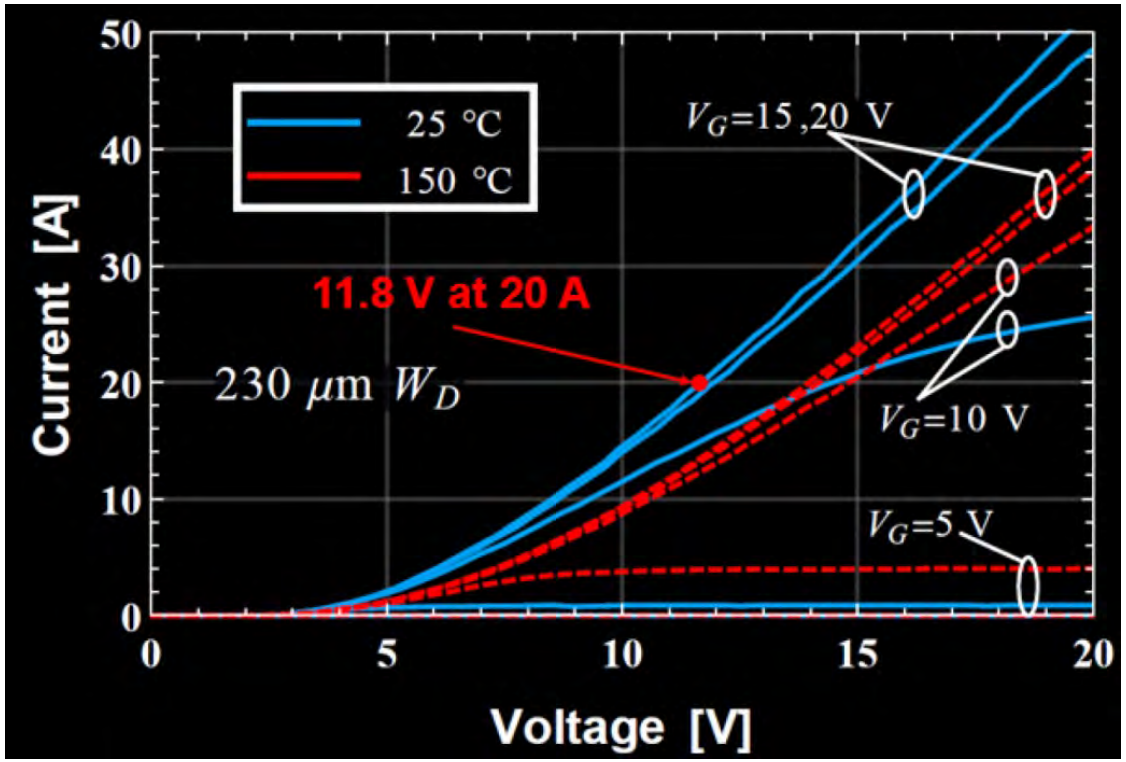
- HVDC Transmission
- FACTS
- Microgrids
- Solar Energy
- Wind Energy (500 GW installed)
- Energy Storage



Currently, ~40% of generated electric power passes through Power Electronics between generation and use

Wolfspeed SiC IGBT Blocks 27 kV with a Low Leakage Current of 1 µA and a DC current output of 20 A





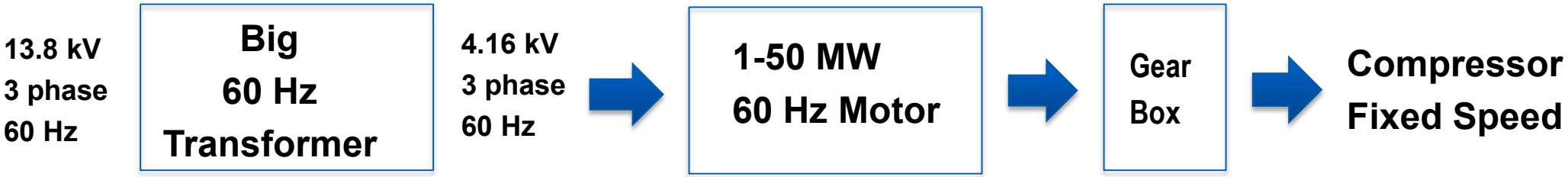
230 µm SiC drift layer supports 27 kV

~2700 µm Si drift layer needed for 27 kV; major conduction and switching losses

ECSCRM September 25, 2014, Courtesy of Dr. S.-H. Ryu, CREE Inc.

Variable Speed Drives Enable Efficient Adaptation to Motor Speed/Torque and Reduce Energy Consumption

Traditional Motor Drives: 20-40% of energy is wasted with throttles and other mechanical devices



Across all sectors, electric motors account for approximately 45% of total world electricity consumption International Energy Agency (IEA)

https://arpa-e.energy.gov/sites/default/files/documents/files/ARPA-E_Power_Electronics_Paper-April2018.pdf

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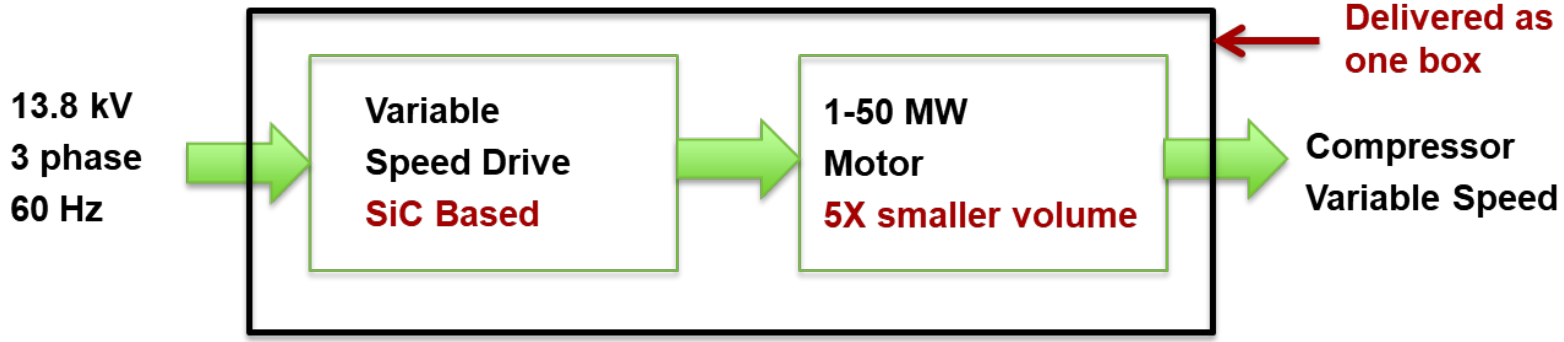
SiC Based Variable Speed Drives have Volume, Weight, and Cost Advantages

Si based VSD save energy but have limited adoption due to big footprint, weight, and cost

SiC based VSD use novel architectures to reduce volume, weight and cost, accelerating adoption



- Big 60 Hz Transformer replaced by small high frequency Transformer
- VSD system is reduced in size & weight and cheaper due to WBG devices
- Gear Box eliminated
- Motor size reduced by 5x – cheaper, less magnets

US Department of Energy (DOE), Next Generation of Electric Machines Program

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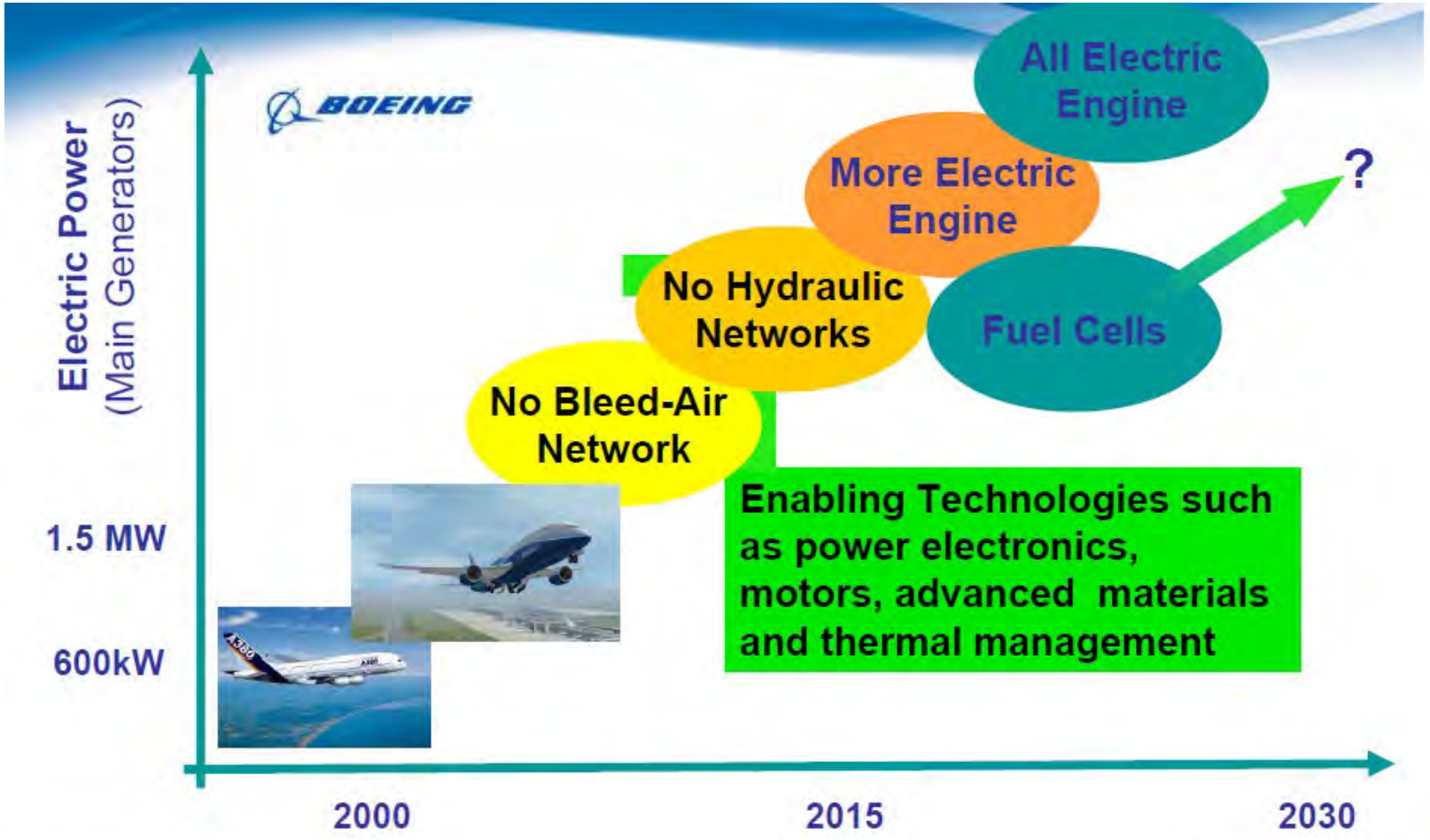
"More Electric Aerospace" is Primarily an Evolutionary Application of Power Electronics and Energy Storage

A more electric aircraft is a more energy efficient aircraft

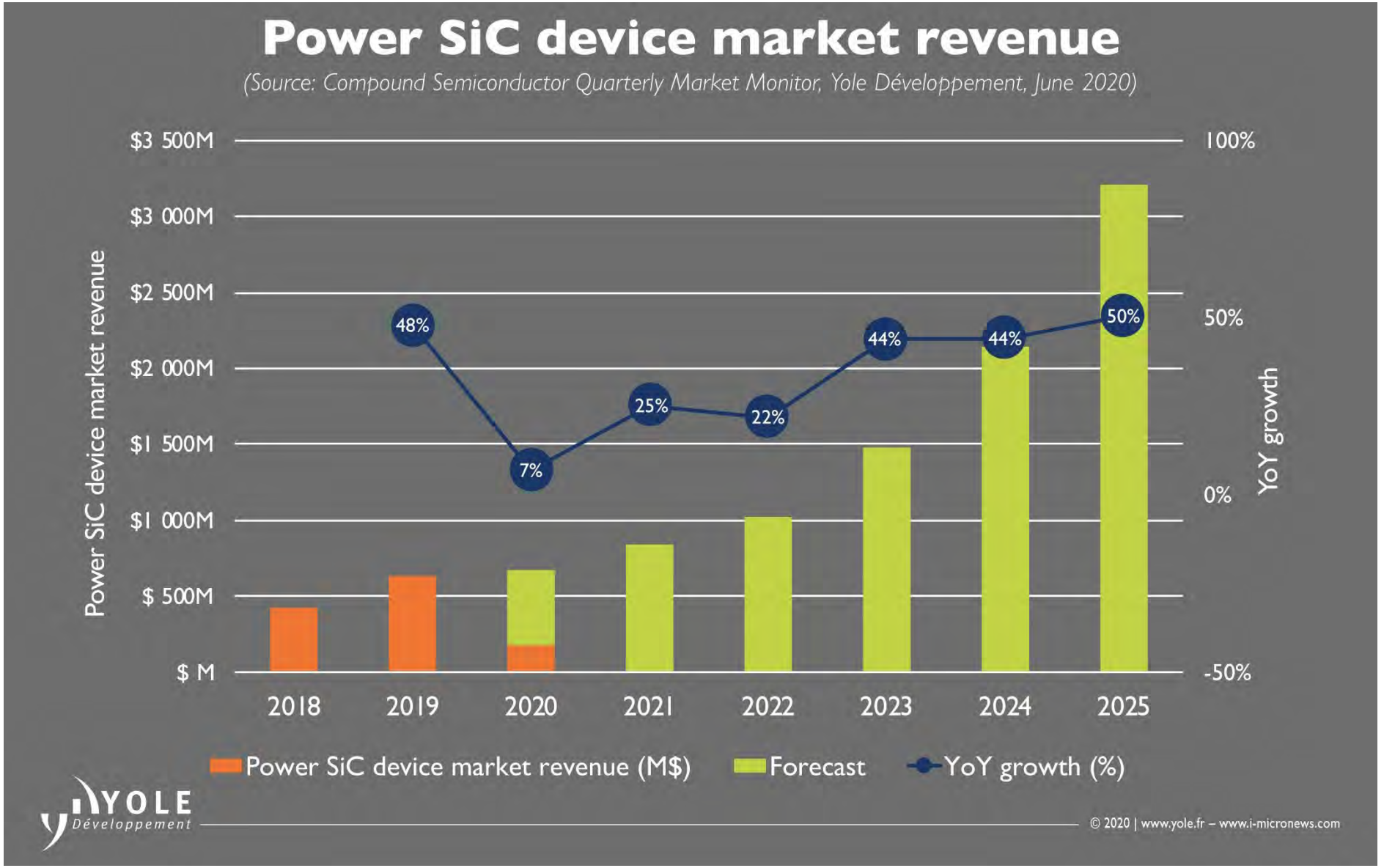


- *Replace hydraulic systems with electrical*: lower fluid leak hazard, lower operation/maintenance cost, lower system complexity, higher reliability
- *Electrical generation/distribution systems replace electromechanical relays, pneumatics, and hydraulics*: reduce aircraft wiring and overall weight for fuel savings
- *Increased power electronics density*: reduces aircraft weight for fuel savings

Higher fuel efficiency, lower maintenance/operation costs, higher reliability, less noise, lower NOx emissions

Power electronics innovations drive aerospace – aircraft, satellites, drones, rovers

SiC Device Projected Revenue by 2025: $3.2B/Yr



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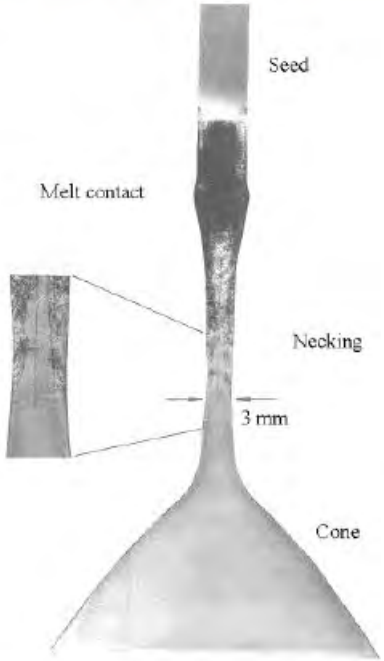
SiC Substrate Growth is More Complex Than That of Si

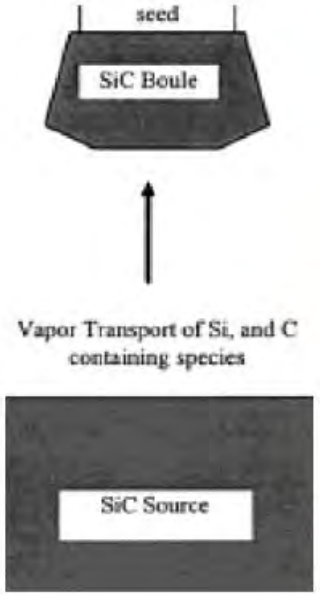
Silicon liquid-phase growth

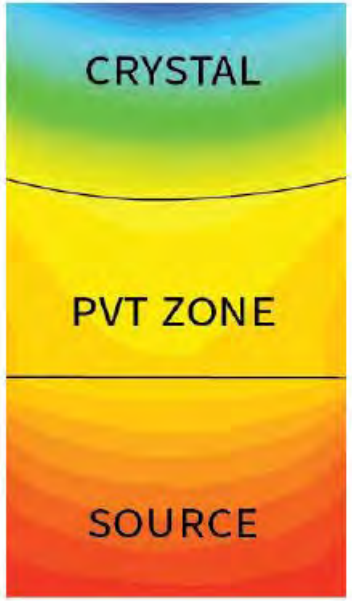


https://www.tf.uni-kiel.de/matwis/amat/semitech_en/kap_4/illustr/i4_1_6.html

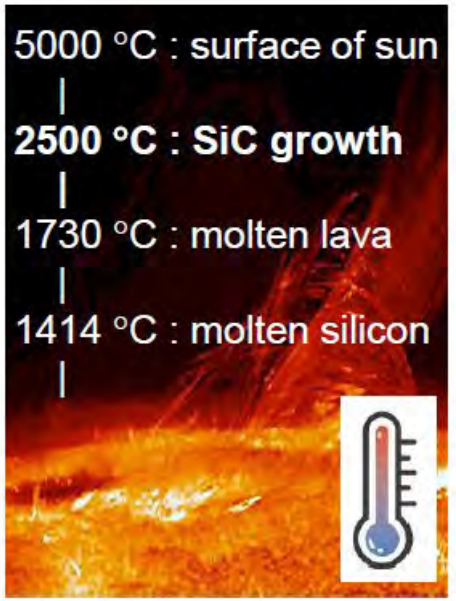
- Si is pulled from molten silicon
- Seed is very small, necking reduces defects
- Rapid crystal expansion
- Process temperature ~1500°C

SiC vapor-phase growth





Glass et al, phys. Stat. sol., 1997



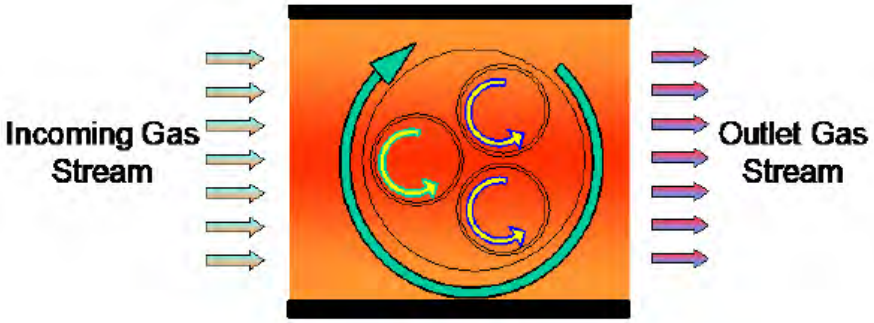
How Hot?

- SiC does not melt (sublimes)
- Must use large seed
- Limited crystal expansion
- Process temperature ~2500°C

Slide courtesy of Warren Weeks, CREE Wolfspeed

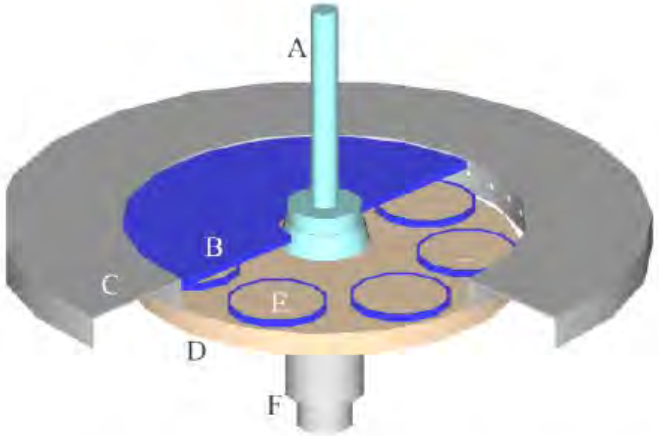
SiC Epitaxial Growth is Well Established and Strives to Minimize Defect Propagation from the Substrate

Two SiC CVD Epitaxy Platforms



Horizontal Hot-Wall Reactors:

- 5 x 100 mm, 3 x 150 mm or 1 x 200 mm
- Growth Conditions
  - 1500 - 1650°C
  - 30 - 90 torr
  - 2 - 30 mm/hr
  - silane/propane



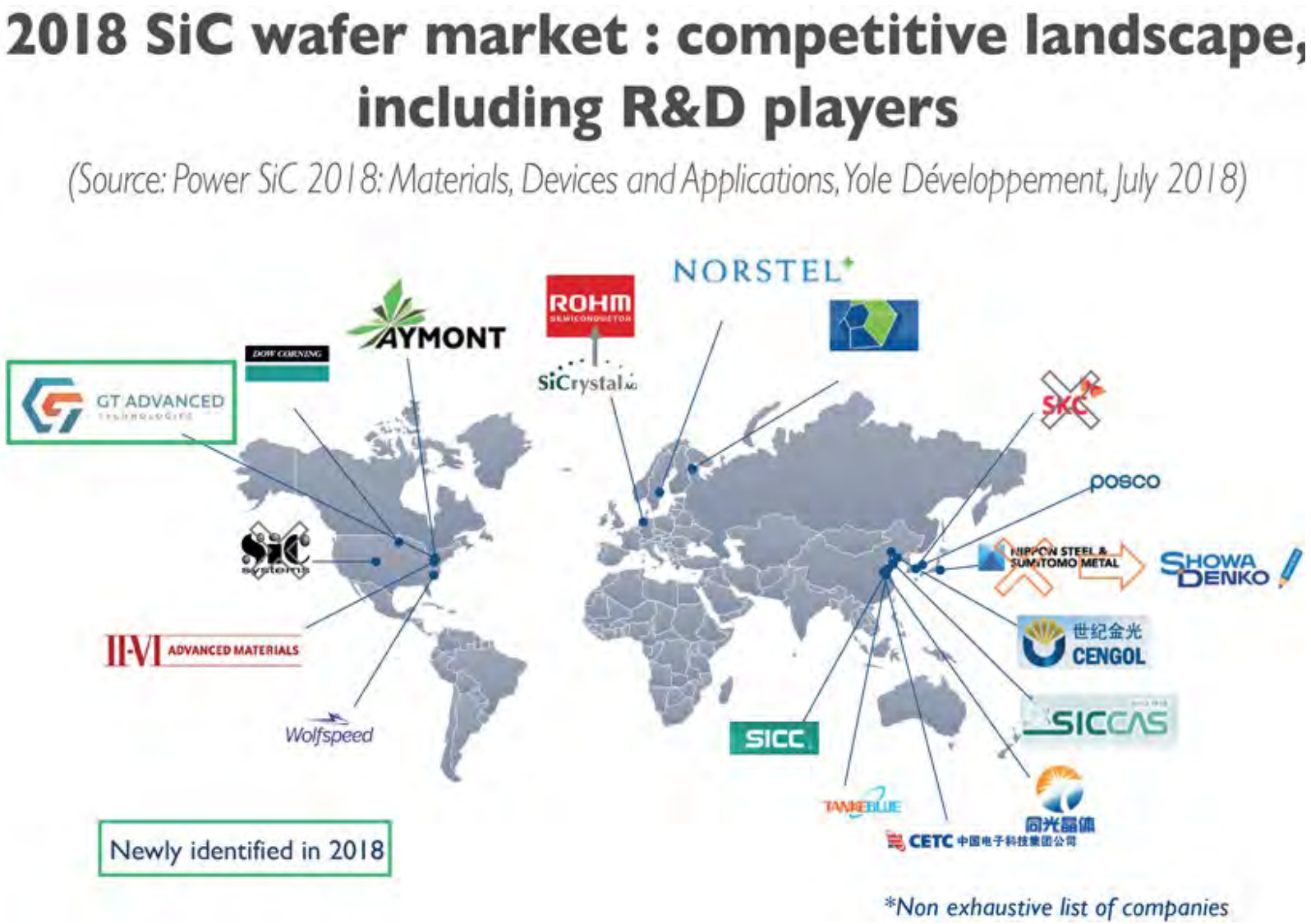
Planetary Warm-Wall Reactors:

- 12 x 100 mm, 8 x 150 mm
- Growth Conditions
  - 1550 - 1650°C
  - 76 torr
  - 25 - 46 mm/hr
  - dichlorosilane/propane/HCl

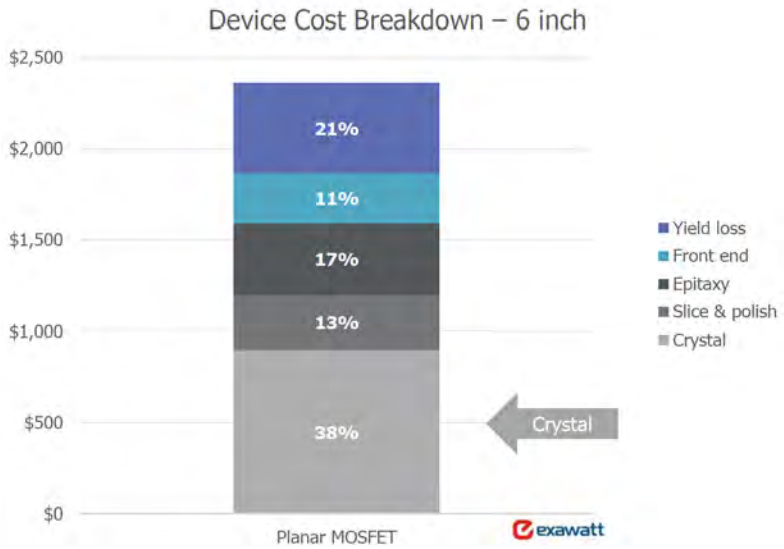
Both platforms are proven to be highly successful for SiC epi production

Slide courtesy of Warren Weeks, CREE Wolfspeed

The SiC Wafer Represents 50-70% of the SiC Device Cost



- DuPont sells its SiC wafer business to Korea's SK Siltron
- STMicroelectronics acquires Norstel
- Infineon acquires Siltectra "Cold split" to split crystalline materials efficiently with minimal material loss
- ON-semiconductor acquires GT Advanced
- Pallidus sells SiC boules and wafers
- Aymont sells Physical Vapor Transport SiC growth systems and source powder



Wafer represents 68% of SiC device cost
(Aixtron presented similar numbers in 2019)

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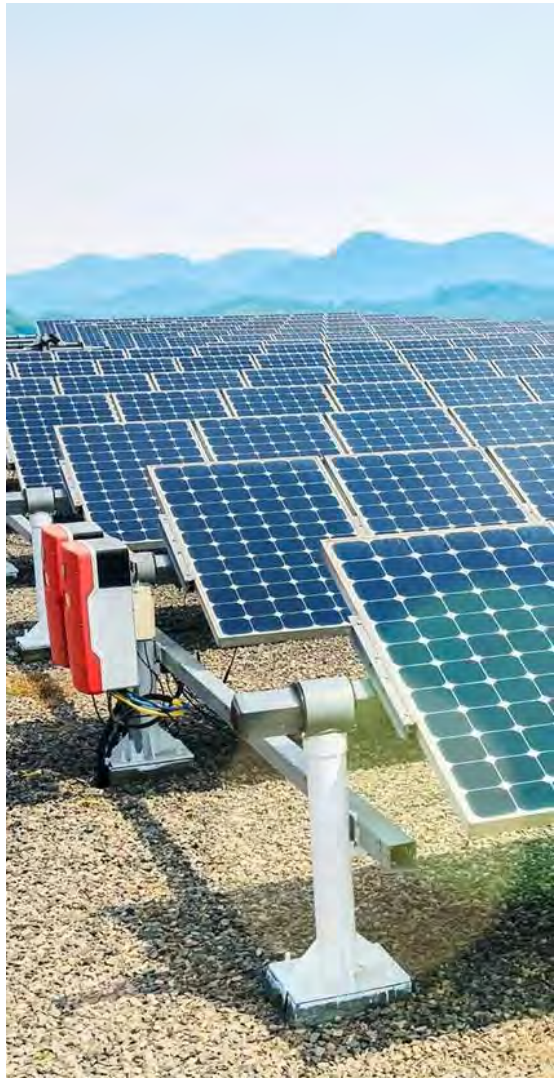
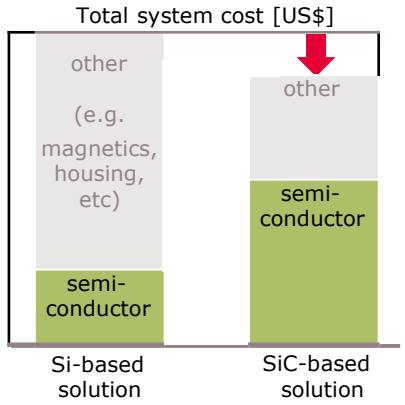
SiC Wafer production is dominated by U.S. CREE-Wolfspeed and II-VI

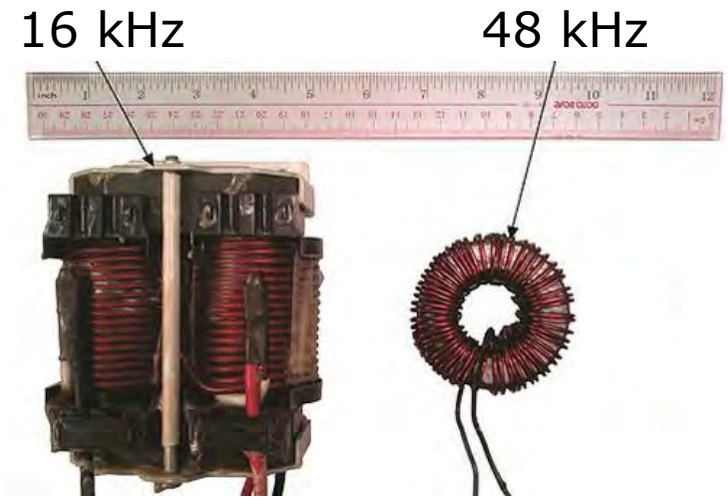
SiC MOSFETs Can Reduce System Cost (and Weight/Volume) Despite Their Higher Than Si Price



PV Reduction of system cost and size with SiC

- 10-15% lower BOM
- 2-3x higher semiconductor costs

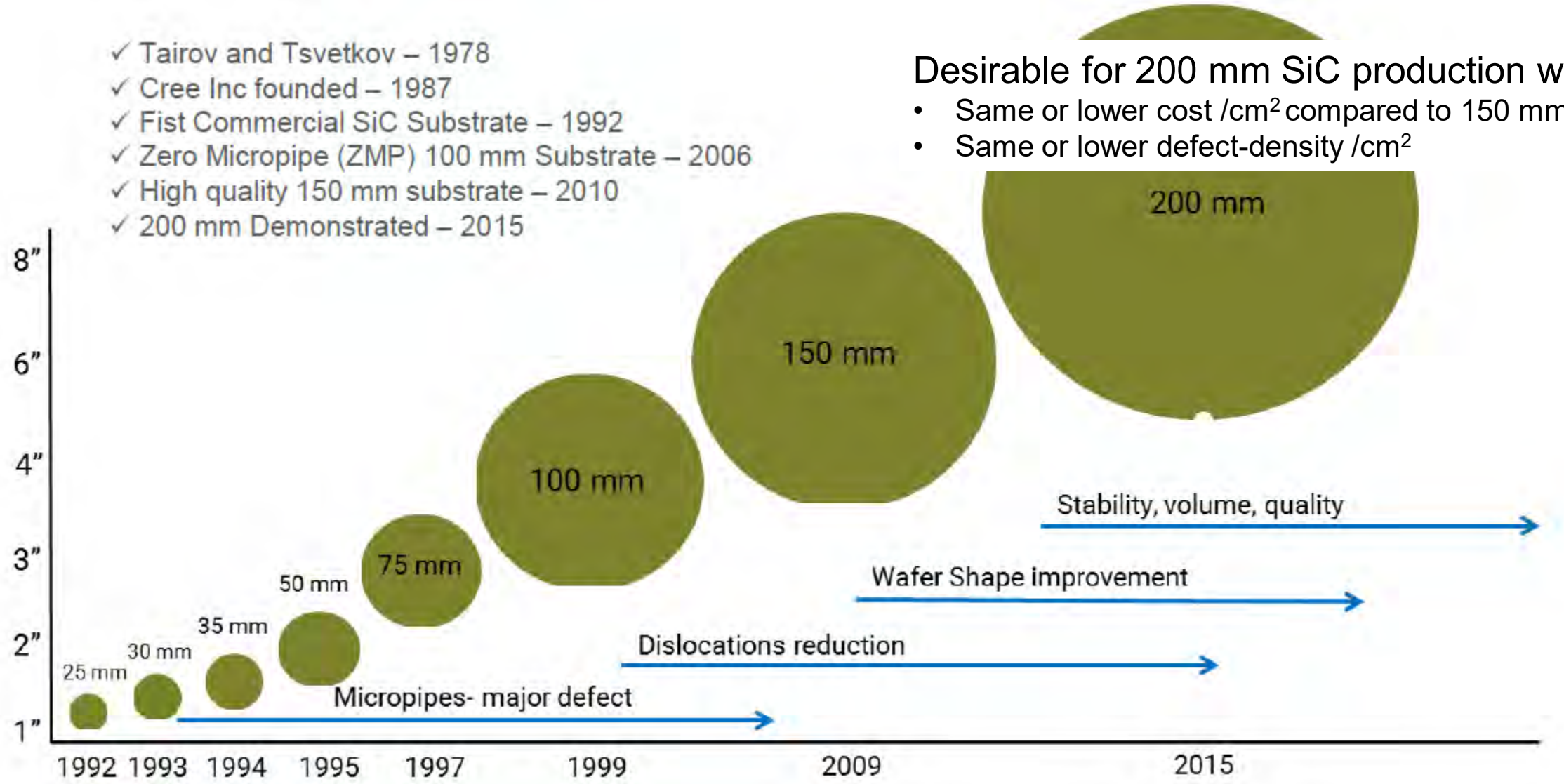




At 5kW Power

Courtesy:
Dr. Levett, Infineon

Demonstrated in 2015, 200 mm SiC Production Wafers Can Reduce Device Cost by >20%



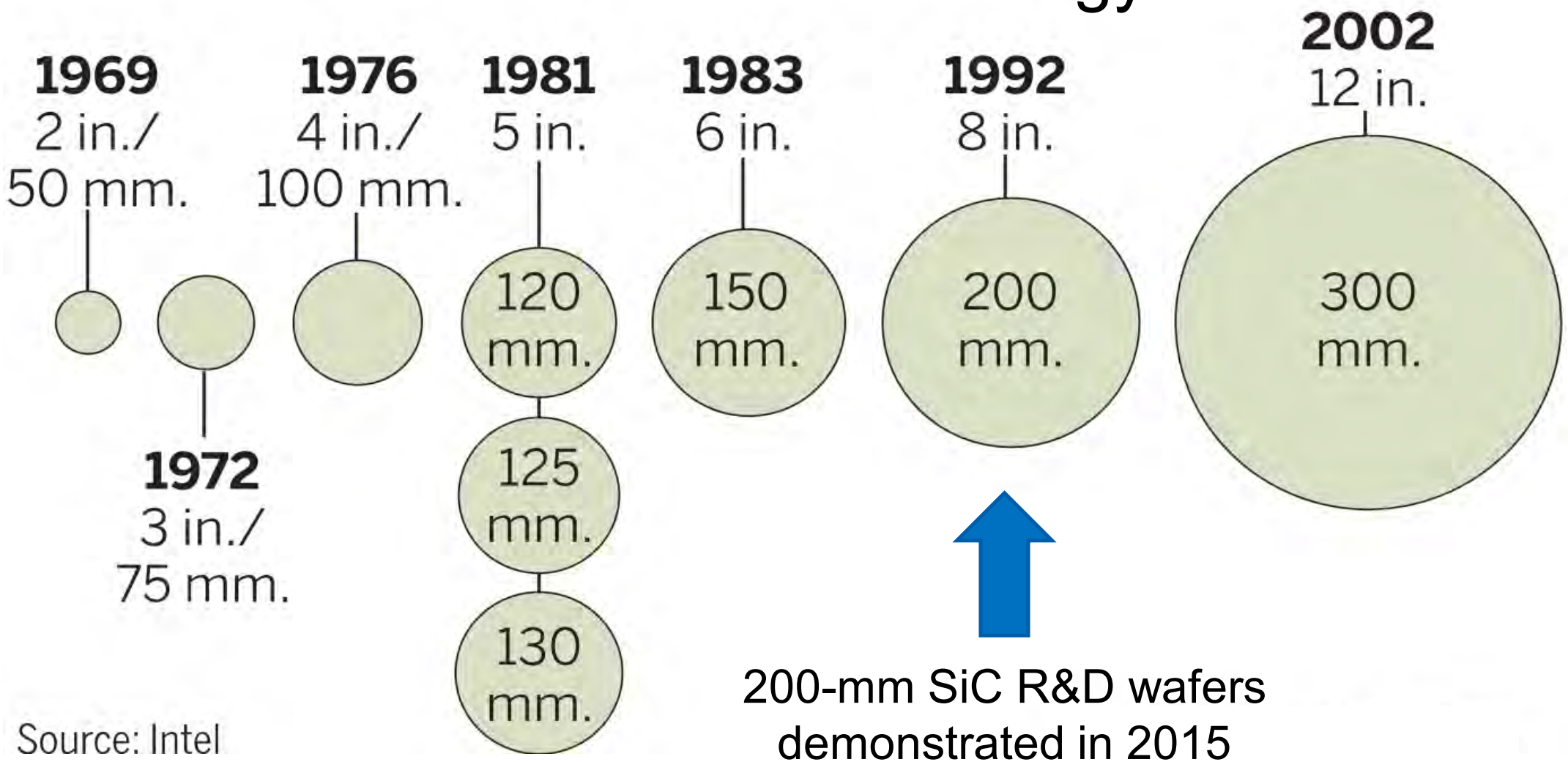
Desirable for 200 mm SiC production wafers:

- Same or lower cost /cm^2 compared to 150 mm wafers
- Same or lower defect-density /cm^2

Slide courtesy of Warren Weeks, CREE Wolfspeed

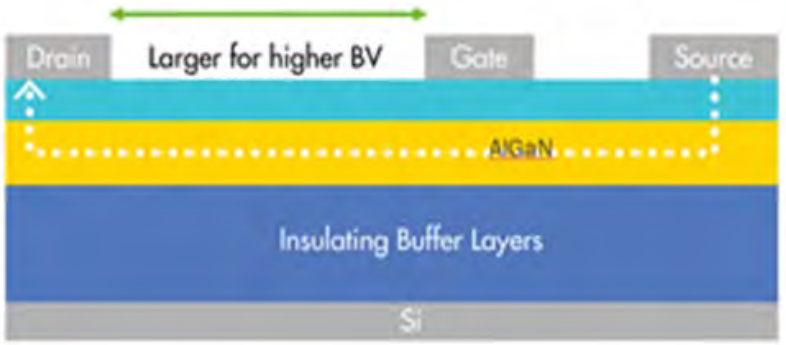
Extensive Semiconductor Fab Infrastructure is Available to Fabricate 200 mm Wafers

Si Wafer Size Chronology

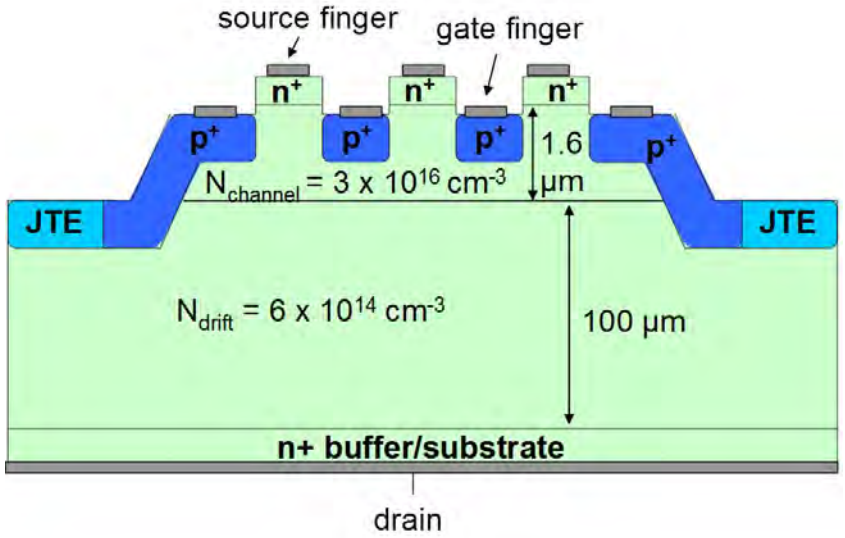


200-mm SiC R&D wafers demonstrated in 2015

High Voltage (+900 V) SiC Power Devices are Typically of Vertical Configuration



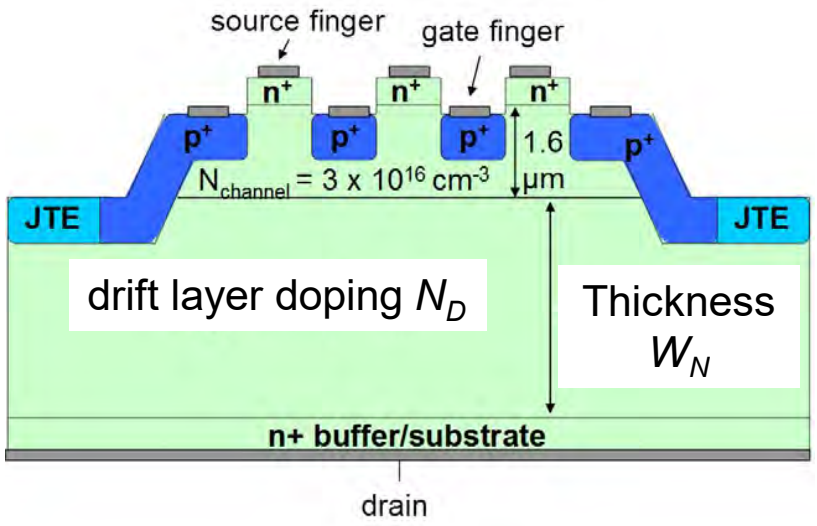
Lateral devices have system integration advantages but necessitate impractically large areas for high blocking voltage capability



Vertical device drift layer thickness can be tailored for high blocking voltage with no corresponding device area increase

- Lateral devices with high blocking voltage capability necessitate large areas because of the required large drift length (defined as the gate to drain spacing)
- For surface stability, adequate separation between high and low voltage electrodes in lateral devices results in higher cell pitch and R_{on}

The Ideal Blocking Voltage of a SiC Device is Determined by the Thickness and Doping of its Drift Layer



Optimal punch-through values for ideal drift region of unipolar devices, assuming high doping concentration on one side and low uniform doping concentration on the other side:

$$W_N = \left(\frac{3}{2}\right)\left(\frac{V_B}{E_C}\right) \qquad N_D = \left(\frac{2}{3}\right)^2 \frac{\varepsilon_S E_C^2}{2qV_B}$$

$$R_{ON,SP} = \frac{W_N}{q\mu_N N_D} \qquad R_{ON,SP} = \left(\frac{3}{2}\right)^3 \frac{V_B^2}{\mu_N \varepsilon_S E_C^3}$$

Theoretical breakdown voltage and measured resistance values:

Drift 11.7 μm, 3.5 10^{15} cm^{-3}: 2.2 kV*, 5.7 mΩ cm^2

Drift 100 μm, 6 10^{14} cm^{-3}: 13.6 kV*, 104 mΩ cm^2

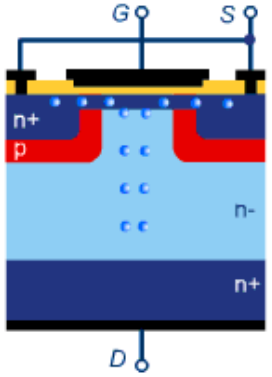
- To lower the on-state resistance of the low-doped thick drift regions of high voltage devices, bipolar current flow is materialized through carrier injection.
- Edge termination structures are implemented in SiC devices to achieve breakdown voltages close to the theoretical material limit.

*Drift layer theoretical limit calculated using: A. O. Konstantinov, Q. Wahab, N. Nordell, and U. Lindefelt, "Ionization rates and critical fields in 4H silicon carbide," *Appl. Phys. Lett.*, vol. 71, no. 1, pp. 90–92, Jul. 1997.

Voltage and Switching Frequency Requirements Drive Unipolar vs. Bipolar SiC Device Selection

Current flow in **unipolar** devices is due to only one type of charge carriers (electrons or holes) majority carriers.
Unipolar devices have higher conduction losses and lower switching losses.

MOSFET

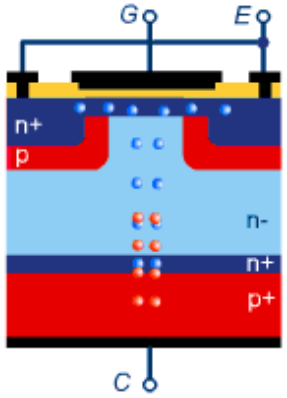


- During conduction, only one type of charge carrier flows: higher on-state resistance.
- Majority only conduction enables fast switching: lower switching losses

$$R_{on\text{-}sp} = \frac{W_D}{q\, N_D\, \mu_n}$$

Current flow in **bipolar** devices is due to both types of charge carriers, electrons and holes.
Bipolar devices have *lower conduction losses and higher switching losses.

IGBT



$$R_{on-sp} = \frac{W_{PT}}{q(\mu_n N_D + \mu_p N_P)}$$

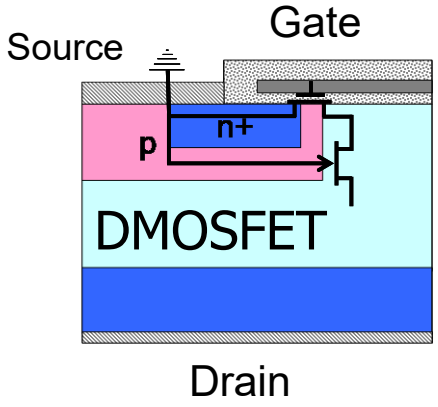
- During conduction, holes from the collector *p*+ region are injected into the *n*- region: the accumulated charge reduces on-state resistance.
- Bipolar conduction results in slower switching as minority carriers also need to be swept during transition: higher switching losses

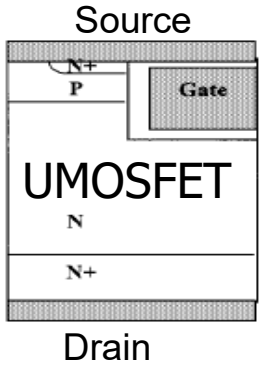
Typically in SiC: Unipolar devices to 10 kV, Bipolar Devices > 10 kV

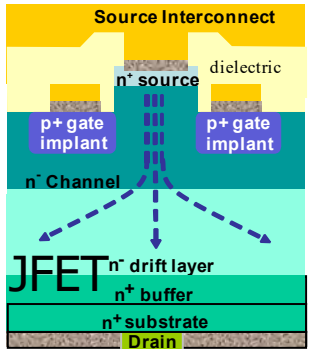
*The knee voltage of bipolar conduction contributes to bipolar device loss at low voltages

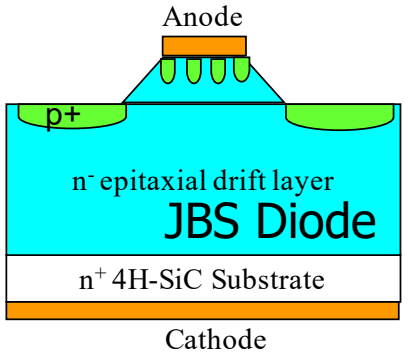
Multiple Power Devices have been Fabricated in SiC

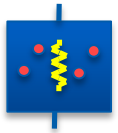
Unipolar devices: MOSFET, JFET, Junction Barrier Schottky Diode





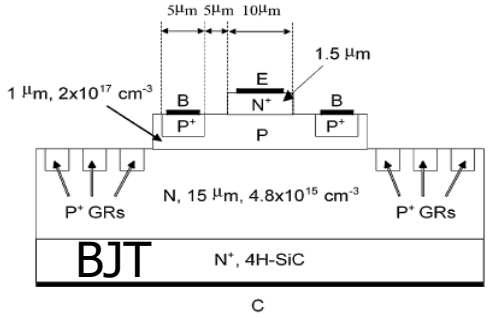


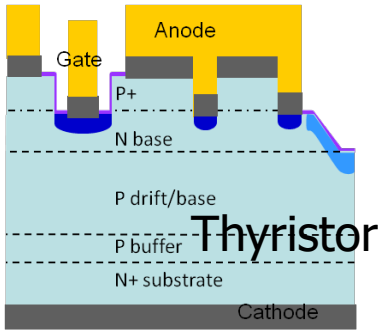


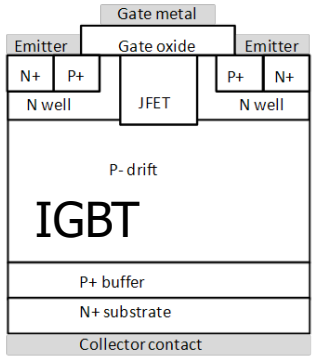


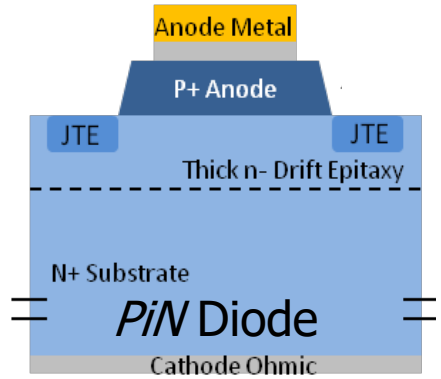
Electrons Only => Higher conduction losses, Faster Switching lower losses

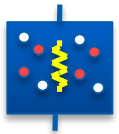
Bipolar devices: BJT, Thyristor, IGBT, PiN Diode





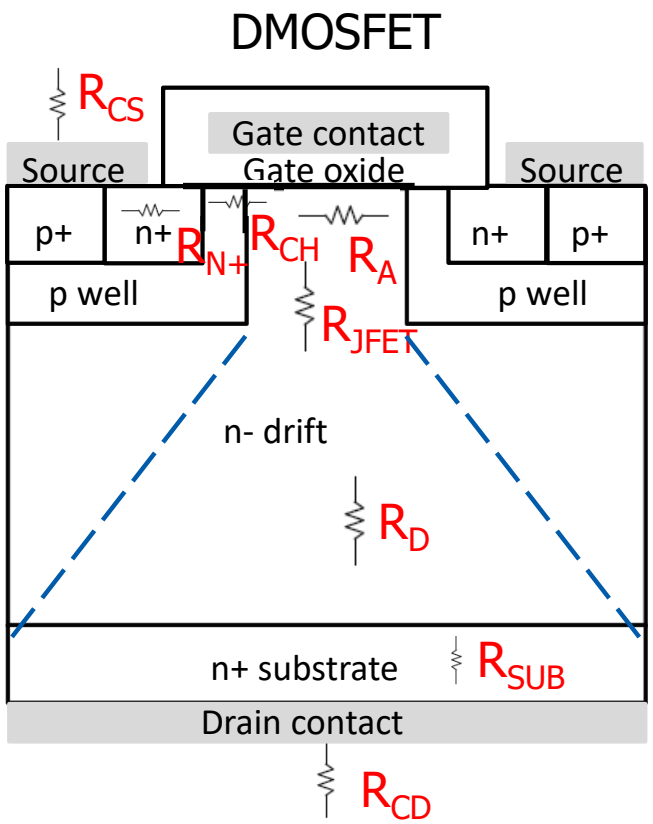


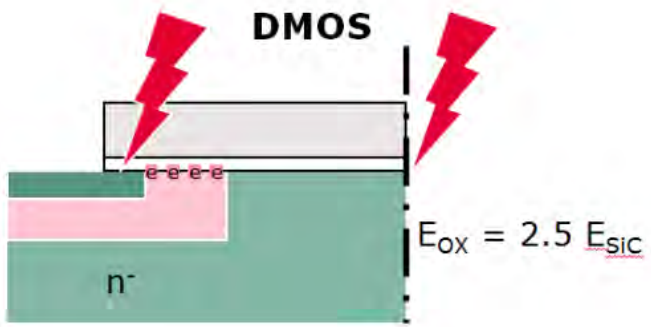


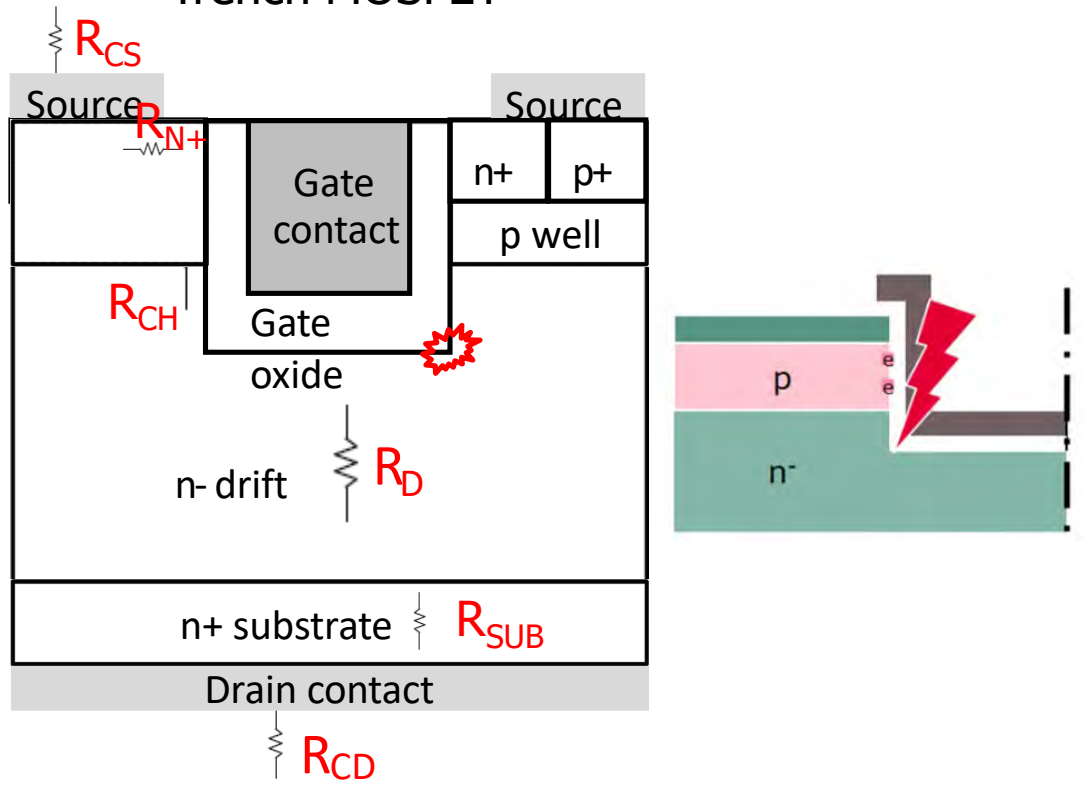


Electrons & holes => Lower conduction losses, Slower Switching higher losses

SiC MOSFETs are Commercially Available in Planar and Trench Configurations and are the Workhorse of Power Applications



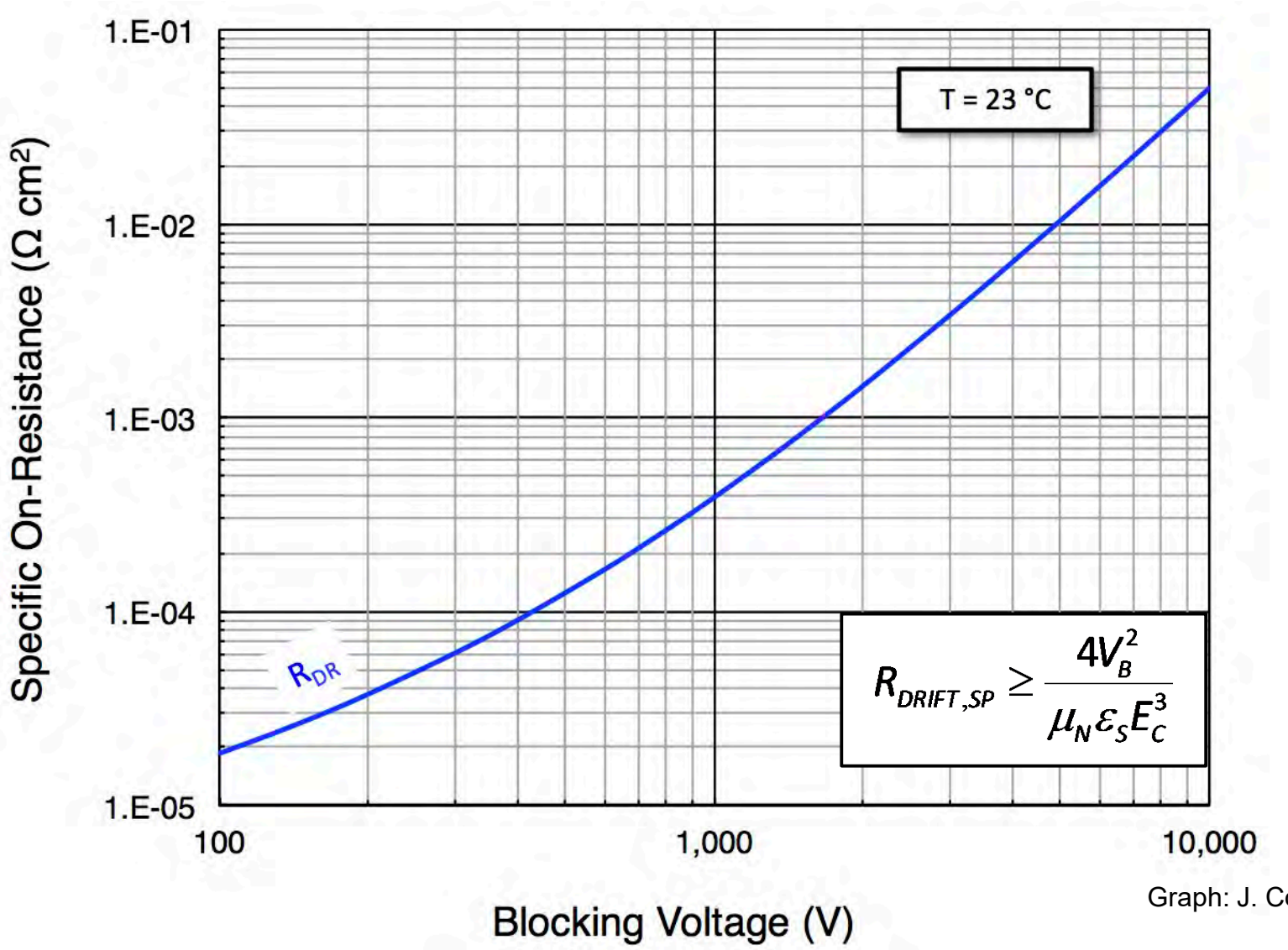


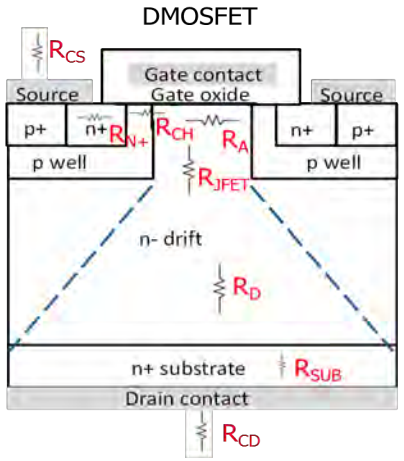


$$R_{ON,D} = R_{CS} + R_{N+} + R_{CH} + \mathbf{R_A + R_{JFET}} + R_D + R_{SUB} + R_{CD} \qquad R_{ON,U} = R_{CS} + R_{N+} + R_{CH} + R_D + R_{SUB} + R_{CD}$$

- ✓ The JFET region on-state resistance is eliminated in the Trench MOSFET (accumulation + JFET), the MOS mobility is higher on the vertical sidewall, and smaller cell pitch is possible
- Trench MOSFET blocking-voltage capability can be lower than that of DMOSFET (for same drift layer specs) due to electric field crowding at the trench corners of the gate oxide

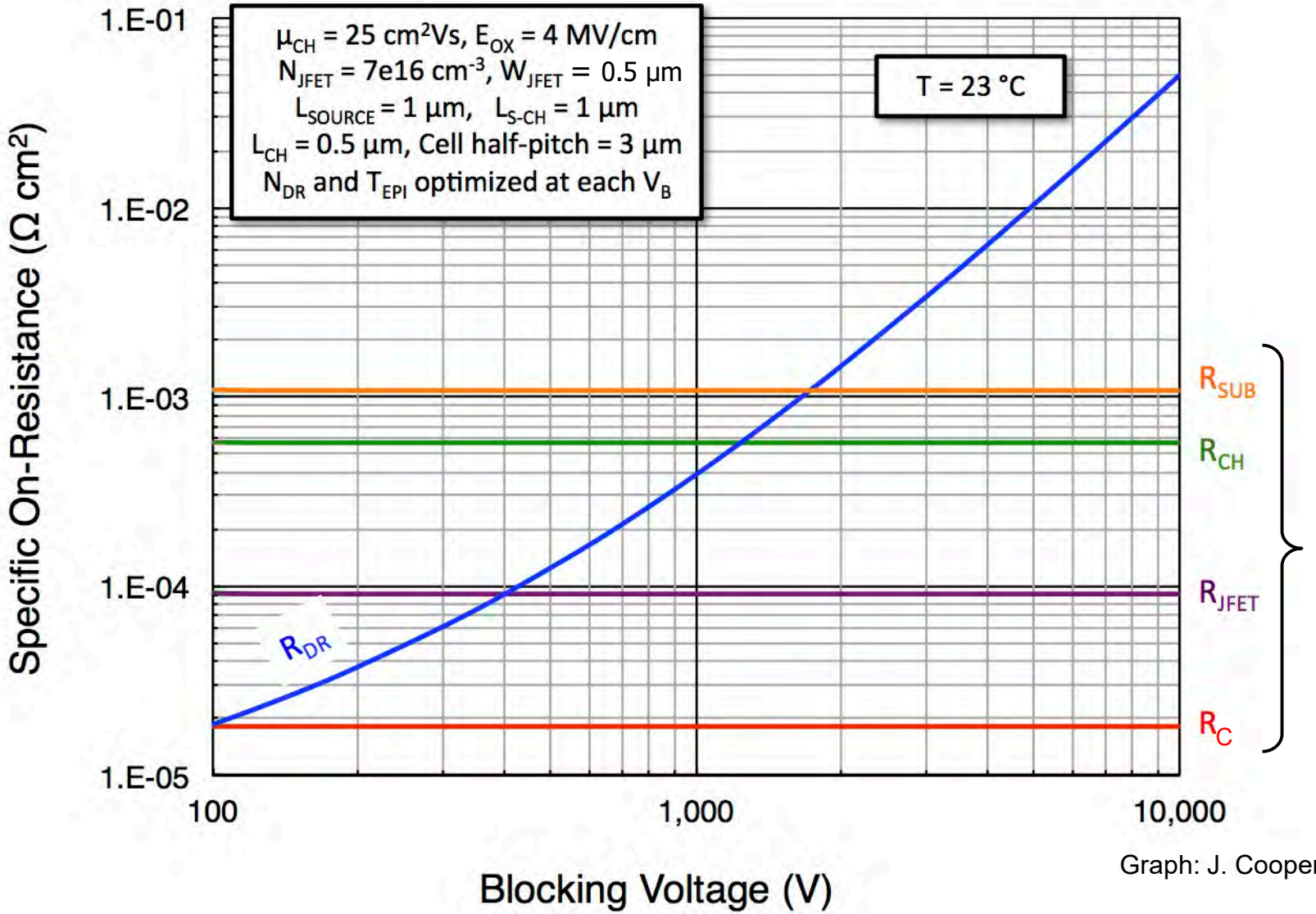
Components of MOSFET Specific On-Resistance

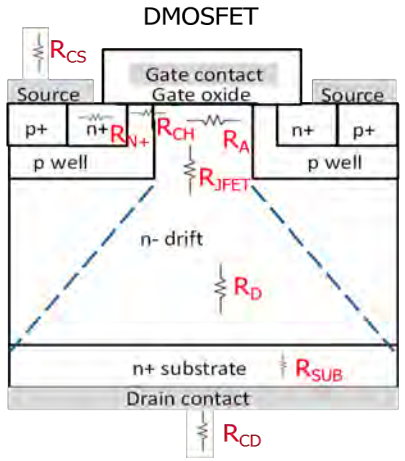




Graph: J. Cooper ECSCRM 2016

Components of MOSFET Specific On-Resistance

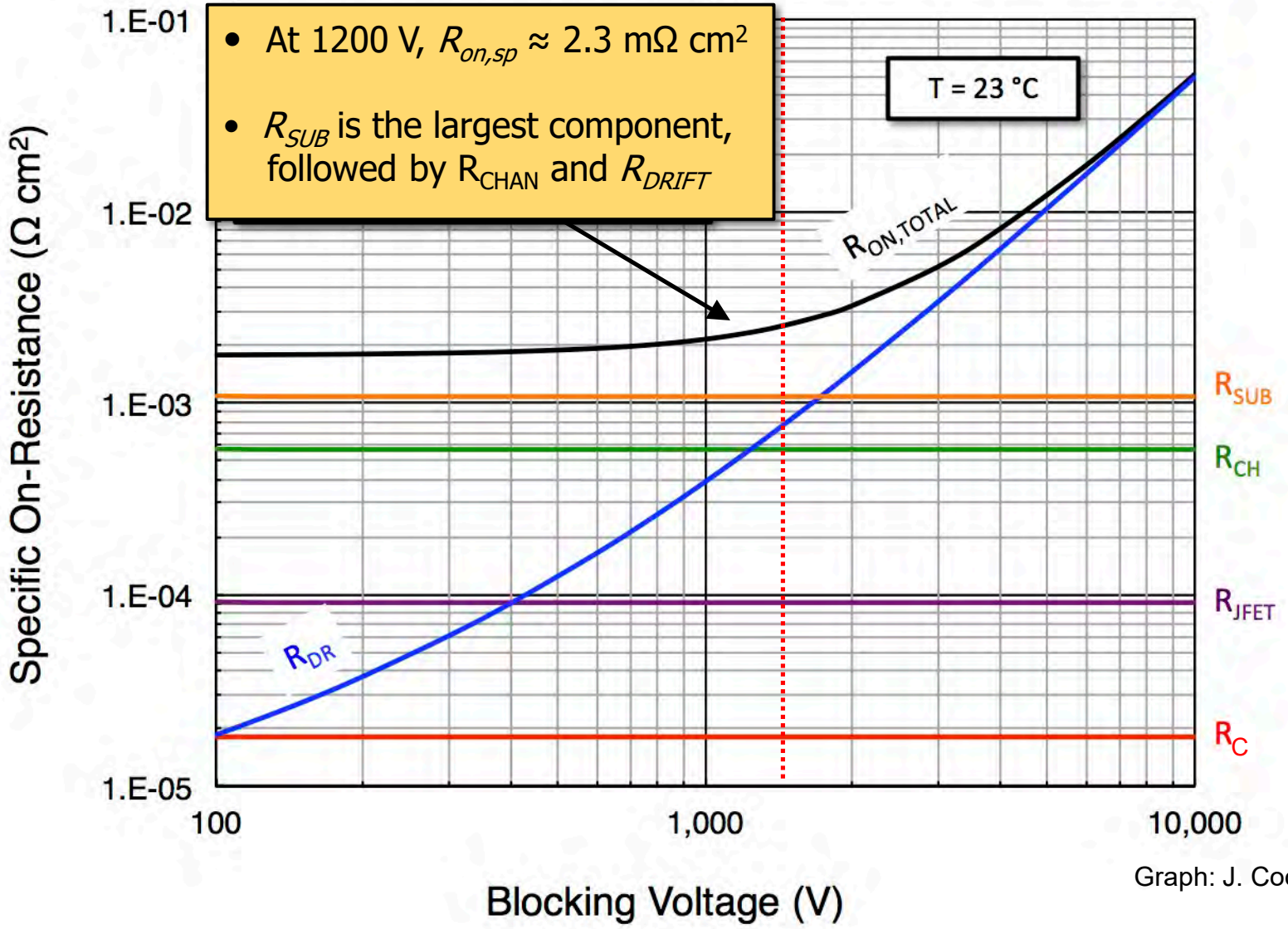


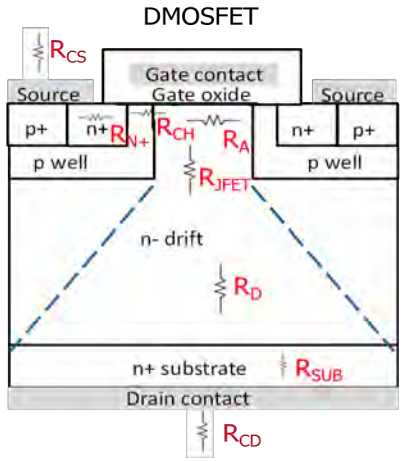


Independent of BV

Graph: J. Cooper ECSCRM 2016

Components of MOSFET Specific On-Resistance





Graph: J. Cooper ECSCRM 2016

SiC Fabrication Requires Investment in Select Tools and Development of Specific Processes

POWERAMERICA

Multiple mature Si processes have been successfully transferred to SiC. However, SiC material properties necessitate development of specific processes, whose parameters must be optimized and qualified:

- **Etch**: SiC is inert against chemical solvents and only dry etching is practical. Masking materials, mask etch selectivity, gas mixtures, control of sidewall slope, etch rates, sidewall roughness, etc., need development.
- **Substrate thinning** for lower resistance or thick epi handling (material hardness requires special recipes). CMP for fine flatness control.
- **Doping**: Conventional thermal diffusion is not practical in SiC due to its high melting point and the low diffusion constant of dopants within SiC. Evaluate implantation species, dose, energy, temperature, masking materials, etc. Post implantation SiC recrystallization and implant activation anneal method (furnace, RTA, etc.), temperature, ramp rate, duration, gas flow, etc. Select anneal protective cap layer to minimize SiC wafer surface degradation. CMP can be used to flatten the wafers alleviating the impact of the high-temp anneal.
- **Metallization**: Evaluate CTE matched metals, select resist type and develop undercut lift-off profile, metal evaporation and lift-off, sputter metal deposition and dry etch.
- **Ohmic contact formation**: High value of SiC/metal barrier results in rectifying contacts. Post metal deposition anneal is required for Ohmic contacts. Optimize anneal temperature, ramp rate, duration, gas flow, maintain surface quality.
- **Gate oxides**: Poor SiC/SiO_2 interface quality reduces MOS inversion layer mobility. Develop passivation techniques to improve SiC/SiO_2 interface quality.
- **Transparent wafers** complicate CD-SEM and metrology measurements as focal plane is determined with the use of an optical microscope. Other tools need software/gain/hardware adjustments to move to wavelengths where SiC is opaque. SiC Metrology/Inspection tools needed.
- **Relative lack of flatness in SiC wafers** can complicate photolithography and other processing particularly of high voltage devices (thick drift epitaxial layers). High temperature processes can further degrade wafer flatness. CMP to flatten wafers at various stages of fabrication.
- **Insulation dielectrics**: Thick dielectrics are deposited in SiC. Evaluate impact of deposited dielectric defects on edge termination and device reliability.

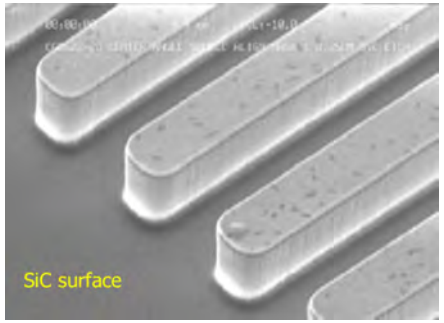
SiC Processing in a Si Foundry Requires a Modest Capital Investment in Additional Equipment

SiC Specific Equipment to be Installed in Si Foundry	
High Temp Anneal Furnace	Maximum Temp: 1950 °C
High Temp Implanter	Maximum temperature 700 °C
SiC Backgrind Tool	Wafer thinning
Backside Metal Deposition Tool	Ti/Cr/W/Mo/TiW/Ni
Backside Laser Anneal Tool (Si RTA works)	Backside ohmic contact formation
SiC substrate and epitaxy wafer surface defect inspection and metrology	Wavelength of operation compatible with transparent wafers (385 nm bandgap)

Processing SiC in “obsolete” fully-depreciated underutilized Si foundries requires a modest capital investment and provides the surplus wafer capacity to maximize the foundry’s utilization.

V. Veliadis

Etch: Reactive Ion Etching (RIE) is Commonly Used to Form Mesa Structures and Trenches in SiC



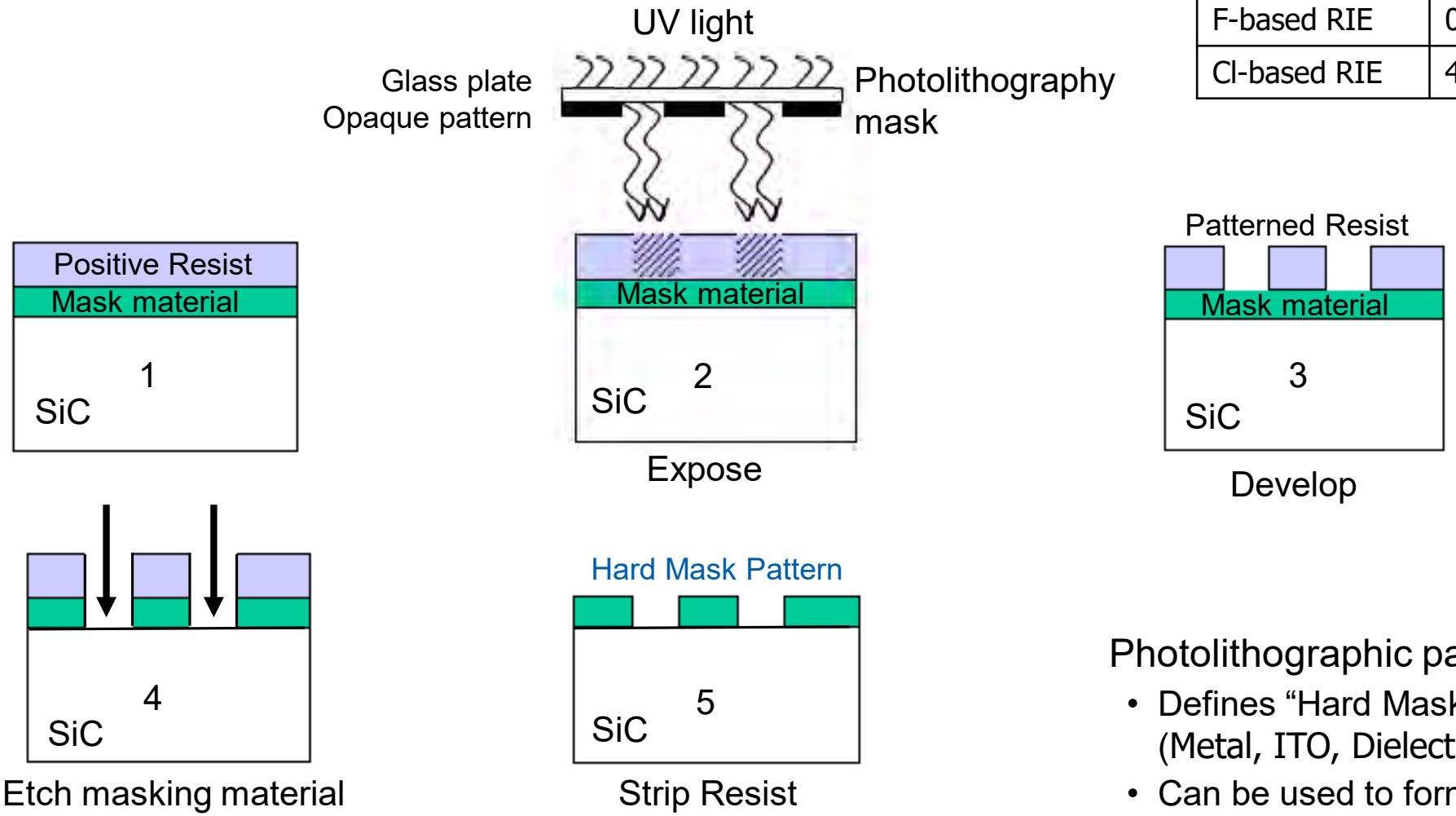
- Commercial RIE systems developed for Si can be used to etch SiC
- Etching gas systems are typically fluorine based, chlorine based, or bromine based
  - Fluorine based: SF_6, CF_4, NF_3, BF_3, CHF_3
  - Chlorine based: Cl_2, BCL_3, $SiCL_4$
  - Bromine based: Br_2, IBr
- Etching rates are relatively low compared with those of Si
- O_2 and *Ar* are commonly used to enhance removal of carbon atoms promoting the etching
- Pressure, gas flows, and RF power are adjusted to optimize etch
- Inductive coupled plasma RIE has increased etch rate over traditional RIE (used for deeper etches)
- Photoresist masks have low SiC selectivity; *Al* and *Ni*, *ITO*, and SiO_2 masks are used

Mask	SiO_2	Al	Ni	Resist	ITO
F-based RIE	0.8-3	5-30	>50	<0.5	10-20
Cl-based RIE	4-15	2-10	–	<0.8	3-10

- *Al* mask RIE forms non-volatile Al_2O_3, which can be adsorbed on the etch surface and act as a micro-mask leading to significant surface roughening
- Micro-masking is reduced with H_2 gas flow but etch rate and selectivity degrade

Etch: Low Photoresist SiC Selectivity Requires Lithographic Patterning of "Hard Mask" for SiC Etch

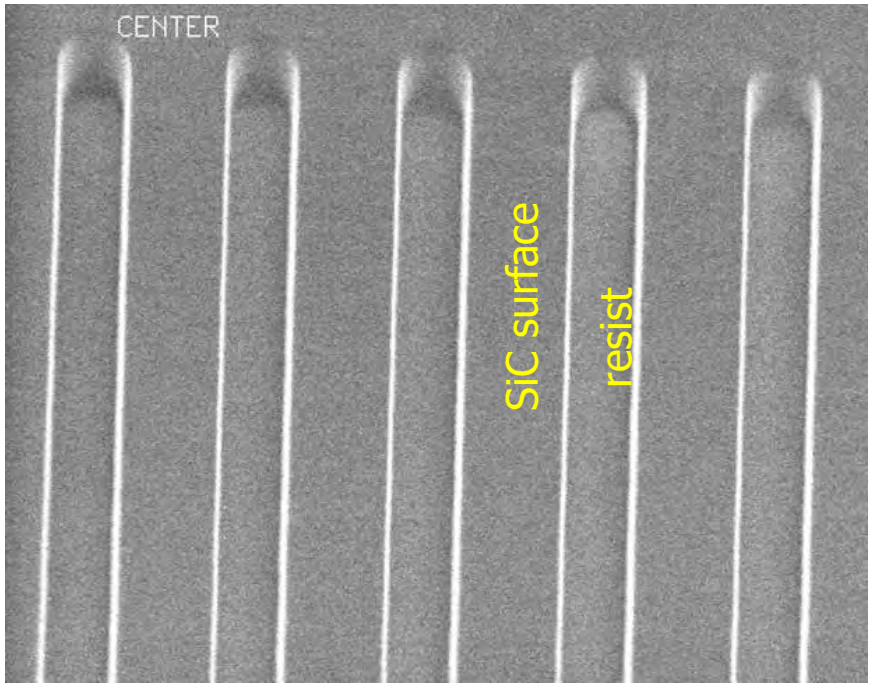
Mask	SiO_2	Al	Ni	Resist	ITO
F-based RIE	0.8-3	5-30	>50	<0.5	10-20
Cl-based RIE	4-15	2-10	—	<0.8	3-10



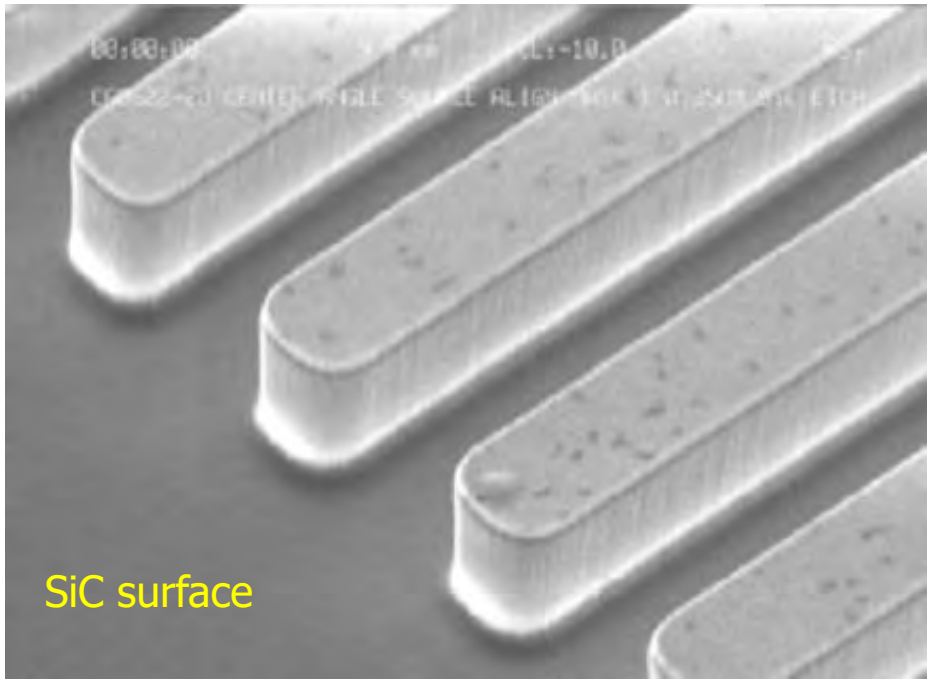
Photolithographic patterning and etch:

- Defines "Hard Mask" for SiC etch (Metal, ITO, Dielectric)
- Can be used to form etched metal patterns

Etch: RIE Using a *Cr/Al* Mask Produces 0.7 µm Deep SiC Vertical Sidewall Trenches for Implantation

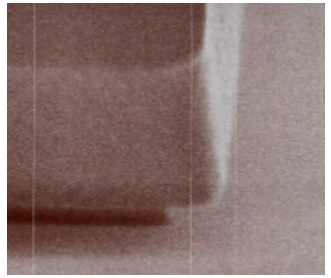


Patterned resist for *Cr-Al* mask formation



Vertically etched 0.7 µm deep SiC Mesas

- *Cr* assists with adhesion of metal layers to SiC surface
- Re-entrant (undercut) bi-level resist profile ensures “clean” *Cr-Al* lift-off
- RIE settings optimized for elimination of micro-masking, and vertical sidewall profile formation
- Vertical sidewall profile minimizes undesirable sidewall implantation.
- Crystal orientation dependent SiC oxidation rate can be exploited to further protect against unwanted sidewall implantation.

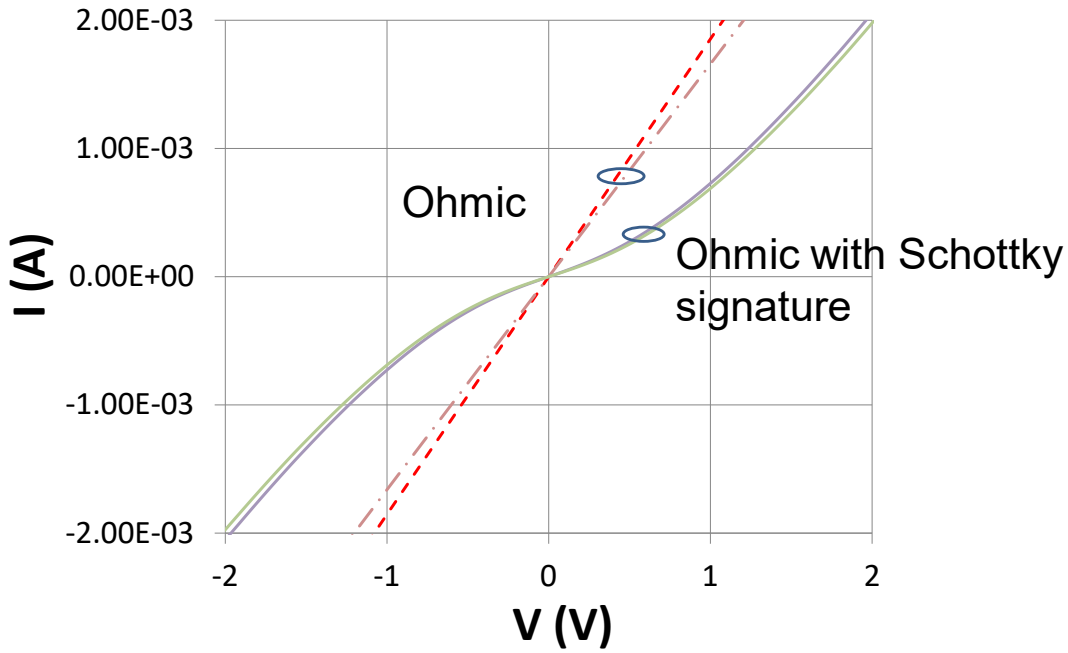


Bi-level resist profile for metal lift-off

V. Veliadis

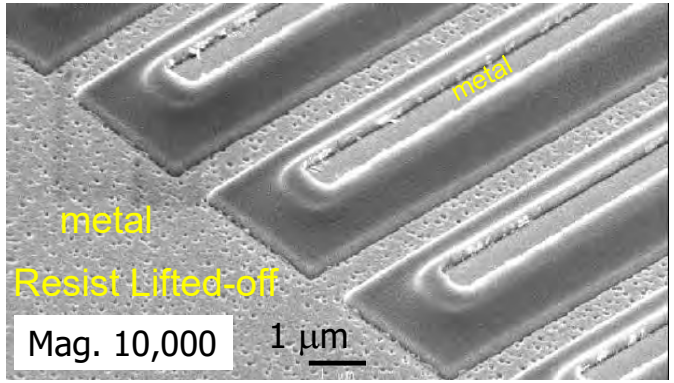
Ohmic Contact: SiC Metal Contacts are not Ohmic after Deposition Due to the High Schottky Barrier Height

To form a low resistivity semiconductor/metal Ohmic contact, a metal having a low Schottky barrier with the underlying semiconductor must be selected

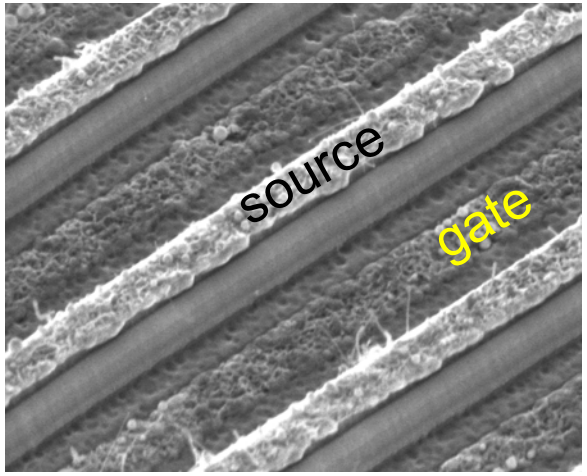


- A consequence of the wide SiC bandgap is the high Schottky barrier height at the SiC/metal interface after deposition.
- To form Ohmic contacts in SiC, post metal deposition annealing at 900-1000 ºC is typically performed. Reaction of the metal with SiC reduces Schottky barrier height or thickness.
- A heavily doped SiC/metal interface creates a thinner barrier for carrier tunneling (contacts).
- *Ni* is commonly used in the formation of *n*-SiC/metal contacts.
- Ohmic contact formation is more difficult in *p*-SiC/metal due to the higher Schottky barrier height. *Al/Ti* alloys are commonly used in the formation of *p*-SiC/metal contacts.

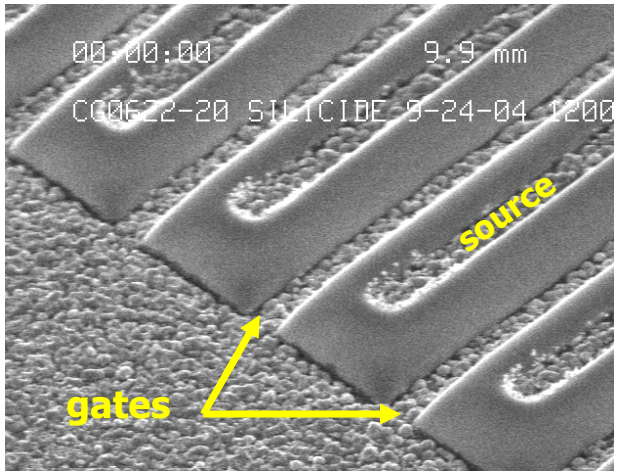
Ohmic Contact: Simultaneously Forming Low-resistivity *Ni*-silicide Ohmic Contacts to Both *n*-type and *p*-type Simplifies Fabrication



Ni prior to RTA silicidation

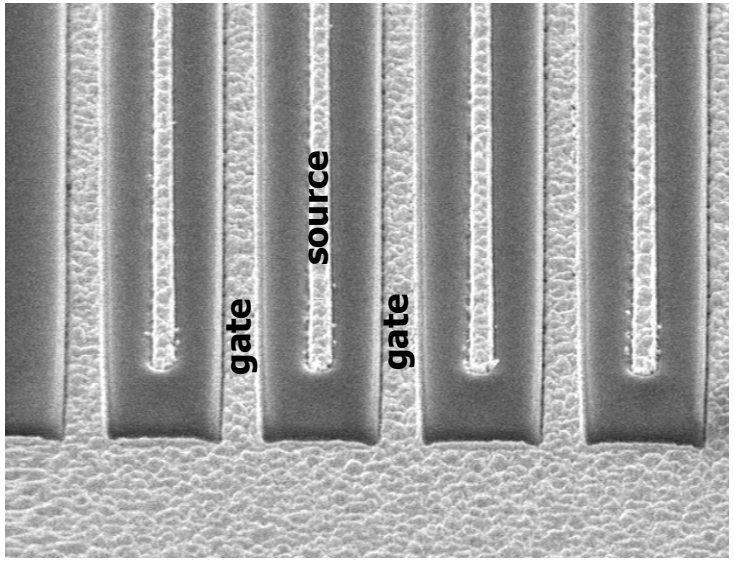


Ni silicide with metal strings



Ni silicide with no metal strings

- Thick *Ni* layers suffer from roughness while thin *Ni* layers are relatively resistive. 50-100 nm *Ni* thickness is a good compromise.
- 900-1000 °C RTA sintering at optimized ramp rate creates smoother lower-resistivity Ohmic contacts.
- Subsequent thick overlay metal deposition reduces surface roughness and accommodates wire bonding.
- *n*-source and *p*-gate (5.9 10^{-4} Ω cm^2) Ohmic contacts are formed simultaneously.



Thick interconnect metallization

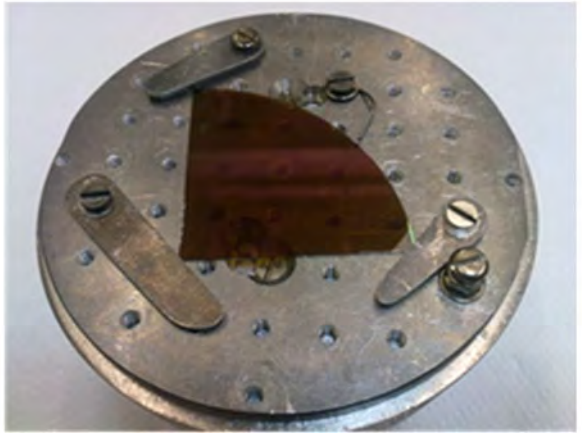
Implantation: Ion-Implantation is the Practical SiC Selective Doping Technique Followed by ~1600 °C Furnace Annealing

- Diffusion doping is not realistic in SiC because of its strong chemical bonding that results in negligible dopant diffusion below 1800 °C. Lack of masking materials and defect generation at >1800 °C make ion implantation the exclusive SiC manufacturing doping method.
- SiC implantation is typically performed at elevated temperatures to minimize crystal lattice damage from ion bombardment, particularly for the high doping densities required for good Ohmic contact characteristics.
- Room temperature implantation works well for low implant doses (< 10^{15} cm^{-2}).
- Doping densities of 10^{19}-10^{20} cm^{-3} are required for Ohmic contact formation.
- Implant profiles can be predicted by Monte Carlo simulations such as SRIM (stopping and range of ions in matter), and verified by SIMS (secondary ion mass spectroscopy).
- Post implantation anneal at 1600-1800 °C is required for lattice damage recovery, and high dopant electrical activation ratios (~95%).
- Standard on-wafer test structures such as van der Pauw/Hall effect and C-V provide sheet resistance, carrier density, mobility, depth profile, and doping density.
- The as-implanted depth profiles are retained after the 1600 °C anneal for Al, P, and N as expected from their low diffusion constants. The lack of diffusion makes it easy to form shallow junctions and difficult to form deep ones.
- Boron is typically not used in device fabrication due to its higher implantation related defect generation, and the higher ionization energy of its acceptors that hampers the formation of low resistance p-type SiC.

Implantation: Protective Cap Layer Post Ion-implantation 1650 °C Furnace Annealing Produces Excellent SiC Surface Morphology

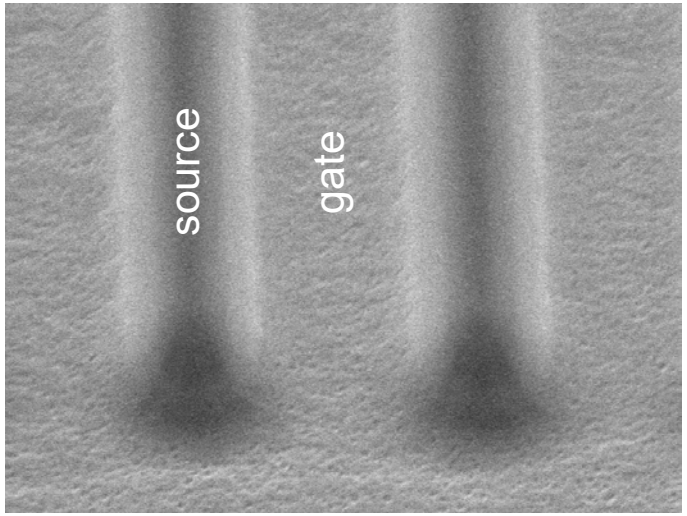
Heated SiC ion-implantation minimizes crystal lattice damage

*Before ion Implantation

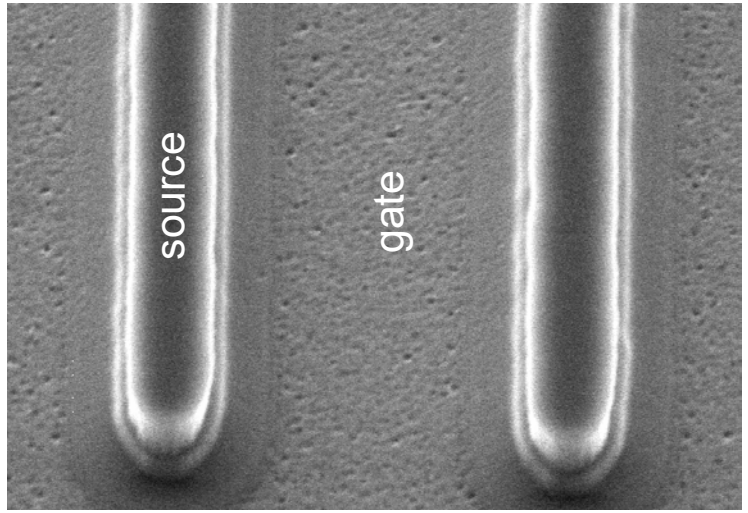


*After 400 °C ion implantation

1600 – 1700 °C implant anneal in *Ar* recrystallizes the SiC surface and electrically activates dopants



Post *p*+ ion-implantation anneal in absence of protective cap layer: surface degrades due to Si desorption and migration of surface atoms



Post *p*+ ion-implantation anneal with carbon protective cap layer: surface morphology is excellent

- SiO_2, Si_3N_4, AlN, BN/AlN, and carbon protective cap layers have been investigated
- Carbon cap gives best results. It can be formed by RF sputtering or graphitization of photoresist
- No chemical reactions occur at the SiC/carbon interface
- The carbon cap can be removed by ashing (O_2 plasma) or 700 – 800 °C oxidation

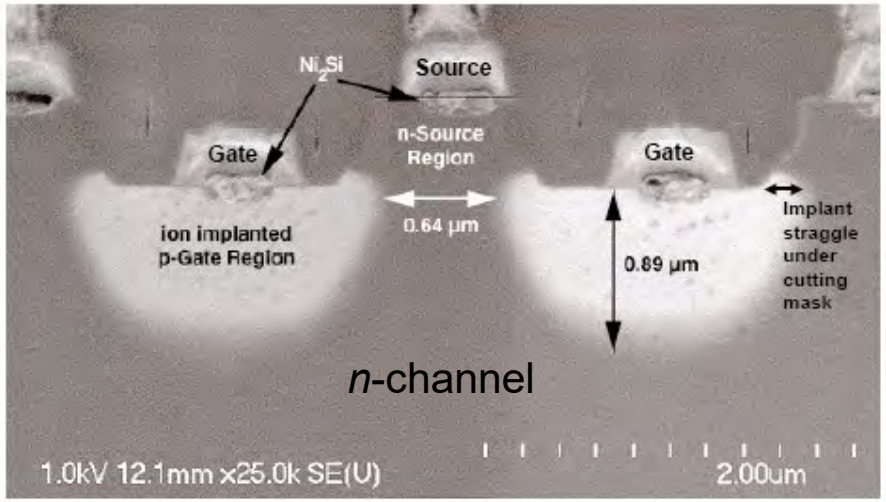
*Photos courtesy Dr. R. Nipoti

Implantation: Ion Implantation and Subsequent Annealing Can Generate Defects that Degrade Device Performance

Ion implantation and subsequent annealing defects include:

- Complex point defects
- Localized levels (shallow or deep)
- Extended defects (Basal plane dislocation loops and stacking faults)
- New dislocations and/or movement of existing dislocations

These defects can degrade device performance and are a reliability concern.

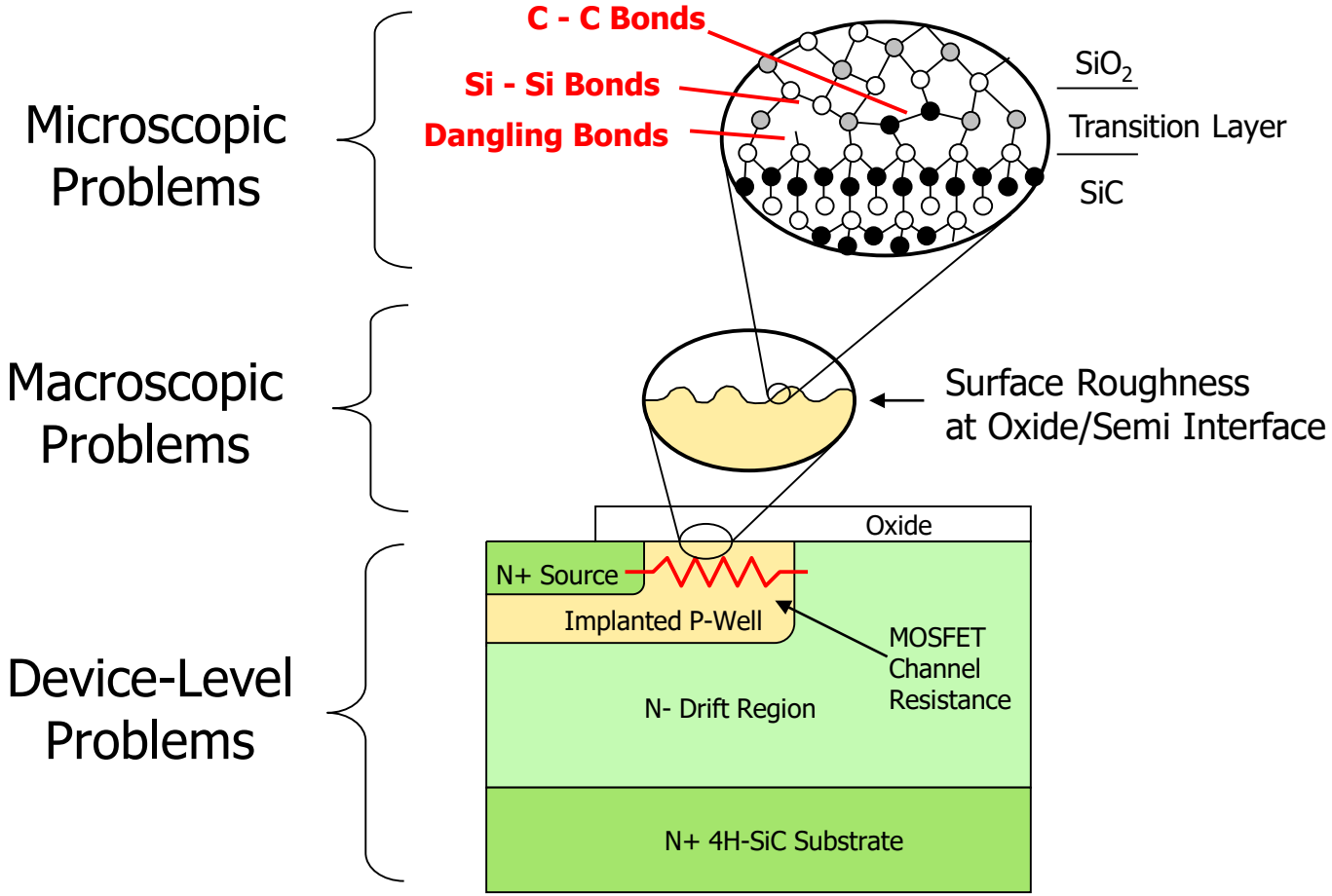


Cross sectional SEM image of heavily doped *p*+ implanted gate regions in *p*-channel. Lateral straggle of implantation undercuts mask.

Ion-Implantation process needs improvement:

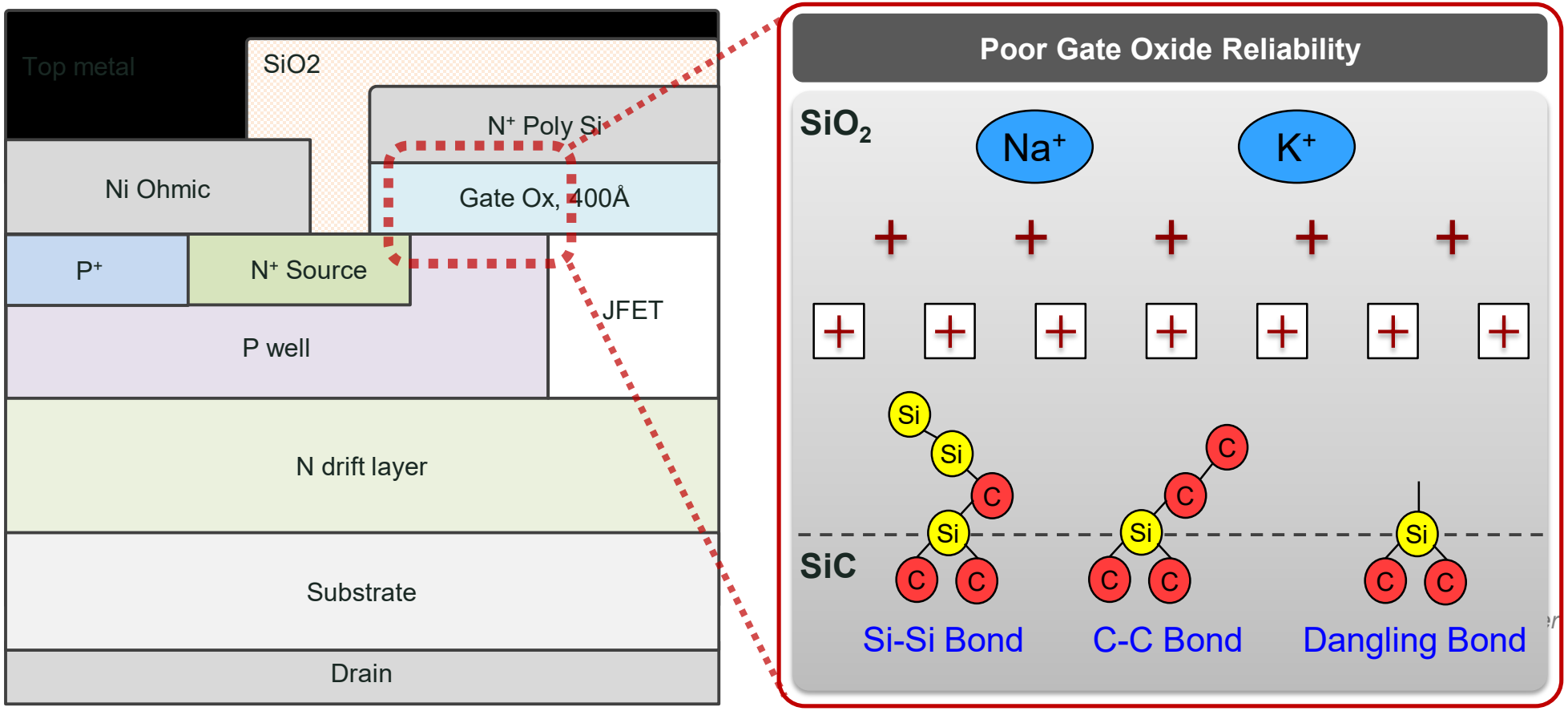
- Develop high quality room temperature heavy dose ion-implantation for manufacturability
- Optimize annealing ramp rate and overall implantation process to minimize defect generation
- Optimize ion-implantation and annealing to minimize impact on wafer planarity

Gate Oxide: Poor Quality of SiC-SiO_2 Interface Degrades Channel Mobility and Leads to Threshold Voltage Instability



Electrons tunnel from the conduction band into the oxide through the narrow barrier at the SiC-SiO_2 interface. Trapping of these electrons within the gate oxide degrades mobility and causes threshold voltage instability.

Gate Oxide: Threshold Voltage Instability in SiC MOSFETs is Due to Oxide Traps and Has Undesirable Consequences



Courtesy S. Yu
Ohio State University

Threshold Voltage (V_T) instability → **Positive** V_T Shift: Conduction loss
Negative V_T Shift: Normally-on

V. Veliadis

Gate Oxide: As in Si, the Gate Thermal Oxidation Process Involves Annealing in Nitrides

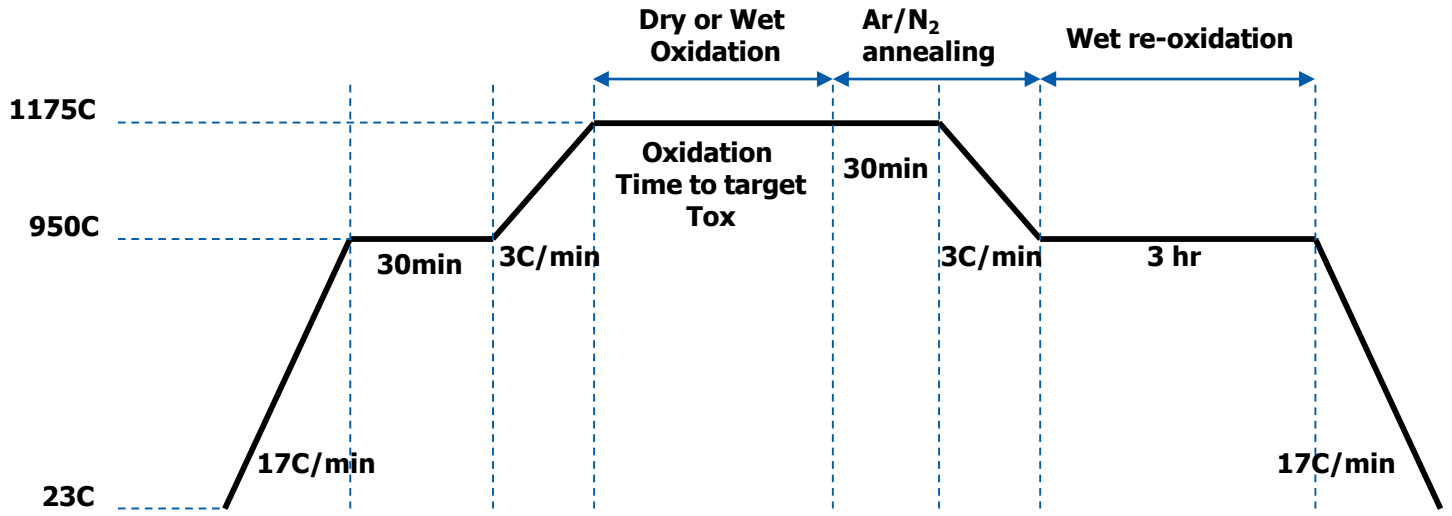
Annealing in inert gas (Ar/N_2 Post Oxidation)[1]

- Remove excess carbon on the oxide/interface[2]
- Improve dielectric properties and reliability[2]
- Carried out at the same oxidation temperature

Oxidation

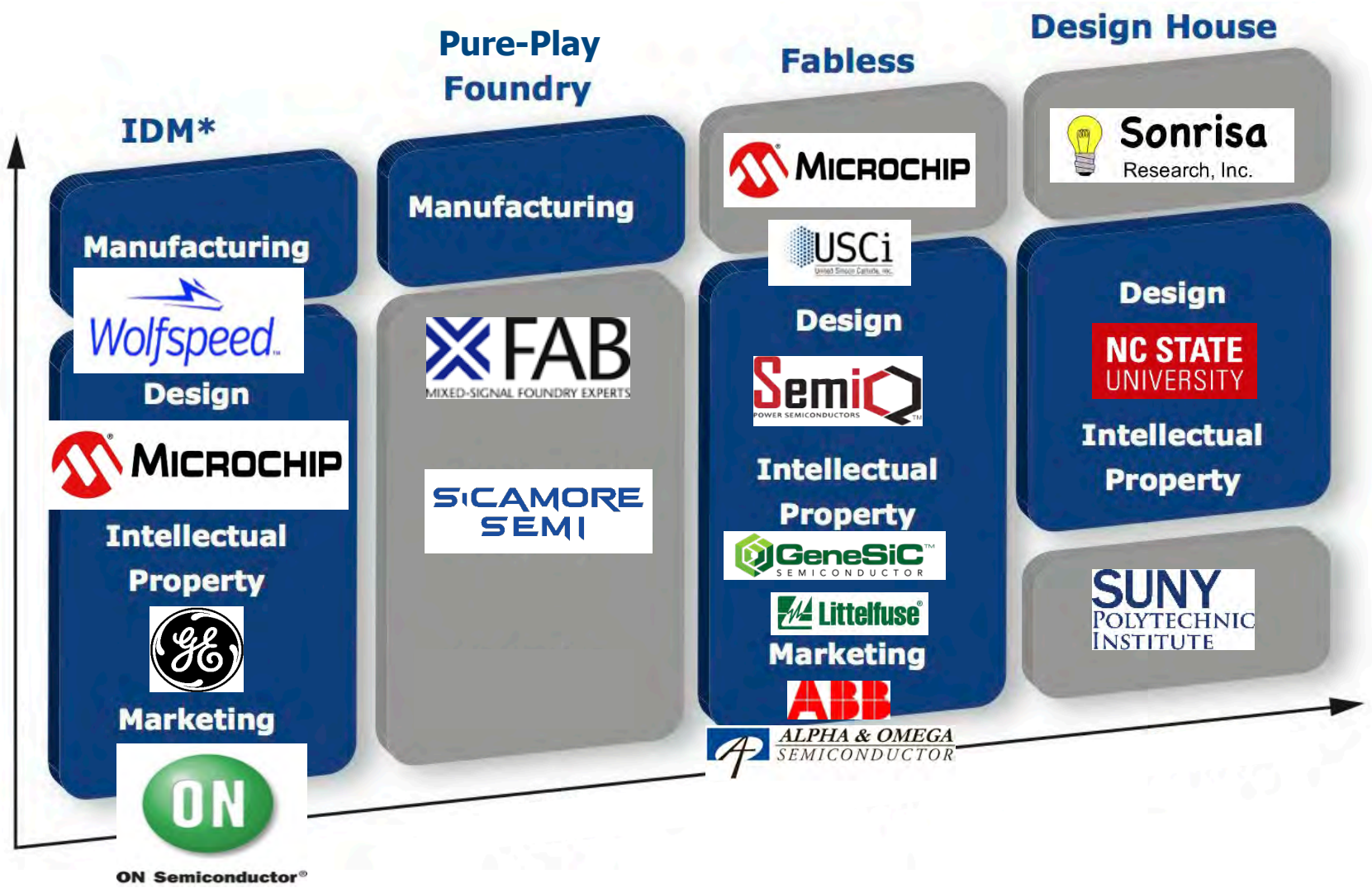
- Sacrificial thermal oxidation
- Wet oxidation at low temperature (950 °C)
- Additional oxidation is negligible
- Reduction of interface state density near mid-gap[3]
- Improvement of channel mobility
- Final D_{it} similar irrespective of dry or wet oxidation[4]

Courtesy: Prof. Woonje Sung



1. S. Wolf, R..N Tauber, Silicon Processing for the VLSI Era, vol.1, Lattice Press, California, 1986, pp. 222-223
2. J. N. Shenoy et, al, "Characterization and Optimization of the SiO2/SiC Metal-Oxide Semiconductor Interface," Journal of Electronic Materials, Vol. 24, No. 4, 1995
3. G. Y. Chung, et al, "Improved inversion channel mobility for 4H-SiC MOSFETs following high temperature anneals in Nitric Oxide," IEEE Electron Device Letters, Vol. 22, No. 4, April 2001
4. L. A. Lipkin, and J. W. Palmour, "Improved Oxidation Procedure for Reduced SiO2/SiC Defects," Journal of Electronics Materials, Vol. 25, No. 5, 1996

PowerAmerica Supports the Vibrant U.S. SiC Fab Infrastructure



SiC Foundry:

- Compete on Process in addition to Design
- Wafer quality and supply chain concerns

*IDM: Integrated Device Manufacturers

Si Foundry graph source: Successful Semiconductor Fabless Conference, Yole Mar. 2013

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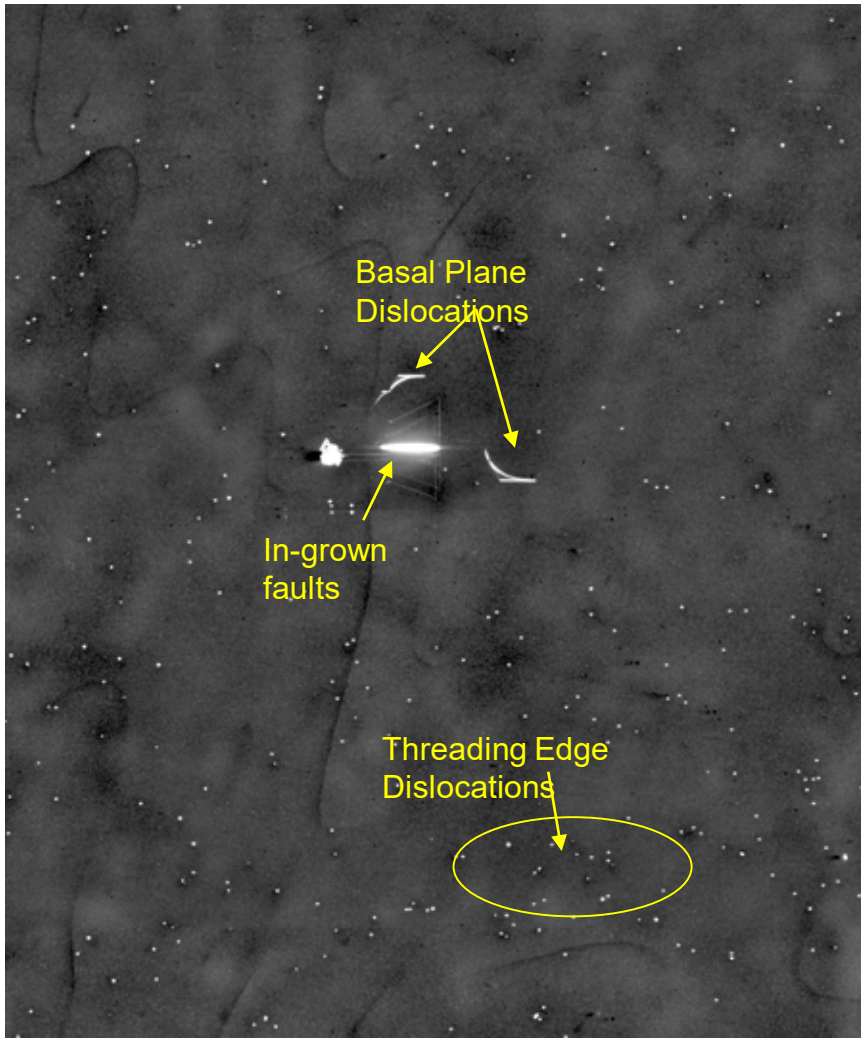
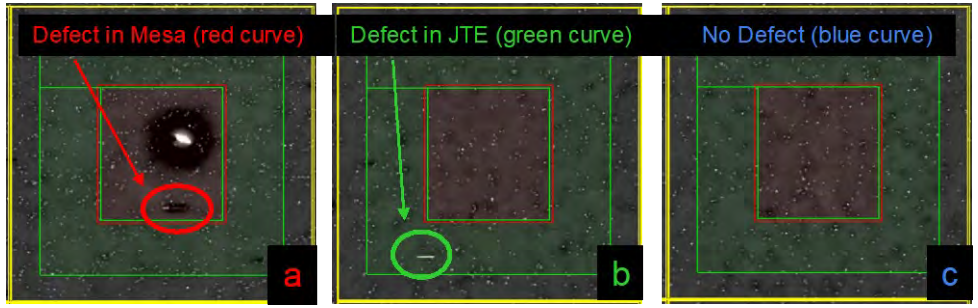
The Presence of Material Defects Degrade SiC Device Performance and Reliability, and Lower "Large Area Device" Yields

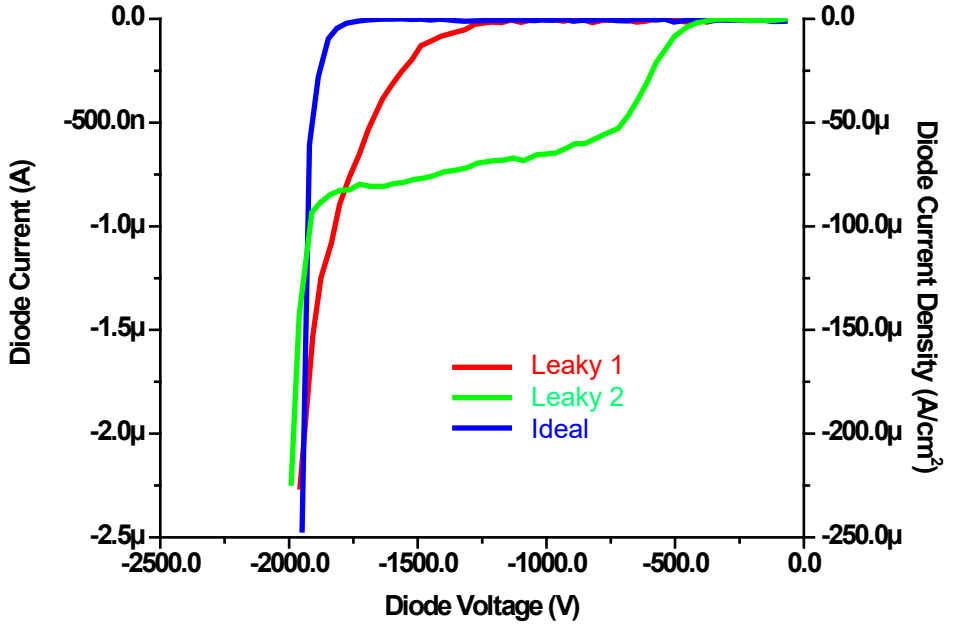


Portion of UV photoluminescence wafer map with various defects identified prior to fabrication

Courtesy of Bob Stahlbush, NRL

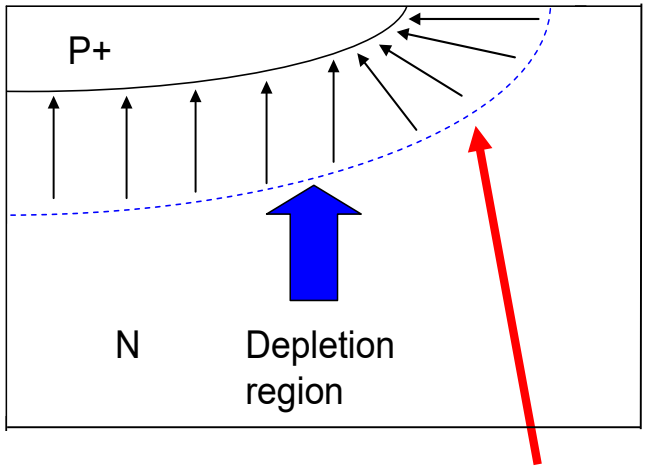


UV Photoluminescence maps with diode reticle overlay to show location of defects



2 kV *PiN* diodes from same wafer: leakage currents correlate to underlying defects

SiC Devices Exhibit Breakdown Voltages Below the SiC Material Limit due to Electric Field Crowding

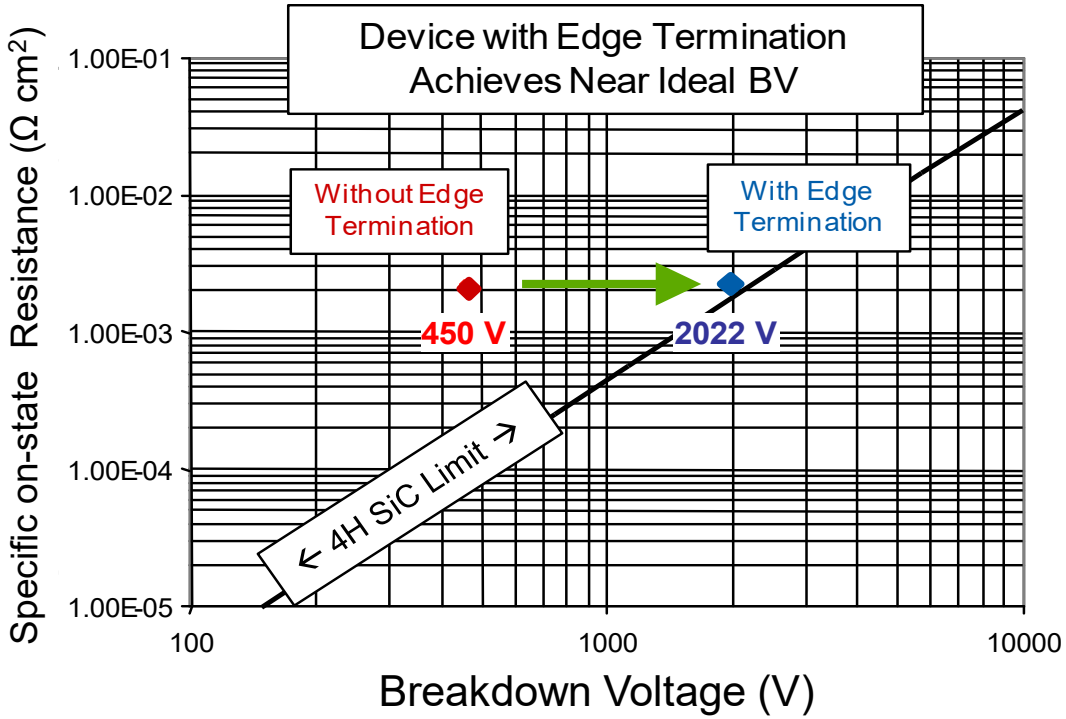


Electric field crowding at the edges of a power device limits blocking voltage to values below the SiC material limit (vertical drift capability)

450 V and 2022 V SiC devices on same wafer test die, have equal on-state resistance

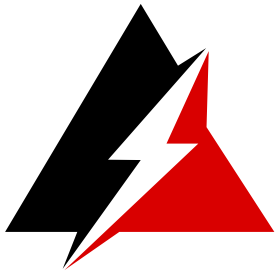
Common SiC Edge Termination techniques:

- Metal Field Plates
- Beveled Edge
- Floating Guard Rings
- Junction Termination Extensions



Edge Termination Maximizes Breakdown Voltage with no Associated Increase in Resistance

Thank you for your attention!



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