# SiC Power Device Reliability Power America WBG Short Course

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# BIO

Dr. Donald A. Gajewski is the Director of the Reliability Engineering & Failure Analysis Department for Wolfspeed, a Cree Company, covering GaN-on-SiC HEMT-MMICs for RF and microwave applications, SiC power MOSFETs, SiC Schottky power diodes, and SiC power modules. He has been in the semiconductor industry reliability profession for 21 years, with previous tenures at Nitronex, Freescale and Motorola. He has experience with other semiconductor technologies including highly integrated silicon CMOS including SiGe HBT and SmartMOS; magnetoresistive random access memory (MRAM); and advanced packaging including flip-chip and redistributed chip package (RCP). He completed a National Research Council Postdoctoral Research Fellowship at the National Institute of Standards and Technology, in the Semiconductor Electronics Division, in Gaithersburg, MD. He earned the Ph.D. in physics from the University of California, San Diego, partially under the auspices of a National Science Foundation Fellowship.

# JOURNEY / MILESTONES

## Timeline

POWER
RF
MATERIALS

**1987** — Cree Founded

**1991** — Released world's first commercial **SiC wafers**

**1993** — Listed on Nasdaq

**1998** — Created industry's first **GaN HEMT** on SiC, with record power density

**1999** — Demonstrated **4-inch SiC wafer** 4"

**2000** — Demonstrated industry's first **GaN HEMT MMIC**, grown on semi-insulating SiC substrate

**2002** — Released our first 600V commercial SiC JBS **Schottky diode**

**2006** — Released industry's first 1200V SiC **Schottky diode**

**2007** — Commercial release of **100mm, zero-micropipe SiC substrates**

**2008** — Announced sample release of 90W **GaN HEMT**

**2009** — Demonstrated record-efficiency **GaN HEMT Doherty amplifier** with digital pre-distortion

**2010** — Developed high-quality **150mm SiC substrates**

Released industry's first 1700V SiC **Schottky diode**

**2011** — Released industry's first SiC **MOSFET**

**2012** — Released new-generation 50V **GaN HEMT** technology

Introduced our first 1200V SiC **half-bridge module**

**2014** — Introduced industry's first 1200V SiC 25mΩ **MOSFET**

Introduced industry's first 1700V SiC **half-bridge module**

Became Department of Defense **Trusted GaN Foundry**

**2015** — Exceeded 2 trillion field hours **power**

Introduced industry's first 900V SiC **MOSFET**

Acquired **APEI**

**2016** — Introduced the industry's first **1000V SiC MOSFET**

Demonstrated **200mm SiC wafer**

Released market's highest power, single-ended GaN RF transistor for **L-Band Radar**

**2017** — Introduced a **SiC** 900V, 10mΩ MOSFET for EV drive trains, enabling reduction of EV drive train inverter losses by 78%

Introduced **SiC** 1200V, 75mΩ MOSFET with industry's lowest figure of merit

**2018** — Acquired **Infineon's RF Power** business

**2019** — Announce **next generation** of **SiC diodes** for renewable energy **EV applications**

**2020** — New **650v MOSFETs** offer industry leading efficiency to enable the next generation of EVs, data centers and solar innovations

**2021** — New **Wolfspeed WolfPACK™** module family enables accelerated production of high growth mid-power technologies

Mohawk Valley opening

# INVESTMENT FOR SiC GROWTH

## Expanding Capacity for Silicon Carbide

RENDERING OF THE MOHAWK VALLEY FAB
CURRENTLY UNDER CONSTRUCTION

At Cree | Wolfspeed, we are driving the industry transition from silicon to silicon carbide. To meet the increasing demand for our groundbreaking Wolfspeed technology that supports the growing electric vehicle (EV), 4G/5G mobile and industrial markets, we announced last fall that the company is establishing a silicon carbide corridor on the East Coast of the United States.

We are currently constructing the world's largest silicon carbide fabrication in Marcy, New York. This brand new, state-of-the-art power and RF wafer fabrication facility will be automotive-qualified and 200mm-capable. It is complemented by our mega materials factory expansion currently underway at our Durham, North Carolina headquarters. The new fabrication facility will dramatically increase capacity for our Wolfspeed silicon carbide and GaN business and will be a bigger, highly-automated factory with greater output capability.

# WOLFSPEED

**New name!**

Cree, Inc. Officially Changes Com

https://www.wolfspeed.com/company/news-events/news/cree-inc-officially-changes-company-name-to-wolfspeed-inc-marking-successful-transition-to-global-semiconductor-powerhouse

Wolfspeed

Products Applications Tools & Support Company Careers Investors

中文

Contact

Corporate, Investors

## Cree, Inc. Officially Changes Company Name to Wolfspeed, Inc., Marking Successful Transition to Global Semiconductor Powerhouse

Oct 04, 2021

Home > Company > News & Events > News > Cree, Inc. Officially Changes Company Name To Wolfspeed, Inc., Marking Successful Transition To Global Semiconductor Powerhouse

*Company Begins Trading Today Under New Ticker "WOLF" on NYSE*

**DURHAM, N.C.** *Oct. 4, 2021* – Following a massive four-year transformation, involving the divestiture of two-thirds of the business and a repositioning of the company's overall core strategy, today marks the creation of Wolfspeed, Inc. (NYSE: WOLF), the global leader in Silicon Carbide technology and production. The company, formerly known as Cree, Inc. (Nasdaq: CREE), officially launches under its new name with the support of a comprehensive, multi-channel, integrated marketing campaign.

Wolfspeed has served as the brand for the company's Silicon Carbide materials and semiconductor devices business unit for the past six years. Built on a 30-year heritage of domain expertise, the name Wolfspeed conveys both the noble traits of the wolf – leadership, intelligence and endurance – and

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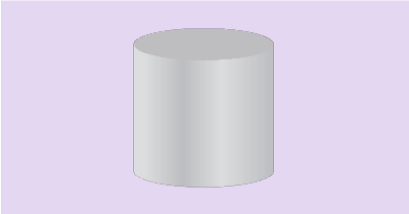
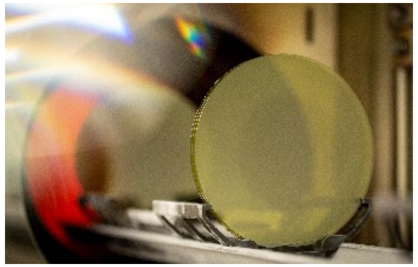
# THE WOLFSPEED ADVANTAGE

**Vertically-Integrated SiC and GaN Manufacturer**

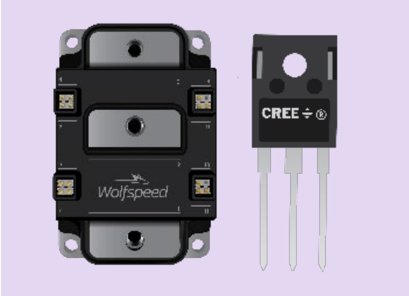


**GROW** SILICON CARBIDE BOULES



**SLICE & POLISH** WAFERS

**GROW** EPI & **FABRICATE** DEVICES




**PACKAGE** DIE

# ADOPTION OF WOLFSPEED SiC INTO VARIOUS APPLICATIONS

**It's all around**

## PV Inverters

Shipping in high volume

- MOSFETs
- Diodes
- Modules

## Battery Chargers for EV

Shipping in high volume

- MOSFETs
- Diodes
- Modules

## Server Power Supply

Shipping in high volume

- MOSFETs in evaluation
- Diodes shipping in high volume

## Traction

Shipping in volume

- SiC Modules

# ABSTRACT

SiC power devices offer performance advantages over competing Si-based power devices, due to the wide bandgap and other key materials properties of 4H-SiC. For example, SiC can more easily be used to fabricate MOSFETs with very high voltage ratings (up to 10 kV), and with lower switching losses. The reliability of SiC power devices is excellent and has continued to improve due to continuing advancements in SiC substrate quality, epitaxial growth capabilities, and device processing. This has enabled the continually accelerating growth of SiC power device commercial adoption. I will review the wear-out mechanisms and intrinsic reliability performance of power SiC devices as characterized by time-dependent dielectric breakdown (TDDB), accelerated life test high temperature reverse bias (ALT-HTRB), bias/temperature instability (BTI), terrestrial neutron exposure, and power cycling. I will review failure mechanisms that have been characterized and addressed through technological advances. I will show qualification data on a wide variety of product families, including discrete devices up to 50 A rated current. Finally, I will show field return data that demonstrates less than 5 FIT (fails per billion device hours) for commercially produced SiC MOSFETs and Schottky diodes, with over 2 trillion device field hours.

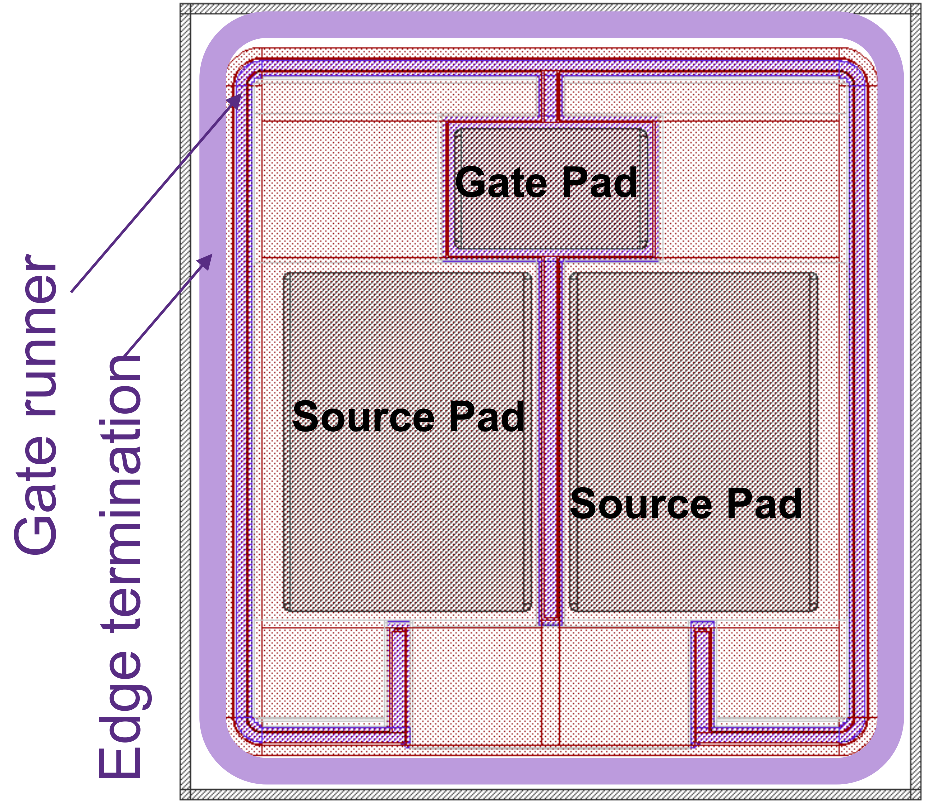
# GLOSSARY

- ALT-HTRB: accelerated life test HTRB
- BDOL: body diode operating life
- BPDs: basal plane dislocations
- BTI: bias-temperature instability
  - NBTI: negative-BTI
  - PBTI: positive-BTI
- ELFR: early life failure rate
- HTGB: high temperature gate bias
- HTGS: high temperature gate switching
- HTRB: high temperature reverse bias
- HV-H3TRB / THB (synonymous): high-voltage high humidity, high temperature reverse bias / temperature-humidity bias
- MTTF: median time to failure
- SEB: single event burn-out
- SFs: stacking faults
- TDDB: time-dependent dielectric breakdown
- $V_{TH}$, $V_{gs(th)}$: threshold voltage
- WBG: wide bandgap

# OUTLINE

- MOSFET salient features and device-level failure mechanisms
- Reliability 101
- Packaging reliability
- Product qualification
- Field reliability
- Industry-wide consortia guidelines and standards

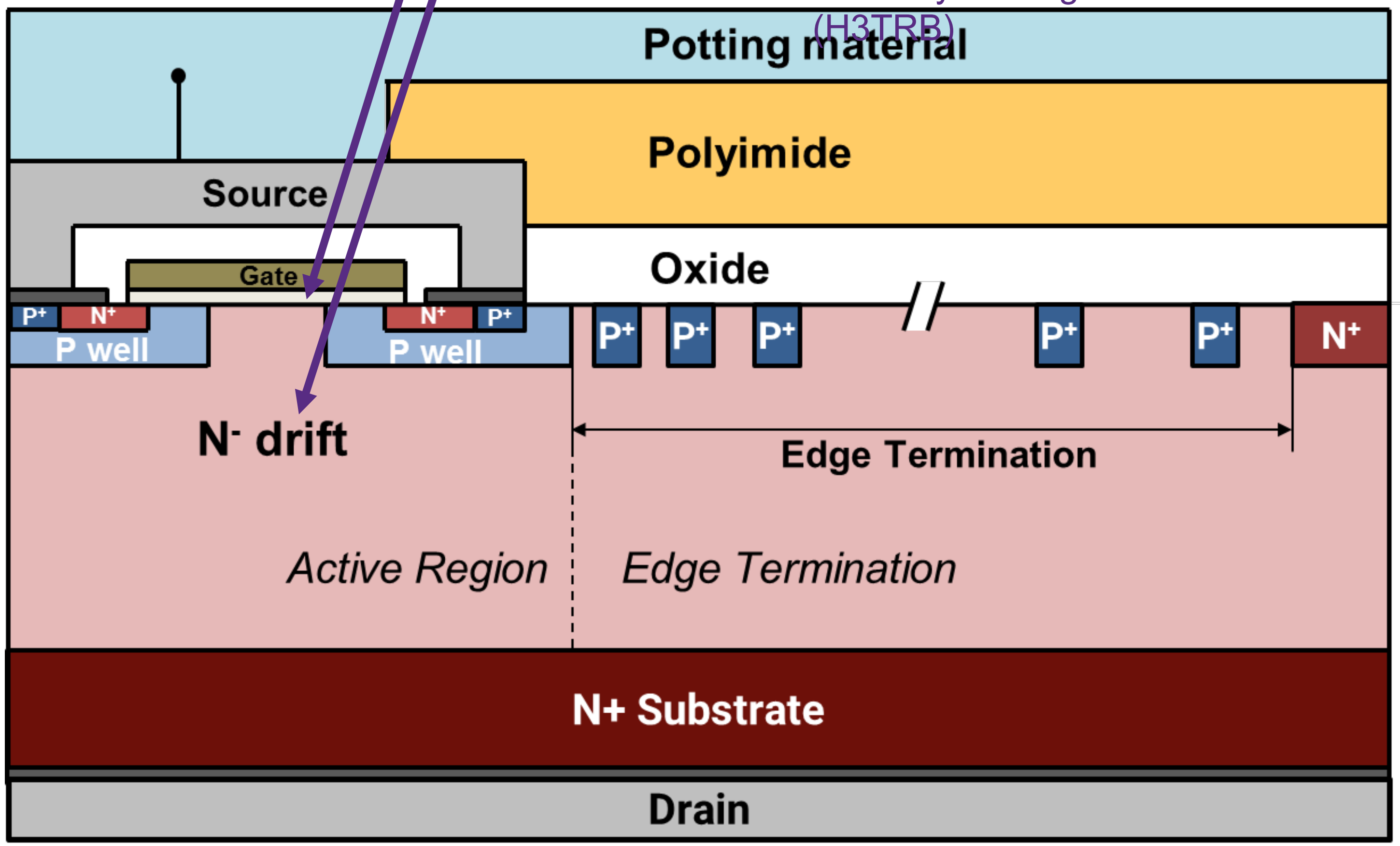
# SiC MOSFET SALIENT FEATURES




**Drain is the backside of the chip**

**Device-level failure mechanisms**

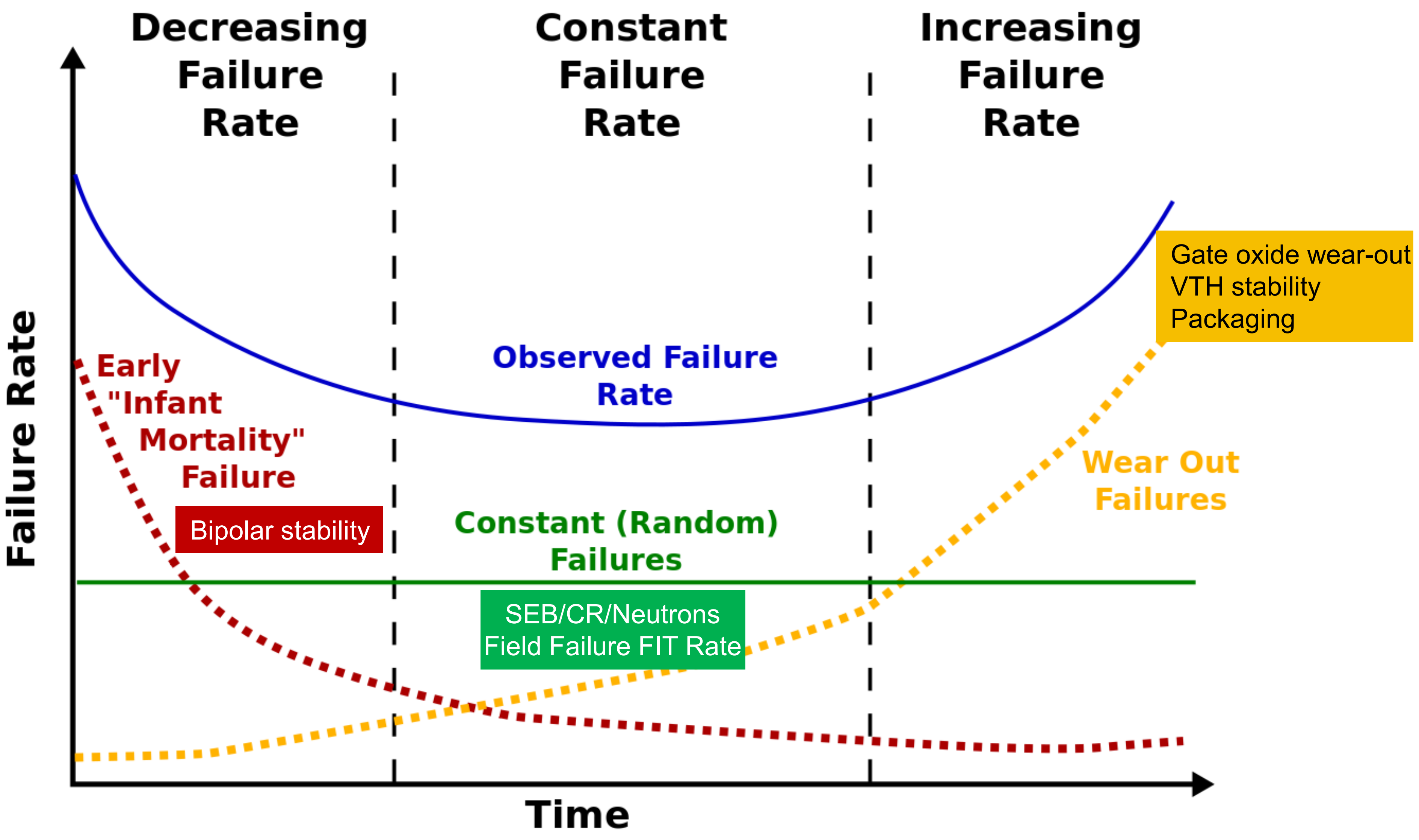
- Gate oxide wear-out (TDDB & HTRB)
- VTH stability (NBTI/PBTI)
- Neutron SEB (CR)
- Bipolar instability: BPDs/SFs (BDOL
- Humidity: leakage / corrosion (H3TRB)




Schematic by E. VanBrunt et al., ECSCRM 2018

# RELIABILITY 101

**Failure rate over time: Bathtub Curve**



# THRESHOLD VOLTAGE STABILITY

# THRESHOLD VOLTAGE STABILITY (PBTI OR NBTI)

- Threshold voltage shift ($\Delta V_T$) with time can change the on-state and/or blocking characteristics
- This can happen in Si or SiC MOSFETs
- $\Delta V_T$ relates to interface & oxide traps [1,2] (filling/emptying/creation):

  $$\Delta V_T = q*(\Delta N_{ox}+\Delta N_{IT})*[(q*T_{ox})/(K_{ox}*\varepsilon_o)]$$

- $\Delta V_T$ of Si MOSFETs depends on MOS gate electric field, temperature, and time [1,2]:

  $$\Delta V_T = A*\exp(\gamma E_{ox})*\exp(-\mathbf{E_A}/kT)*t^n$$

  n typically ~0.2 – 0.25 for Si devices

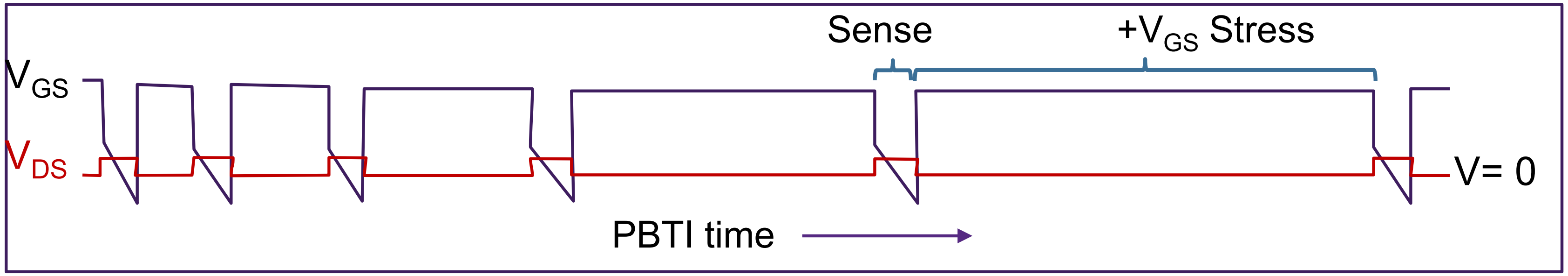
- SiC MOSFETs have more traps than Si MOSFETs -> $V_T$ stability more of a concern

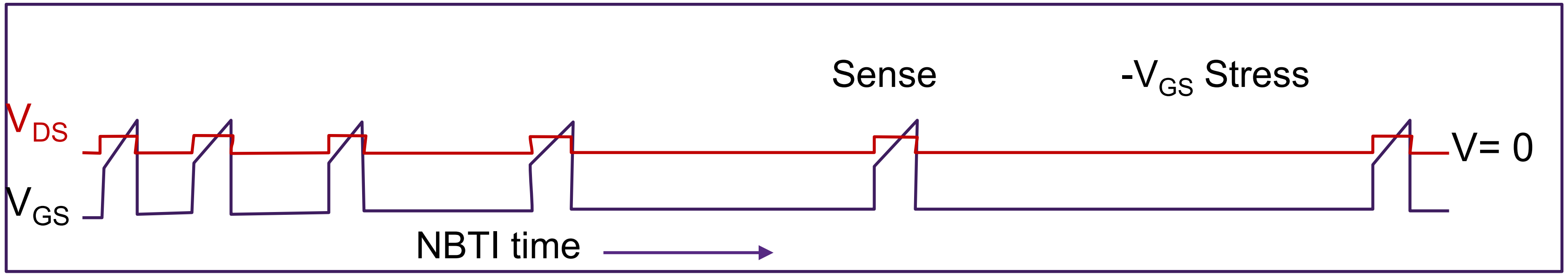
[1] J.H. Stathis and S. Zafar, “The negative bias temperature instability in MOS devices: A review,” Microelectronics Reliability 46 (2006) pp. 270-286.
[2] D.K. Schroder, “Negative bias temperature instability: What do we understand?” Microelectronics Reliability 44 (2007) pp. 841-852.

# PBTI, NBTI TEST PROCEDURE

- Heat sample to test temperature, and hold T constant

1. Apply $V_{GS}$ stress for given time (start with 0.1s), with $V_S = V_{DS} = 0$ V
2. Sweep $V_{GS}$ from stress V towards $V_{GS} = 0$ V, with $V_S = 0$ V and $V_{DS} = 0.1$ V
3. Repeat 2) and 3) using logarithmically increasing stress times
4. Extract $V_T$ at a fixed current level to plot $V_T$ versus time

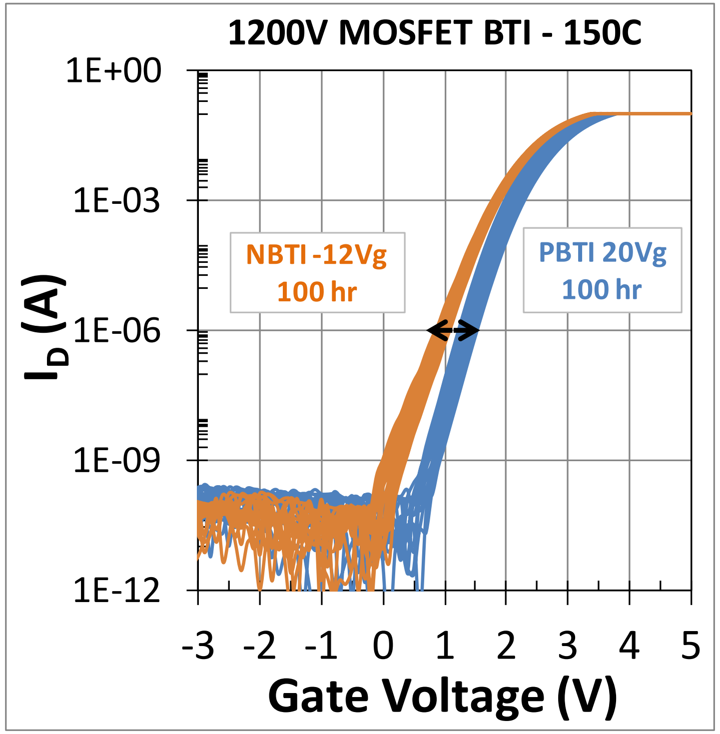


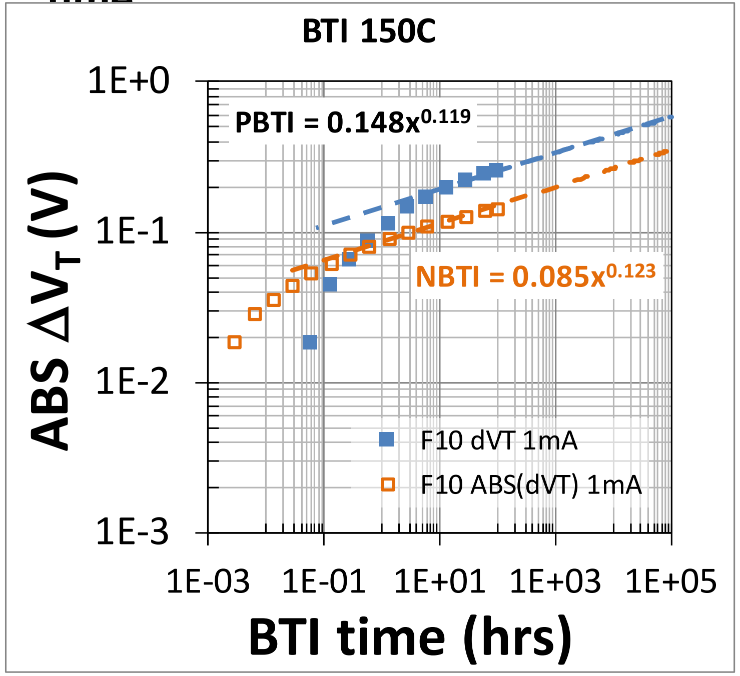

Lichtenwalner - Virtual IIRW, October 2020

# THRESHOLD VOLTAGE STABILITY (PBTI, NBTI) OF SIC POWER MOSFETS

- **1200V Gen3 13mohm SiC MOSFETs, Wolfspeed**
- Recommended use $V_{GS}$ is +15V/-4V
- Log time stress periods, $V_{GS}$ sweep $V_T$ sense




- Log-Log plot of $\Delta V_T$ vs *accelerated* BTI stress time

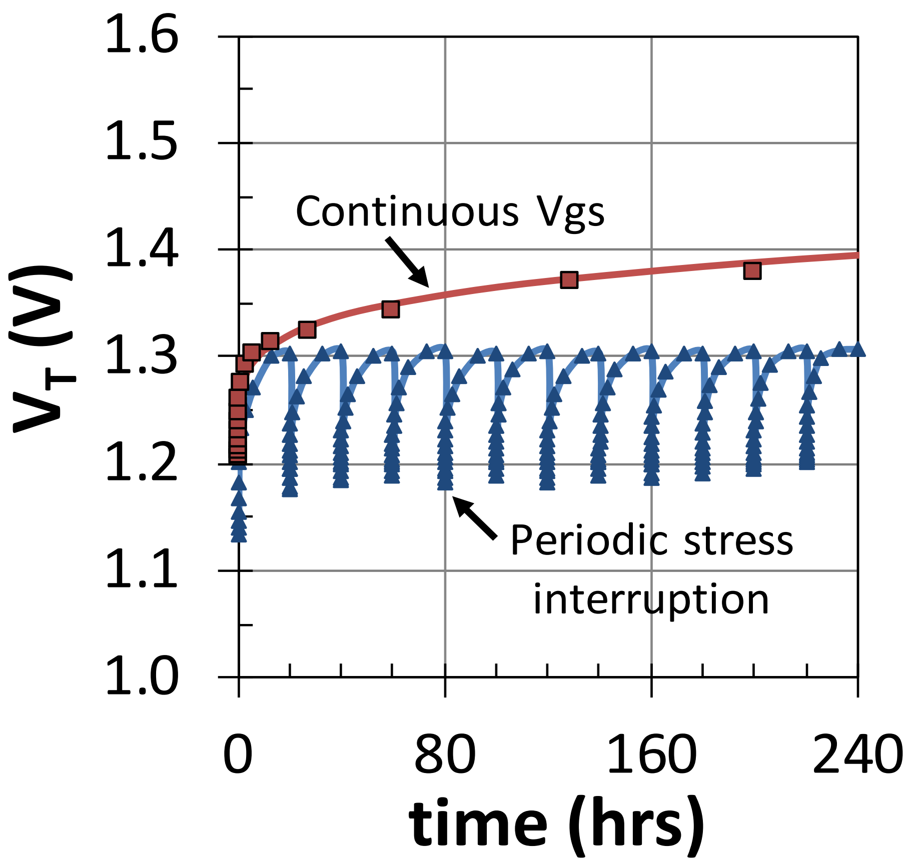



- Power law exponent (~0.12) describes long-term $V_T$ shift *at $V_{GS}$ above use conditions*
- ~0.3V $V_T$ shift in 1000hrs of +20$V_{GS}$ stress

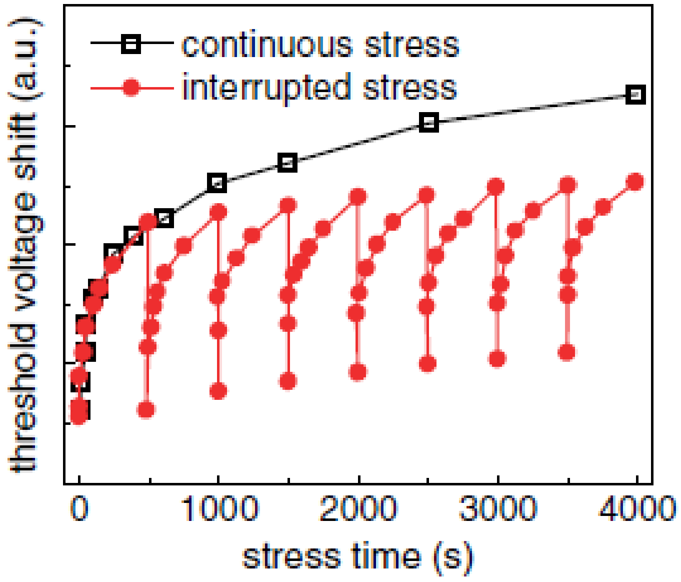
How much does $V_T$ shift under interrupted bias / switching operation?

# PBTI/NBTI RECOVERY/SWITCHING EFFECTS

**900V 65mohm SiC MOSFETs (150°C,**




Threshold voltage ‘recovery’ also observed in Si MOSFETs



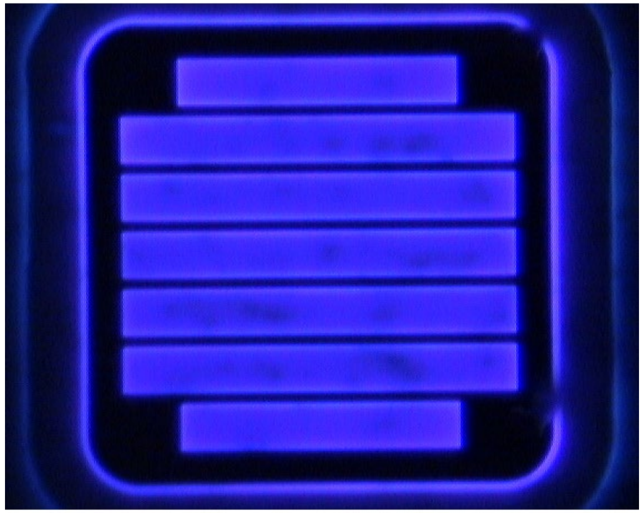

(in J.H. Stathis & S. Zafar, *Micro. Reliab.* 46 (2006))

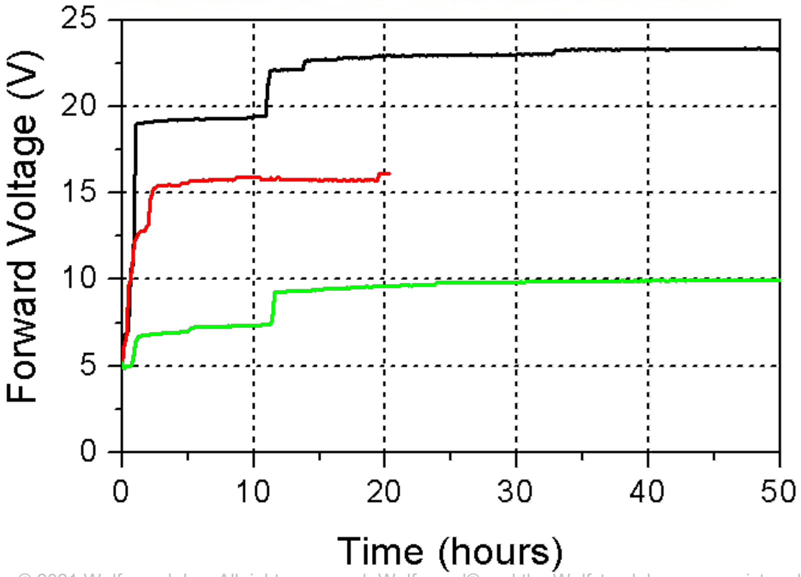
Interrupted stress is closest to SiC MOSFET switching applications; greatly reduced $\Delta V_T$ observed

# BIPOLAR / BODY DIODE STABILITY

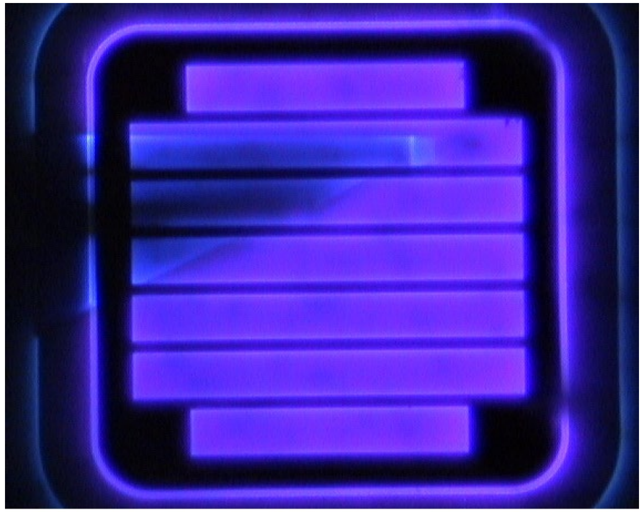
# BIPOLAR / BODY DIODE STABILITY IN SiC

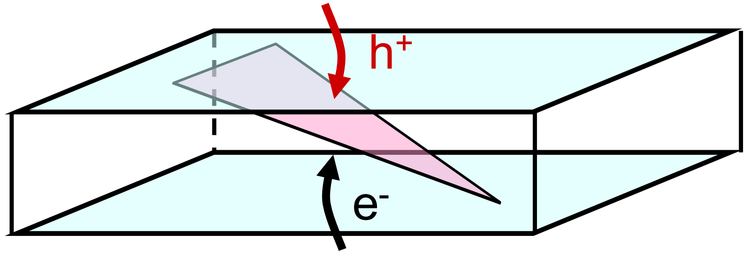
Gridded PiN Diode (ca 2006) EL image






Gridded PiN diode EL after forward stress






Basal plane dislocations

⬇

3rd quadrant electron/hole recombination

⬇

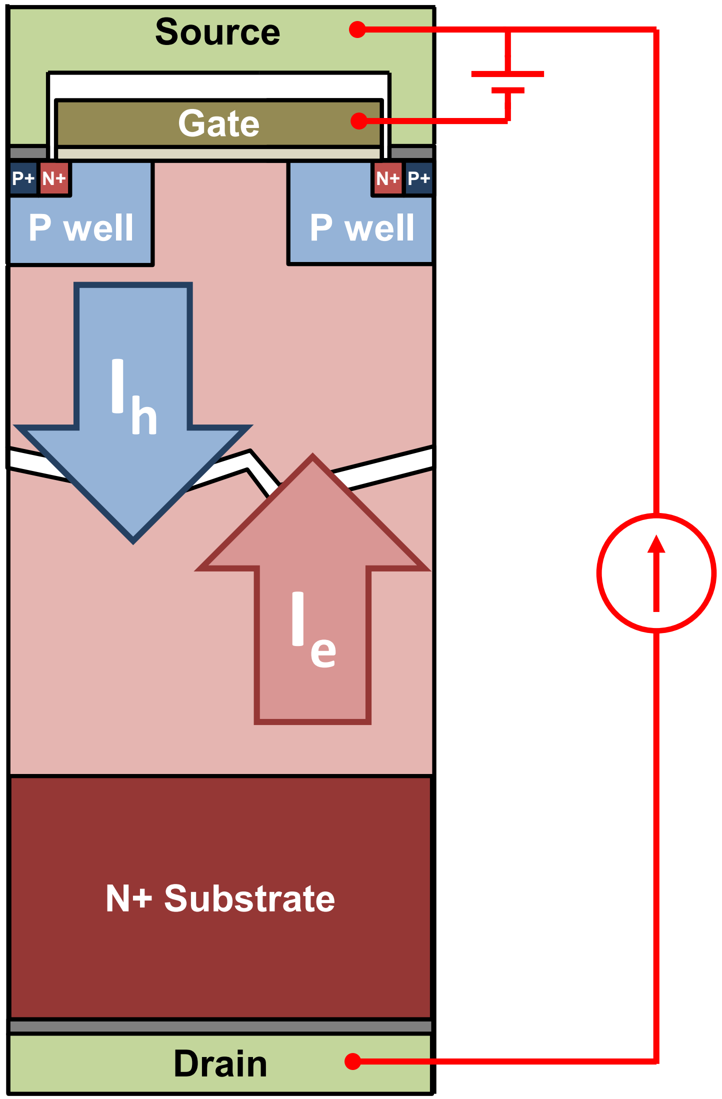
SiC stacking faults

⬇

Increased resistance and leakage

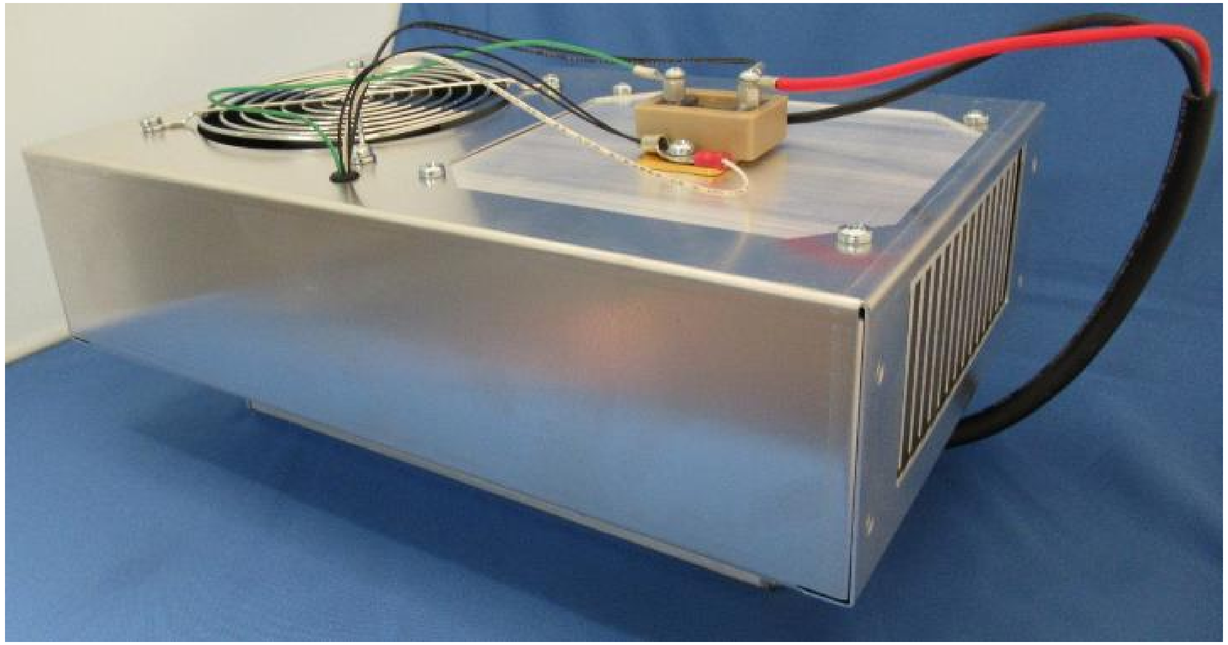
# BODY DIODE OPERATING LIFE (BDOL): A UNIQUE TEST FOR SiC MOSFETS

- Bias gate into off-state ($-V_{GS}$)
- Apply rated device current through body diode conduction path
- See if anything breaks in ### hours



# BODY DIODE TEST SYSTEM DESIGNED FOR HIGH POWER DISSIPATION

Body-Diode Stress Test Unit

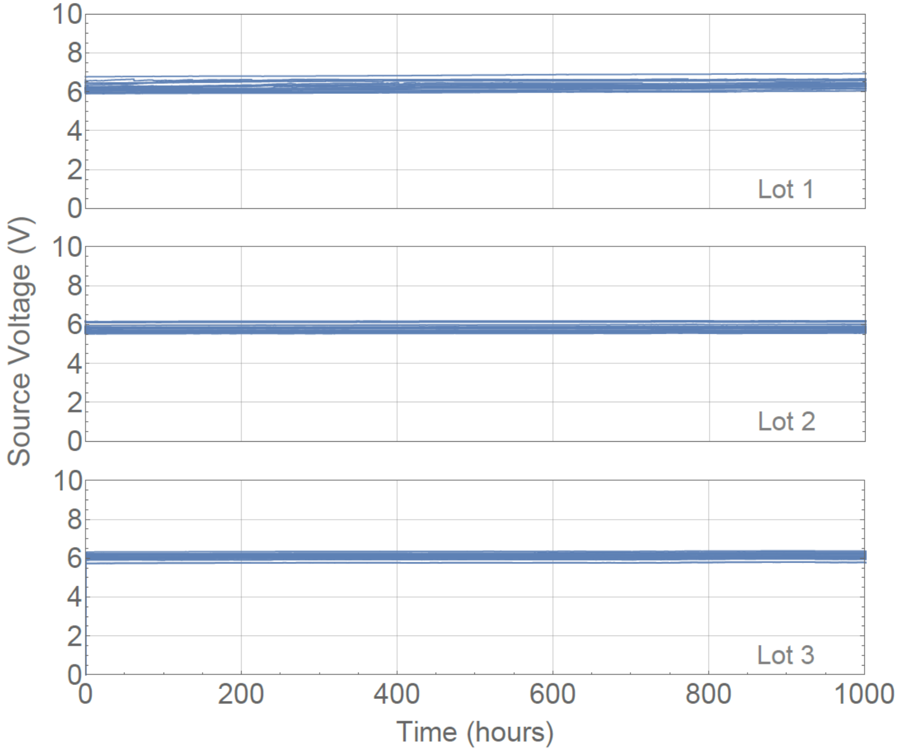


Rack for Stress Test Units

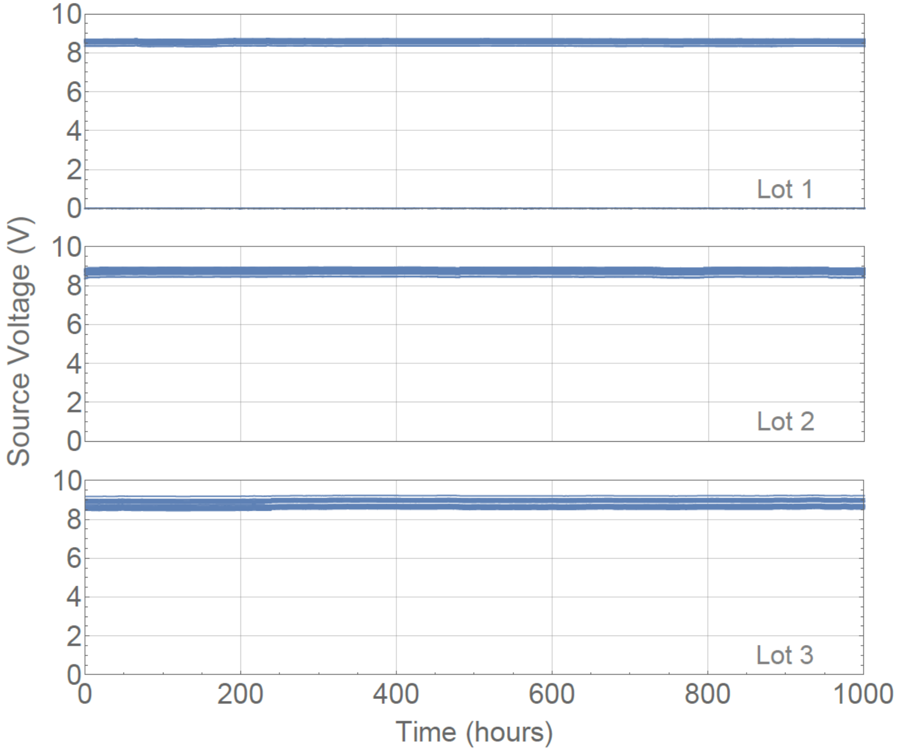
- 3.3 kV MOSFET $T_J$ during testing: 140 °C
- 6 kW dissipated for qualification testing for 3.3kV MOSFET
- Separate circuit board to provide temperature monitoring and -5V gate drive

# BDOL TESTING SHOWED COMPLETE STABILITY IN 3RD QUADRANT OPERATION

*In-situ* monitored source voltage
3.3 kV MOSFETs at 40 A



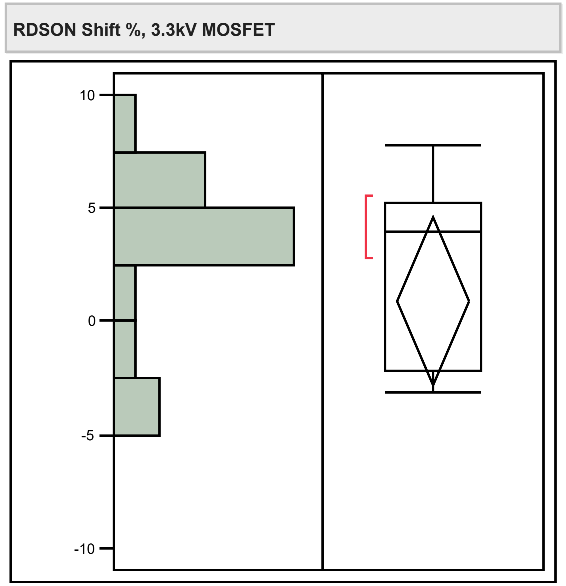

*In-situ* monitored source voltage
10 kV MOSFETs at 15 A

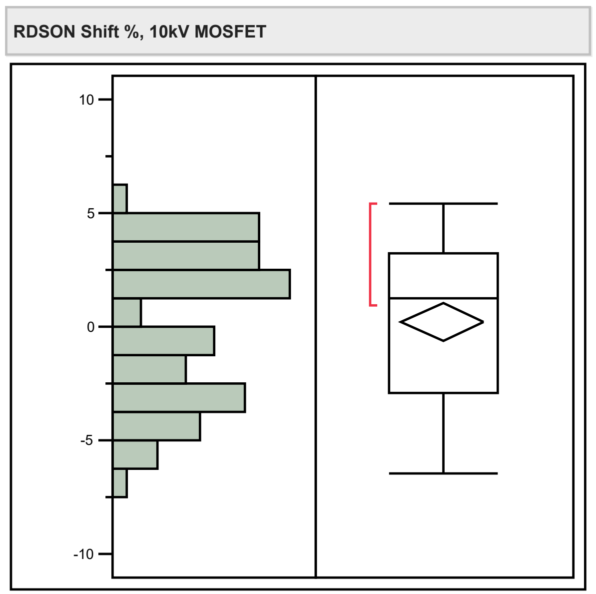



Zero failures in 1000 hours for 61 of 3.3 kV and 65 of 10 kV MOSFETs

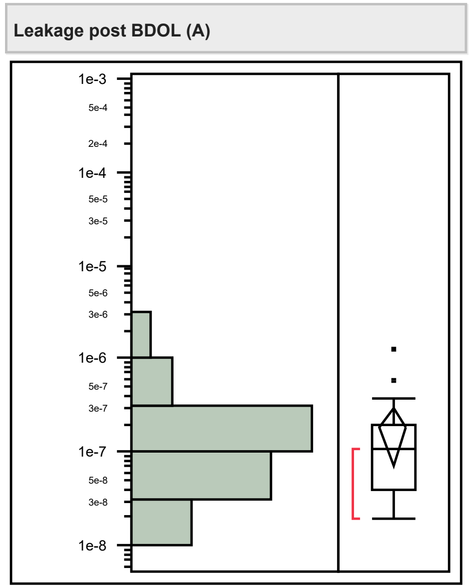
# BDOL: NO SHIFTS IN ANY DEVICE PARAMETER DETECTED POST-STRESS

**(RDSON Post-RDSON Pre)/(RDSON Pre) * 100%, all lots**




**10 kV MOSFET leakage, one lot**

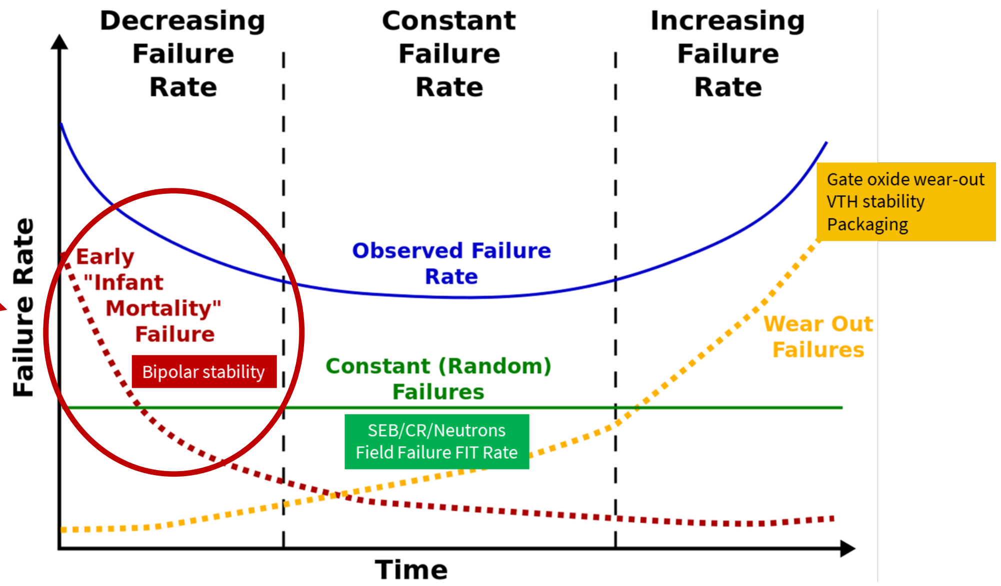



Not shown:

- No shift in MOSFET threshold voltage
- No shift in post-measured $V_{SD}$ (body diode voltage) at room temperature

# BIPOLAR STABILITY – RELIABILITY IMPLICATIONS

- IMPORTANT NOTE ABOUT BODY DIODE:
  - If a MOSFET does not have any BPDs to begin with, then stacking faults cannot nucleate and grow, and bipolar degradation will not occur
  - Therefore, **reducing occurrence of and screening out BPDs** are very important for 3rd quadrant reliability!
- Reliability implications:
  - Literature evidence largely agrees that bipolar instability cannot be accelerated
  - No known acceleration factors
  - No known predictive lifetime model
  - Fortunately, most or all failures occur in <~100 hrs BDOL stress
  - Bipolar stability is an **early life failure** mechanism, **not wear-out**
  - To ensure low PPM and ELRF, need to rely heavily on:
    - Testing large sample sizes
    - Testing large devices
    - Testing higher voltage devices
    - **Aggressive and state-of-the art screening of BPDs in production**



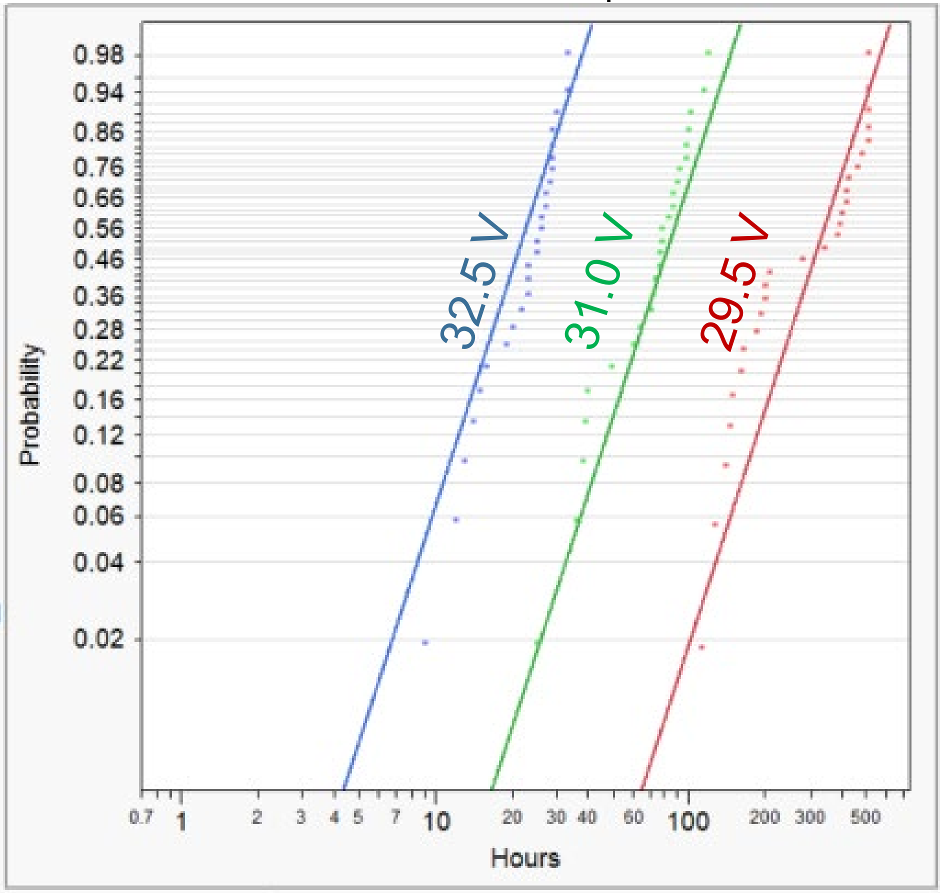
# GATE OXIDE RELIABILITY

# TIME DEPENDENT DIELECTRIC BREAKDOWN (TDDB) METHOD

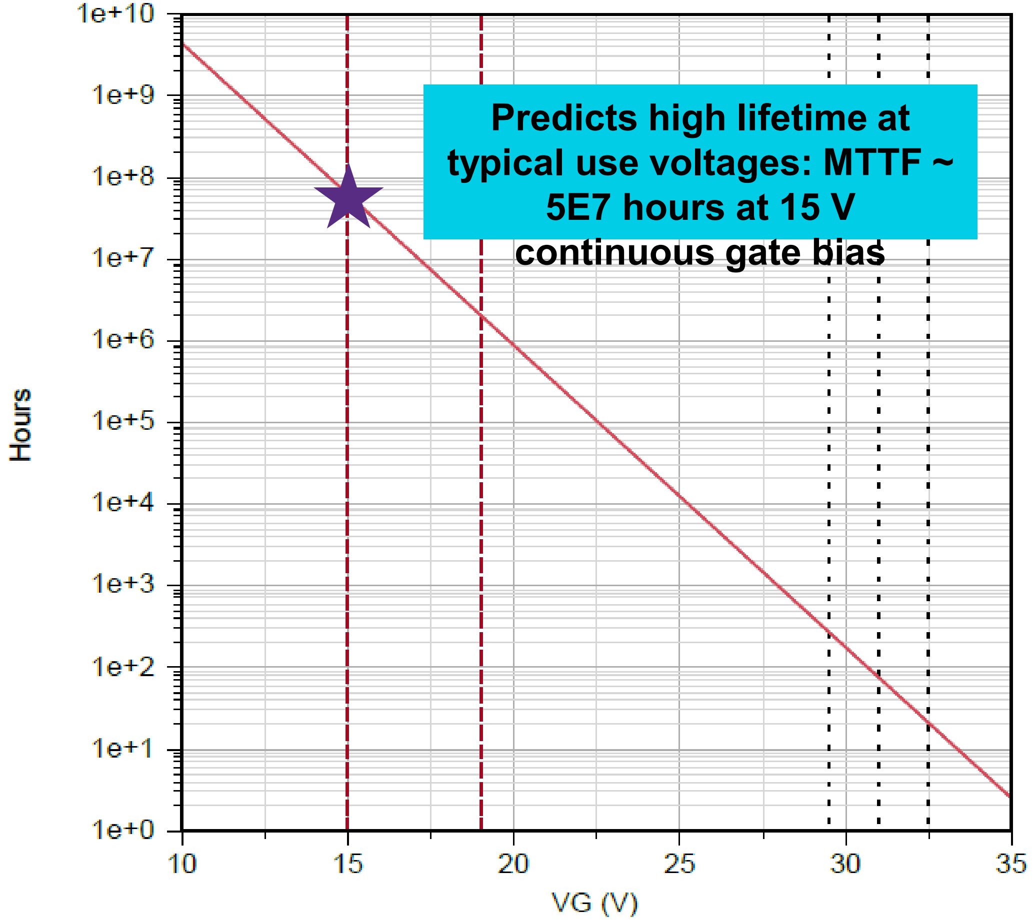
## 1200V 13mohm Gen3 MOSFETs

**175 °C, $V_{DS}$ = 0V**

Weibull statistics plot




Predictive lifetime - MTTF

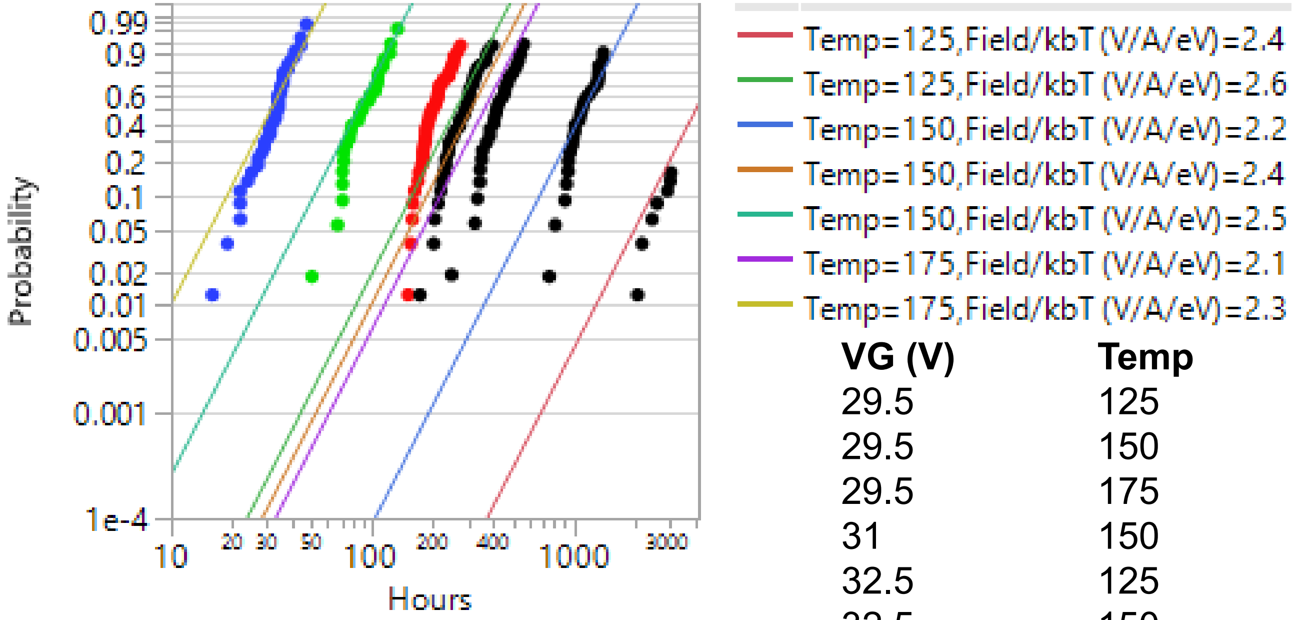



**Similar results on 650V Gen3 MOSFETs**

# PHYSICS-BASED PREDICTIVE LIFETIME MODELING

- TDDB testing versus temperature and voltage used to construct predictive life model published by Joe McPherson (Texas Instruments Reliability Fellow): thermo-chemical model – the same model used for silicon MOSFETs!
- Resulting model parameters are similar to silicon
- Silicon carbide gate oxide reliability on planar MOSFETs is comparable to silicon MOSFETs at the same electric field

$$TF = A_0 \exp\left[\frac{\Delta H_0 - p_{eff} \bullet E}{K_B T}\right]$$



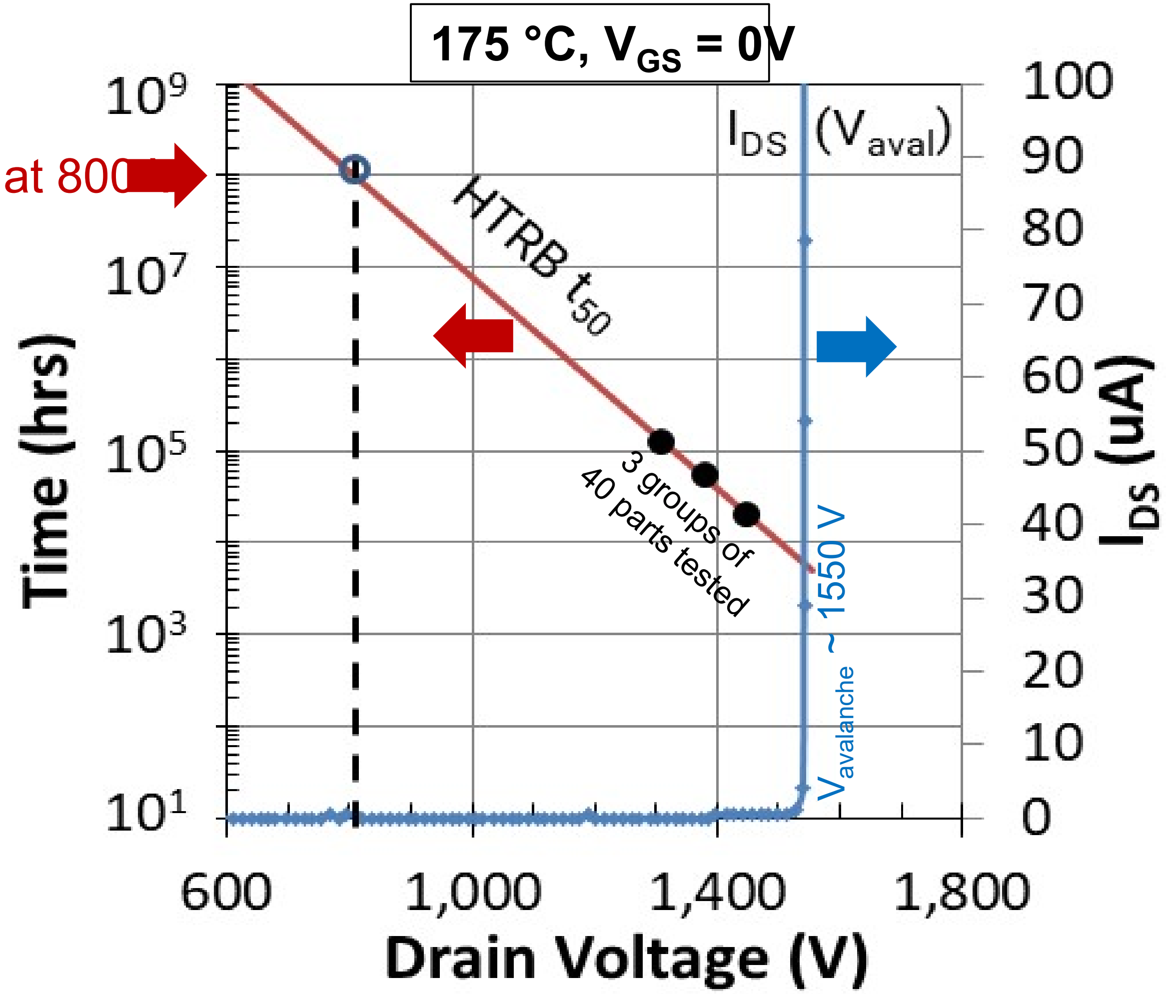

| VG (V) | Temp |
|---|---|
| 29.5 | 125 |
| 29.5 | 150 |
| 29.5 | 175 |
| 31 | 150 |
| 32.5 | 125 |
| 32.5 | 150 |
| 32.5 | 175 |

# REVERSE BIAS RELIABILITY (HTRB)

# ACCELERATED LIFE TEST HIGH TEMPERATURE REVERSE BIAS (ALT-HTRB)

**1200V 75mohm G3 MOSFETs** (C3M0075120D)

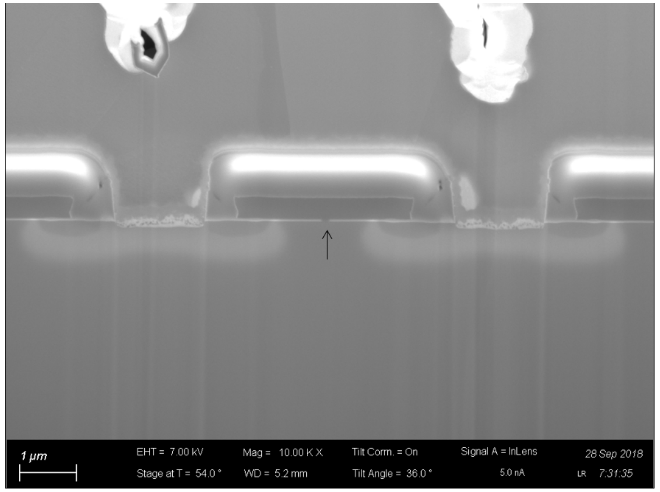
Predicted MTTF 1E8 hours at 800V

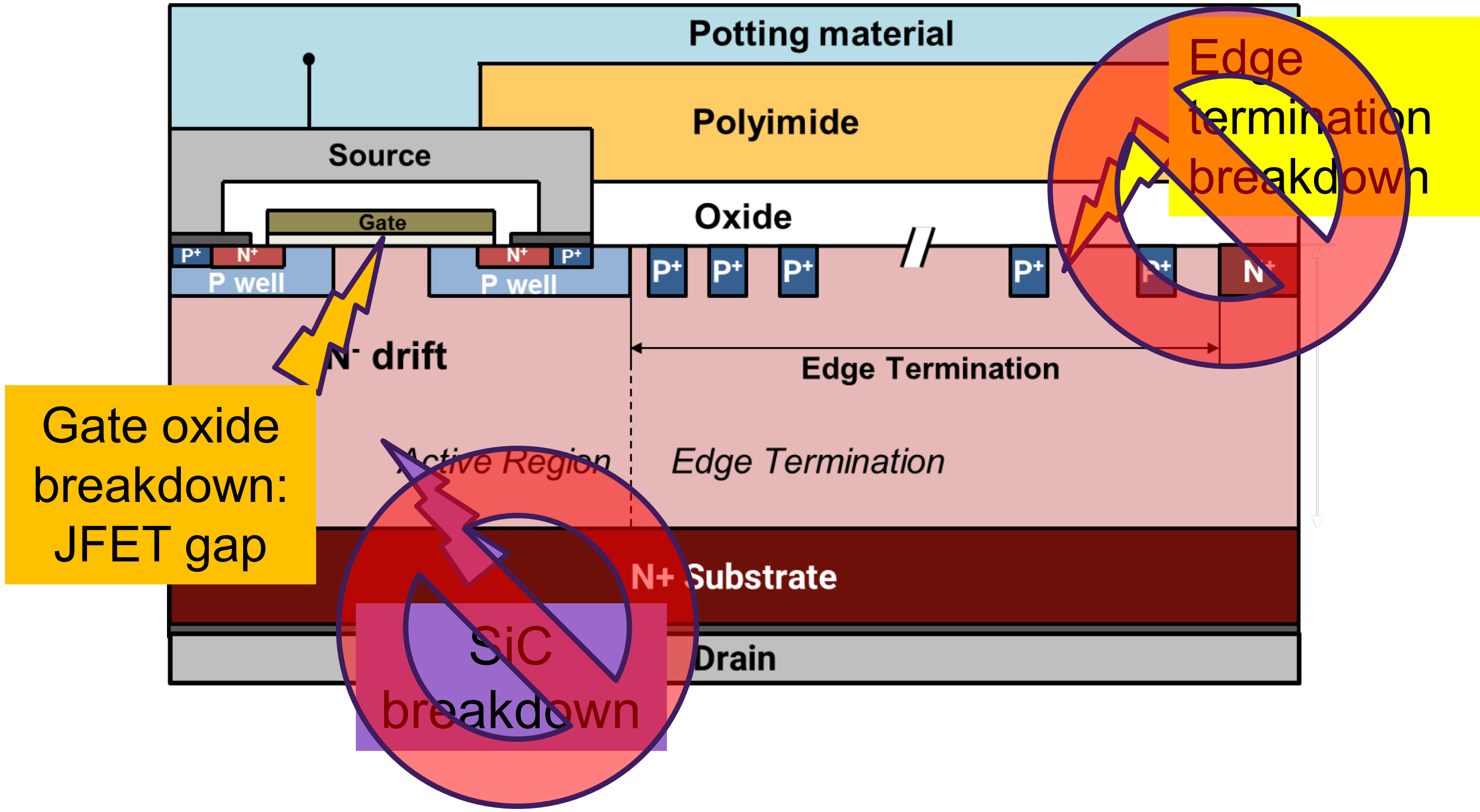



High reverse-bias lifetime demonstrates SiC and $SiO_2$ quality and reliability

# ACCELERATED LIFE TEST HIGH TEMPERATURE REVERSE BIAS (ALT-HTRB)

- For Wolfspeed MOSFETs, physical failure analysis showed that the failures are gate oxide breakdown in the active area, in the JFET gap where the oxide electric field is highest




- Failure analysis found <u>no</u> evidence of:
  - Edge termination breakdown or
  - SiC breakdown
- Gate oxide wear-out models can be used for lifetime prediction

# HUMIDITY RELATED RELIABILITY

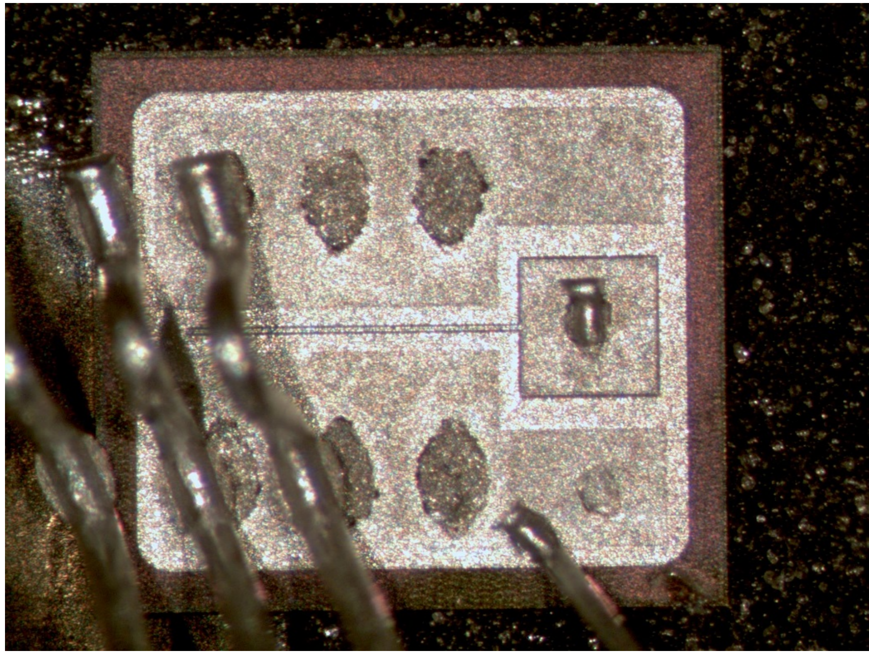
# HUMIDITY RELATED RELIABILITY


- Humidity related reliability is a standard qualification test in all industry standard guidelines
- Wolfspeed E-Series devices have passed 85C/85%RH lifetime testing, with no evidence of corrosion:
  - Gen3 900 V MOSFETs
  - Gen4 1200 V Schottky diodes
- Acceleration factors for THB for SiC have not yet been established, but they are probably similar to those for Si devices, because the metals and dielectrics are similar:
  - Humidity: Peck's model (power law in RH)
  - Temperature: Arrhenius thermal activation
- With good passivation and device design, humidity related reliability of SiC is excellent
  - Inferior passivation films, defects and contamination can lead to issues

# PACKAGING RELIABILITY

# PACKAGING RELIABILITY: POWER CYCLING

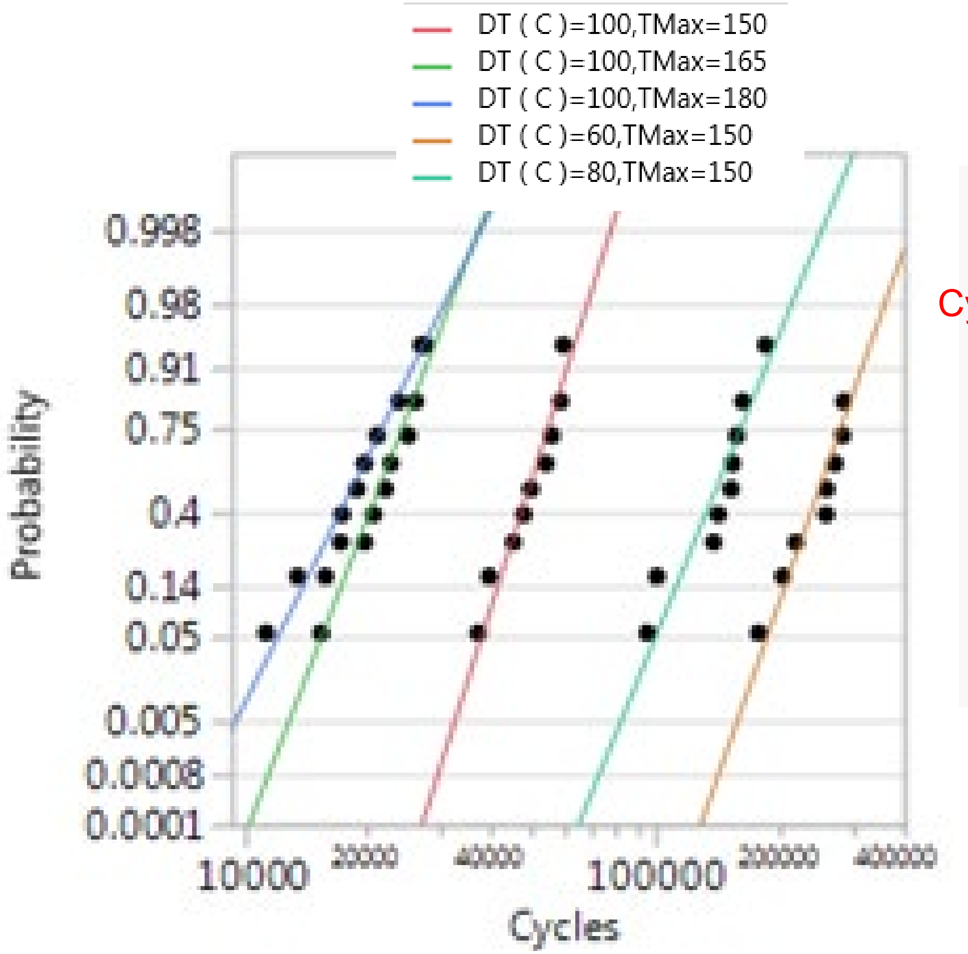
- Power cycling tests wire bond thermomechanical fatigue wear-out
- Use “LESIT model” as described in this paper and others:
  - Held, M. et al., (1997). “Fast Power cycling test of IGBT modules in traction application.” Proc. Power Conversion and Drive Systems. 425 - 430 vol.1. 10.1109/PEDS.1997.618742
  - Model consists of:
    - Arrhenius activation energy term for Tm (max junction temperature)
    - Power law term for ΔTJ: the difference in max and min temperature during the power cycles: ΔTJ = Tjmax – Tjmin
- Power cycling is a property of the die metallization and wire bond
- Not unique to SiC: similar to what happens in Si IGBTs and modules



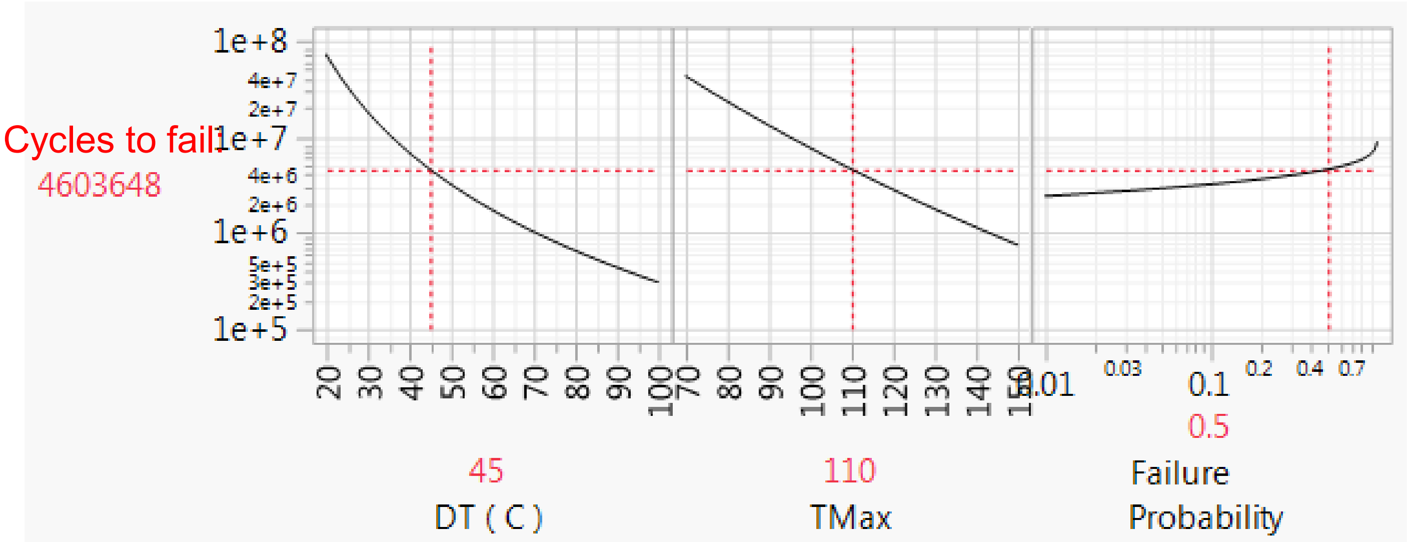
$$Nf = A \cdot \Delta Tj^{\alpha} \cdot \exp\left(\frac{Q}{R \cdot Tm}\right)$$

# POWER CYCLING

**1200V 75 mOhm, Wolfspeed Gen3 MOSFET**
**Plastic overmold packaged C3M0075120K**




Cycles to fail – prediction profiler




Prediction profiler can be used to predict the cycles to fail for any mission profile use condition

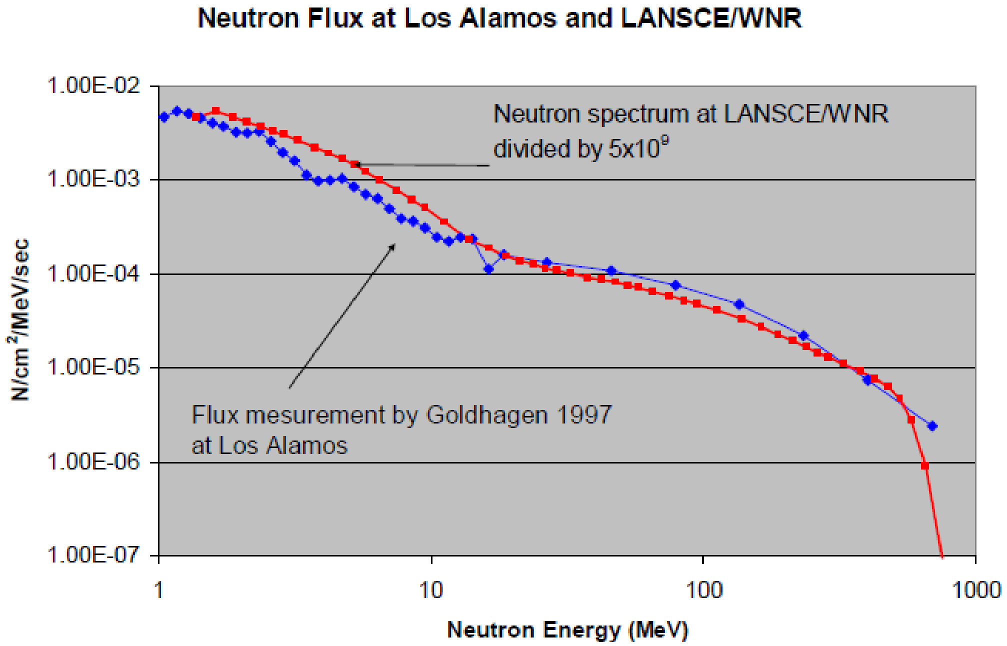
# POWER CYCLING LIFETIME PREDICTIONS FOR EXAMPLE OPERATING CONDITIONS

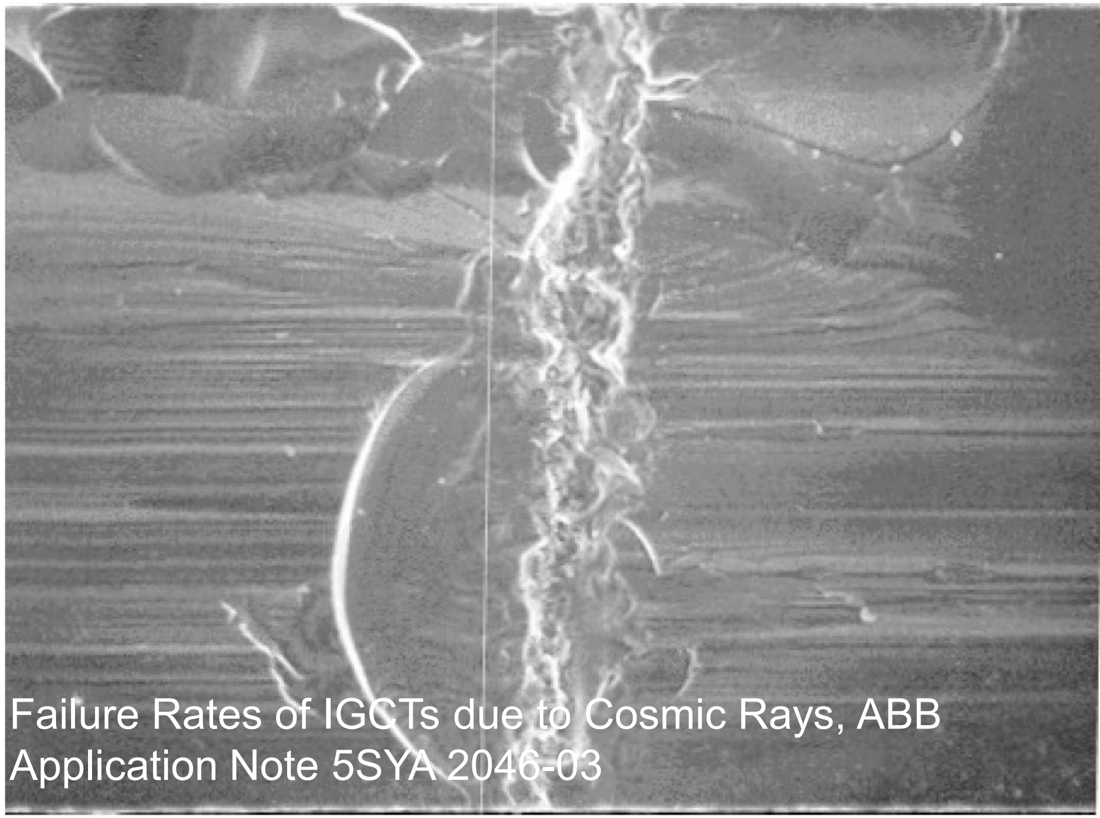
| ΔTJ (°C) | Tjmax (°C) | Cumulative probability | Cycle lifetime prediction | ΔTJ (°C) | Tjmax (°C) | Cumulative probability | Cycle lifetime prediction | ΔTJ (°C) | Tjmax (°C) | Cumulative probability | Cycle lifetime prediction |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 25 | 95 | 0.01 | 38558536 | 35 | 95 | 0.01 | 12328957 | 45 | 95 | 0.01 | 5260910 |
| 25 | 95 | 0.10 | 51560476 | 35 | 95 | 0.10 | 16486281 | 45 | 95 | 0.10 | 7034889 |
| 25 | 95 | 0.50 | 73639345 | 35 | 95 | 0.50 | 23545923 | 45 | 95 | 0.50 | 10047321 |
| 25 | 110 | 0.01 | 17667390 | 35 | 110 | 0.01 | 5649086 | 45 | 110 | 0.01 | 2410531 |
| 25 | 110 | 0.10 | 23624834 | 35 | 110 | 0.10 | 7553958 | 45 | 110 | 0.10 | 3223362 |
| 25 | 110 | 0.50 | 33741297 | 35 | 110 | 0.50 | 10788661 | 45 | 110 | 0.50 | 4603648 |
| 25 | 125 | 0.01 | 8585458 | 35 | 125 | 0.01 | 2745170 | 45 | 125 | 0.01 | 1171396 |
| 25 | 125 | 0.10 | 11480475 | 35 | 125 | 0.10 | 3670842 | 45 | 125 | 0.10 | 1566391 |
| 25 | 125 | 0.50 | 16396564 | 35 | 125 | 0.50 | 5242744 | 45 | 125 | 0.50 | 2237140 |

# COSMIC RAY / NEUTRONS / SEB

# TERRESTRIAL NEUTRONS

- Failure rate is constant with time (FIT): fails per billion device hours)
- Failures are abrupt with very little sign of degradation prior to failure
- Modeling determined empirically at neutron beam facilities to simulate the effect of terrestrial neutrons:




A molten channel through a silicon device created by a charge avalanche triggered by incident cosmic rays during blocking.

Accelerating factors:

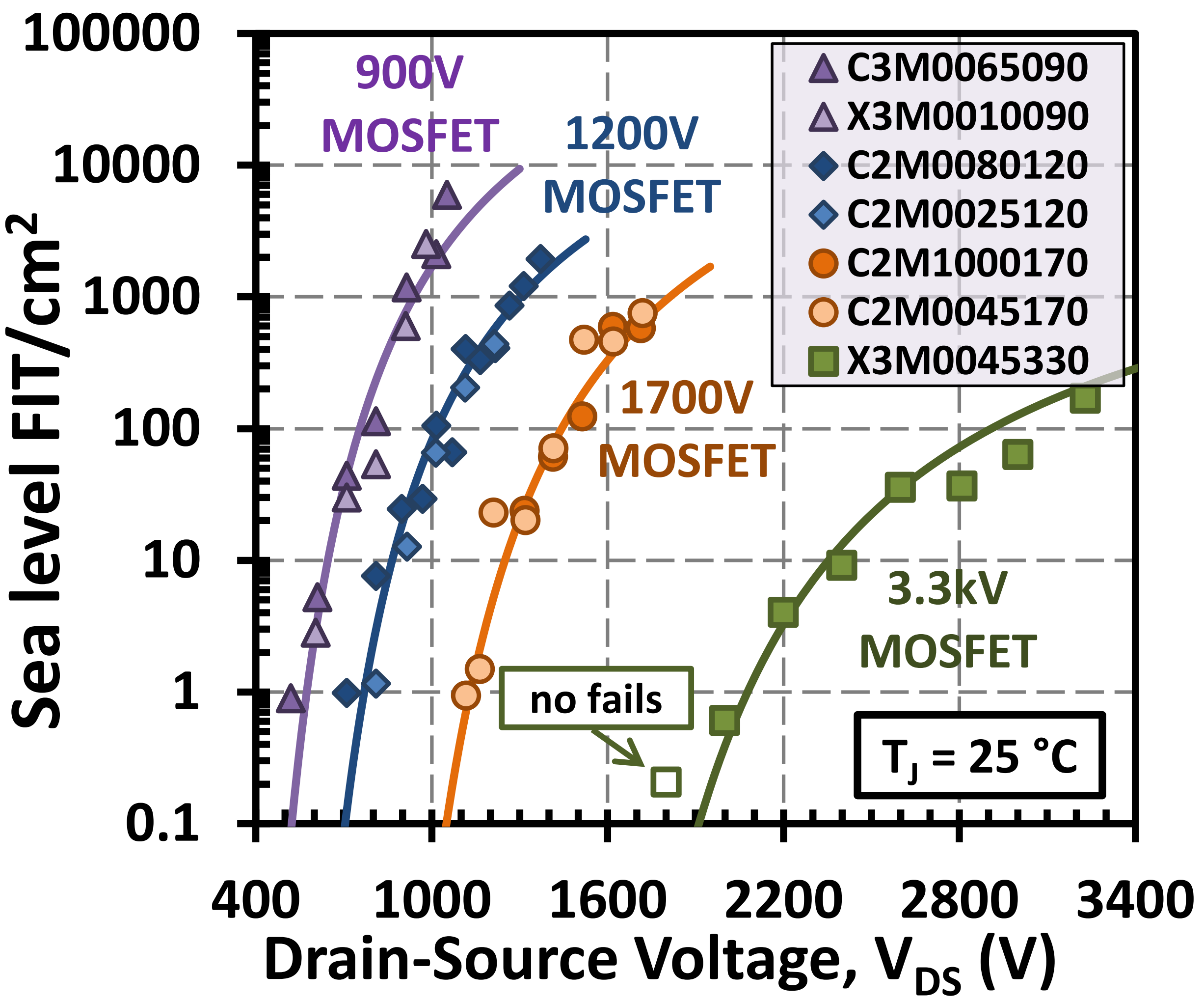
- VDS
- Temperature (negative – colder is worse!)
- Altitude

$$\lambda = C_3 \exp\left(\frac{C_2}{C_1 - V}\right) \cdot \exp\left(\frac{T_0 - T}{C_4}\right) \cdot \exp\left(\frac{1 - \left(1 - \frac{h}{C_5}\right)^n}{C_6}\right)$$

# TERRESTRIAL NEUTRONS

- Wolfspeed SiC MOSFET FIT rates: scaling by active area
- Failure rate increases proportionally with device area
- Failure rate decreases as voltage rating increases
- FIT/cm$^2$ vs $V_{DS}$ for Wolfspeed MOSFETs

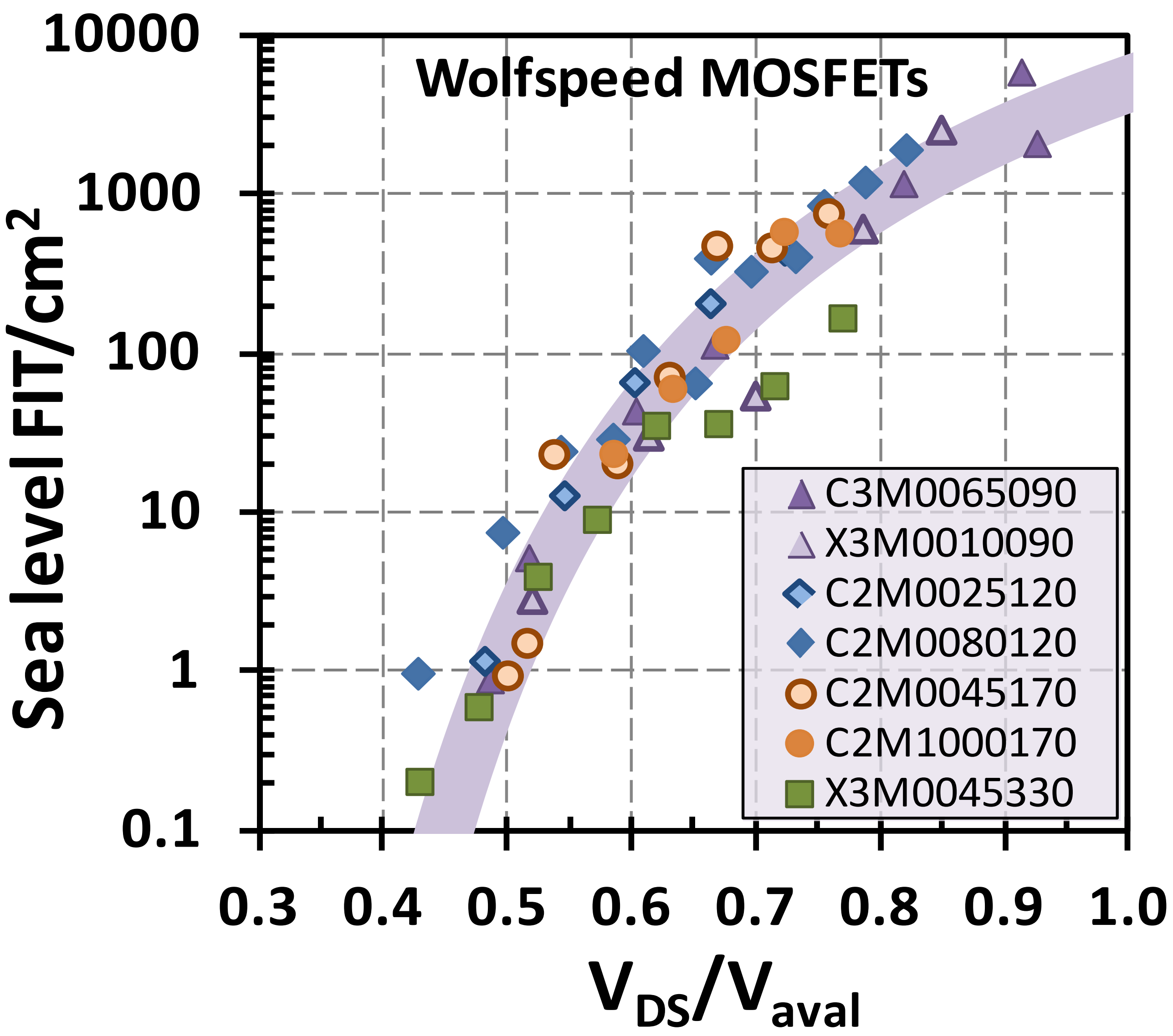
  900V 65 mohm
  900V 10 mohm
  1200V 80 mohm
  1200V 25 mohm
  1700V 1000 mohm
  1700V 45 mohm
  3.3kV 45 mohm




D. Lichtenwalner et al., IRPS 2018

# TERRESTRIAL NEUTRONS

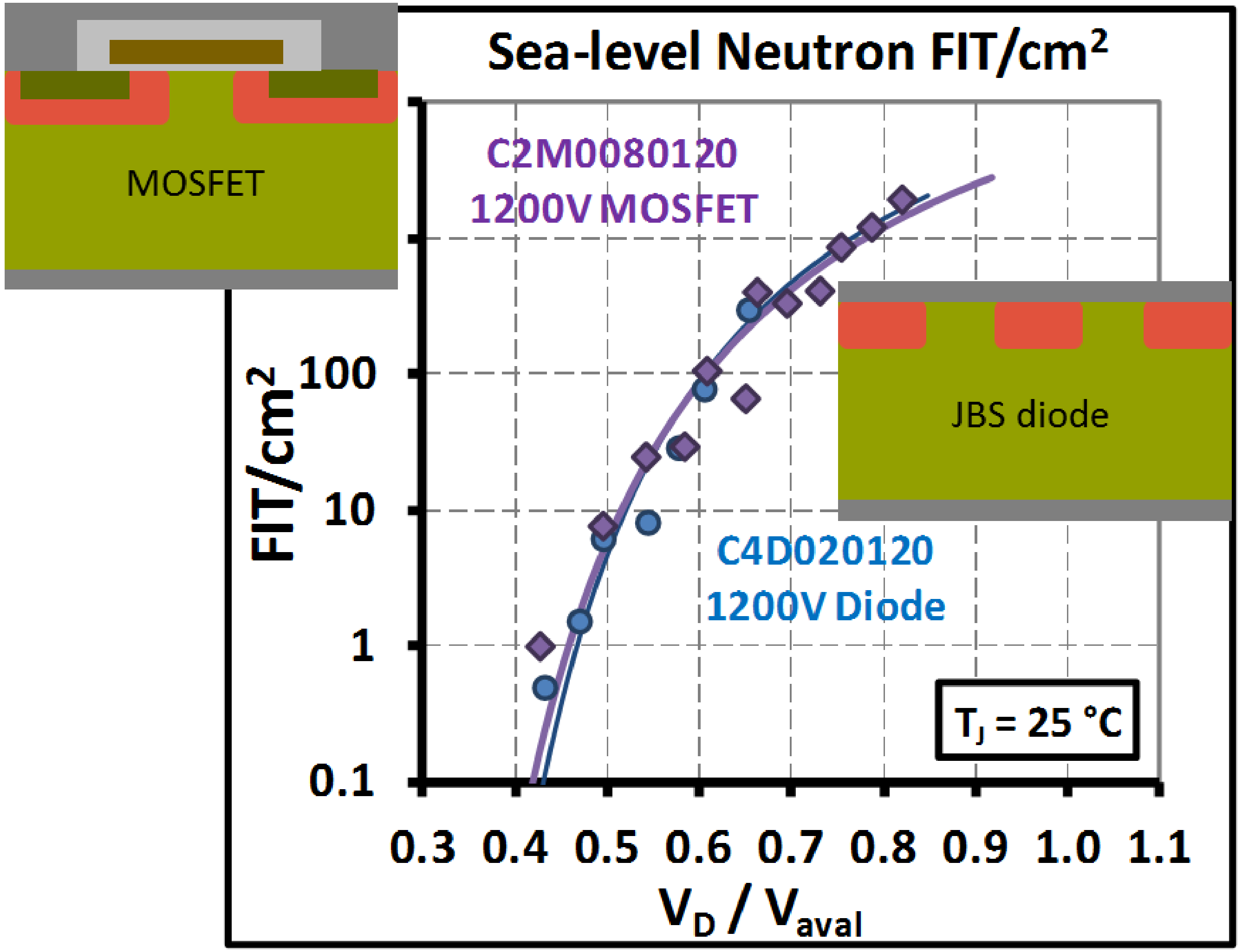
- All device FIT rates scale similarly with active area & drift field (relative to avalanche)
- Active area & drift design can be tailored to meet application-specific system lifetime requirements




D. Lichtenwalner et al., IRPS 2018

# TERRESTRIAL NEUTRONS: MOSFETS AND DIODES

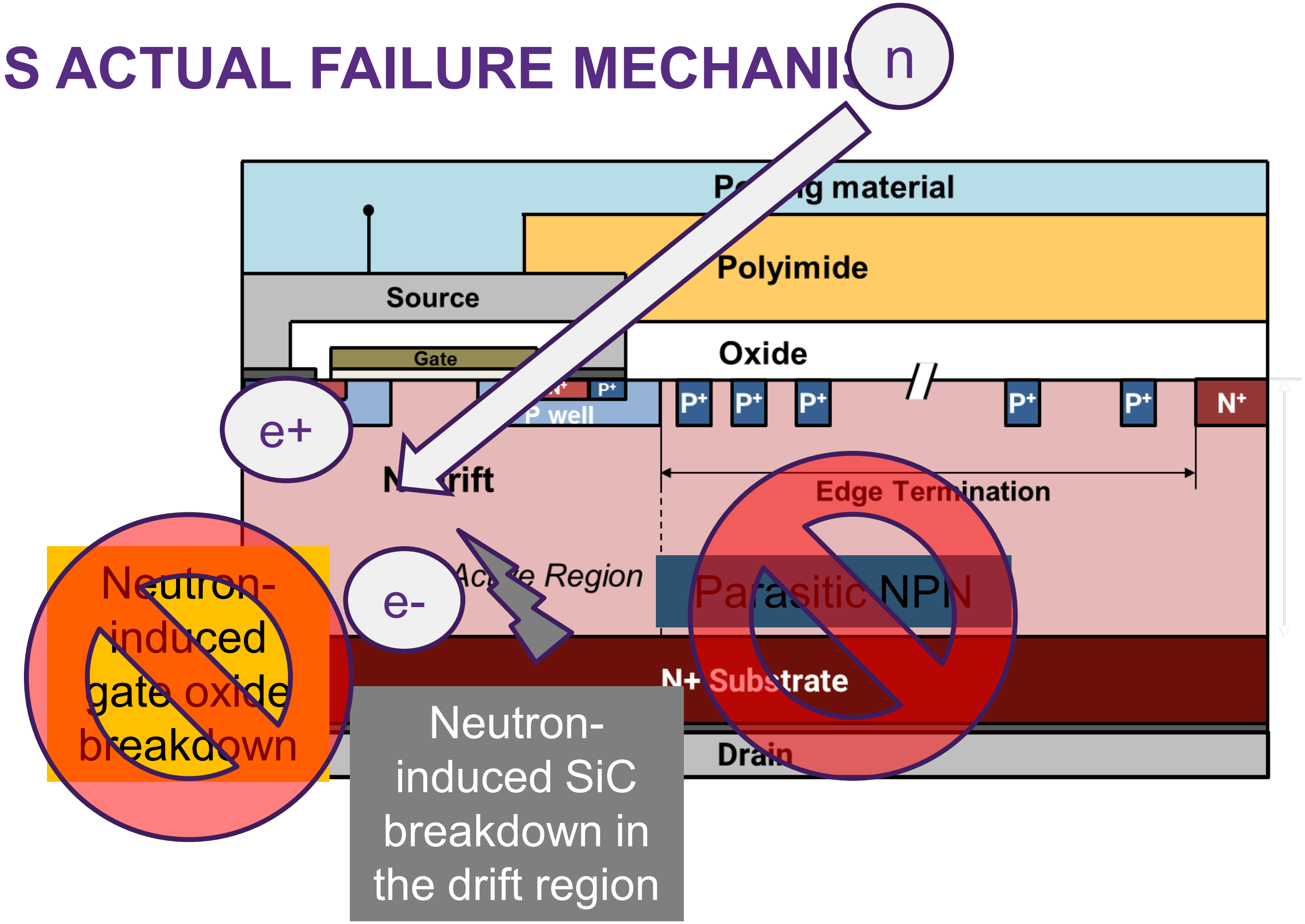
- MOSFETs and diodes show the same neutron reliability:
- Active area & drift effects dominate reliability
- Failure analysis shows no indication of MOSFET parasitic NPN turn-on or gate oxide breakdown




D. Lichtenwalner et al., IRPS 2018

# TERRESTRIAL NEUTRONS ACTUAL FAILURE MECHANISM

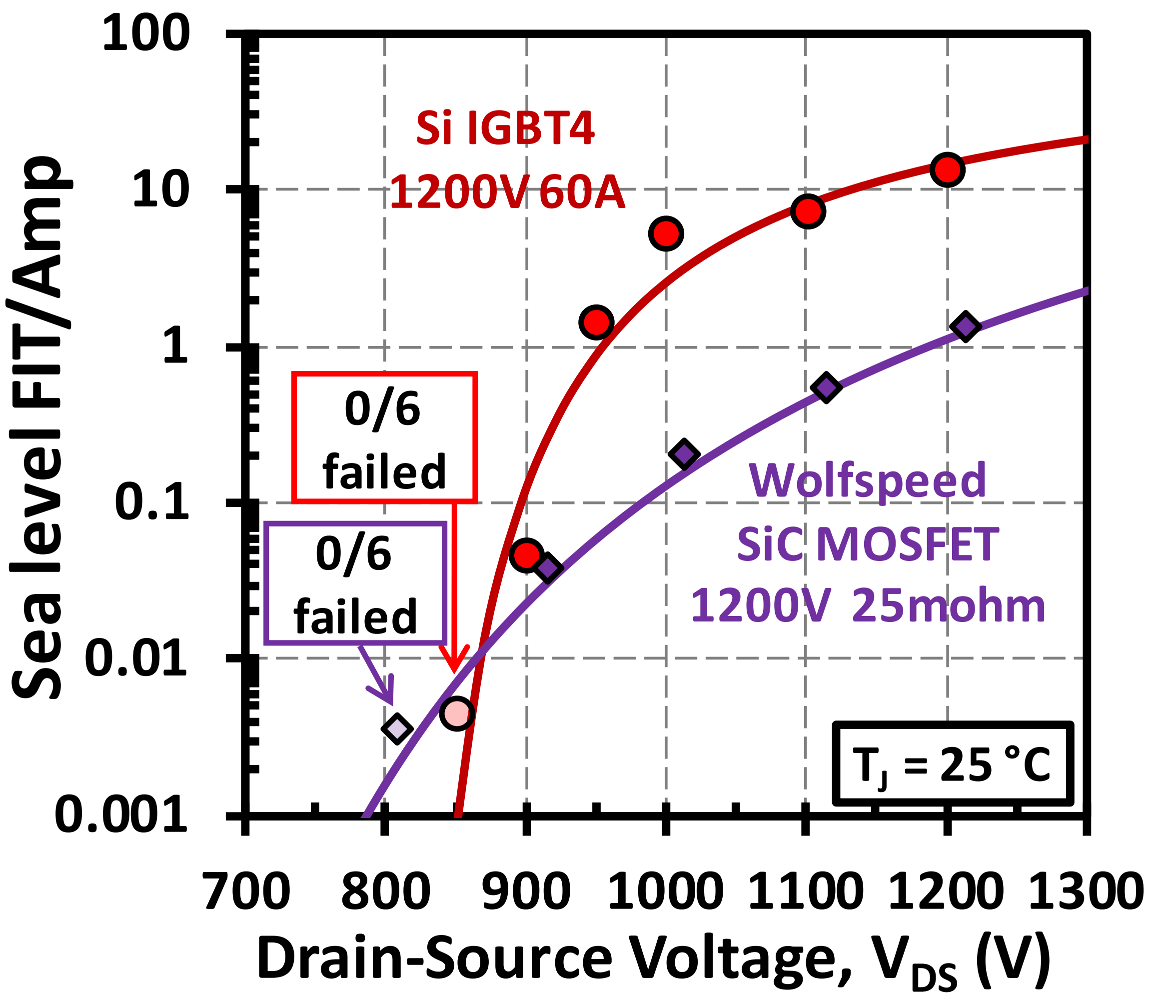
- Only drift-related breakdown is observed
- No gate oxide breakdown
- No parasitic NPN turn-on



# TERRESTRIAL NEUTRONS: SIC VS. SI

- Si IGBTs show sharper failure onset, but higher max failure rate
- Both the SiC & Si parts may require a VDS derating, but SiC is more immune to VDS overshoot

SiC MOSFET has 10X lower FIT rate at high $V_{DS}$




D. Lichtenwalner et al., IRPS 2018

# GATE VOLTAGE HAS NO EFFECT ON NEUTRON FIT RATE

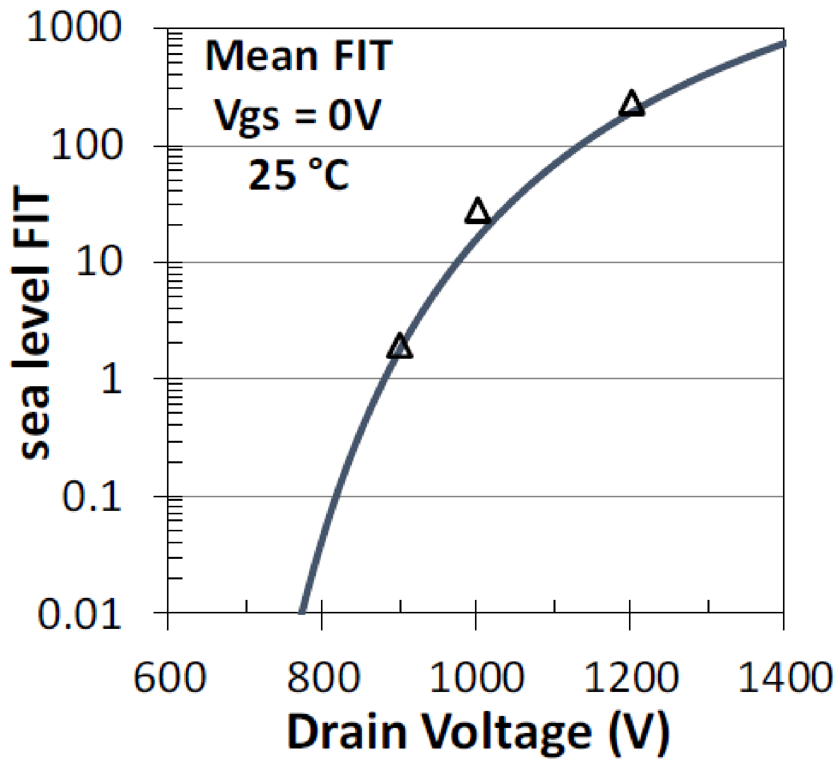



Fig. 1. Mean FIT versus $V_{DS}$ for Wolfspeed G3 1200V 16mohm SiC MOSFETs, with $V_{GS}$ = 0V. FIT rate is strongly dependent on the $V_{DS}$ value.

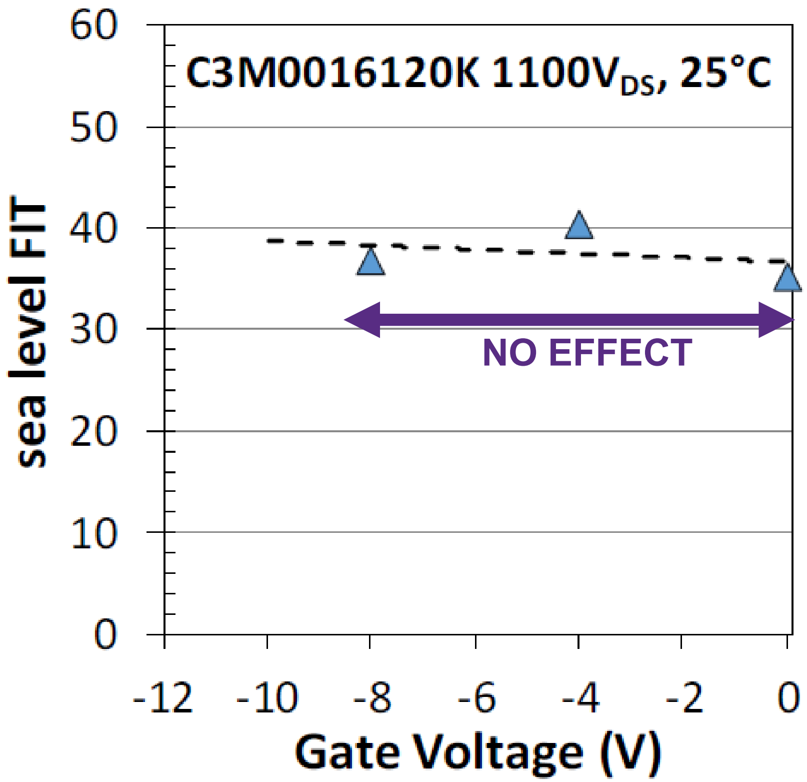



Fig. 2. Mean FIT versus $V_{GS}$ for Wolfspeed G3 1200V 16m SiC MOSFETs, with $V_{DS}$ = 1100V. FIT rate is weakly dependent on the $V_{GS}$ value.

D. J. Lichtenwalner et al., Wolfspeed, ECSRCM 2021 conference

# PRODUCT QUALIFICATION

# TYPICAL PRODUCT QUALIFICATION

| Stress | Abrv | Sample Size Per Lot | # of Lots | Reference (current revision) | Additional Requirements | Accept on # Failed |
|---|---|---|---|---|---|---|
| High Temperature Reverse Bias | HTRB | 77 | 3 | MIL-STD-750-1 M1038 Method A | 1000 hours at VDSmax and Tcmax | 0 |
| High Temperature Gate Bias | HTGB | 77 each Vgs>0 and Vgs<0 | 3 | JESD22 A-108 | 1000 hours at VGSmax and VGSmin and Tcmax | 0 |
| Temperature Cycling | TC | 77 | 3 | JESD22 A-104 | 1000 cycles Ta_max/Ta_min | 0 |
| Unbiased Highly Accelerated Stress Test | UHAST | 77 | 3 | JESD22 A-118 | 96 hours at 130 °C and 85% RH | 0 |
| High Humidity High Temp. Reverse Bias | H3TRB | 77 | 3 | JESD22 A-101 | 1000 hours at 85 °C, 85% RH with device reverse biased to 100 V | 0 |
| Intermittent Operational Life | IOL | 77 | 3 | MIL-STD-750 Method 1037 | 6000 cycles, 5 minutes on / 5 minutes off, devices powered to ensure DTJ ≥ 100 °C | 0 |
| Destructive Physical Analysis | DPA | 2 | 3 | AEC-Q101-004 Section 4 | Random sample of parts that have successfully completed H3TRB and TC | 0 |

# TYPICAL THB-80 ASSESSMENT

| Stress | Abrv | Sample Size Per Lot | # of Lots | Accept on # Failed | Reference (current revision) | Additional Requirements |
|---|---|---|---|---|---|---|
| Temperature-Humidity-Bias at 80% of Rated Voltage | THB-80 | 77 | 3 | 0 | NA | 1000 hours at 85 °C, 85% RH with device reverse biased to 80% of rated voltage |

# METHOD TO ASSESS A MISSION PROFILE

- Any mission profile can be evaluated using the operational conditions, known failure mechanisms and acceleration factors
- It can be assessed if the product qualification performed is sufficient to represent a lifetime test of the product in the application
  - In most cases we have examined, the answer is: “Yes, it is!”

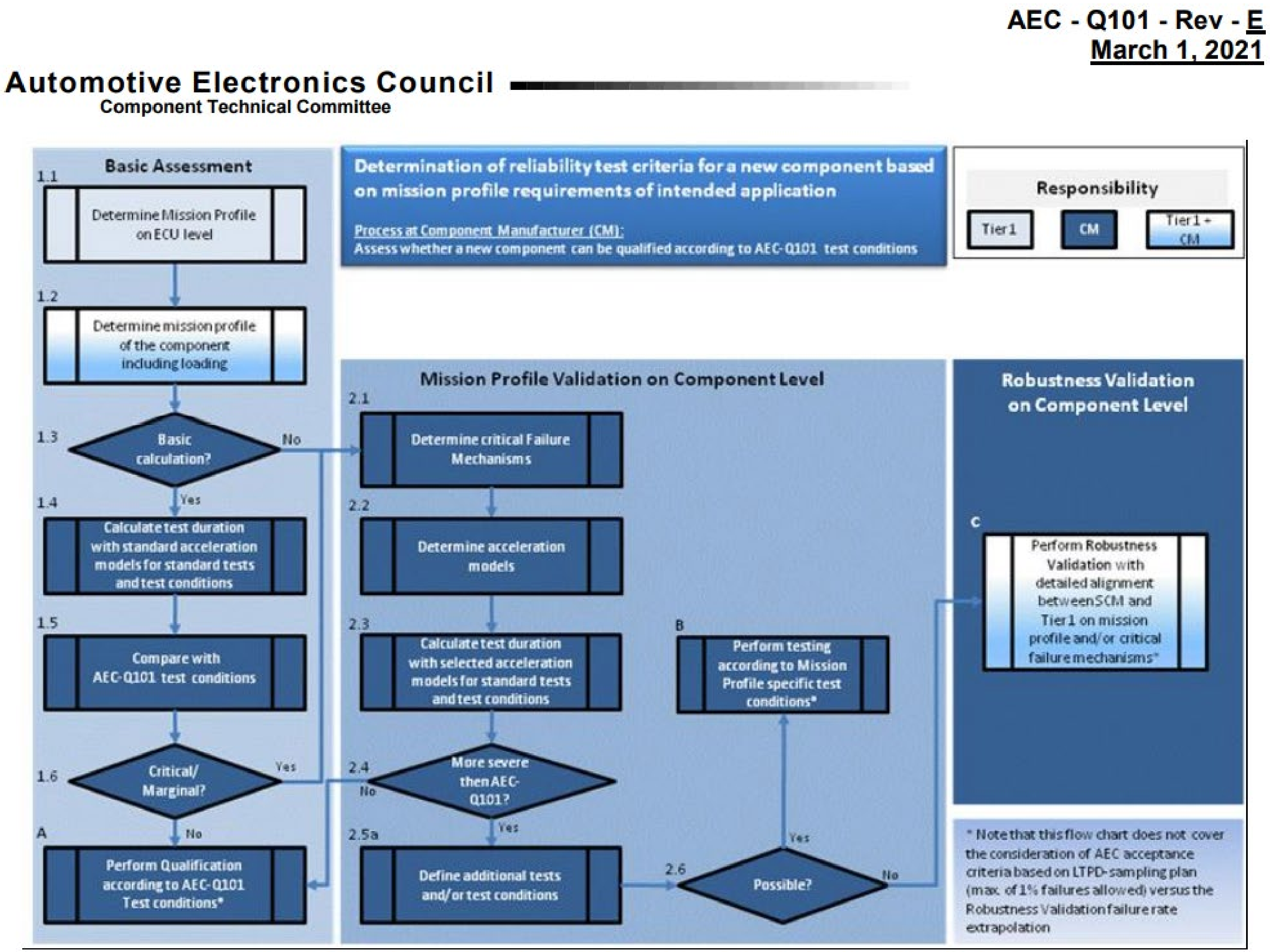
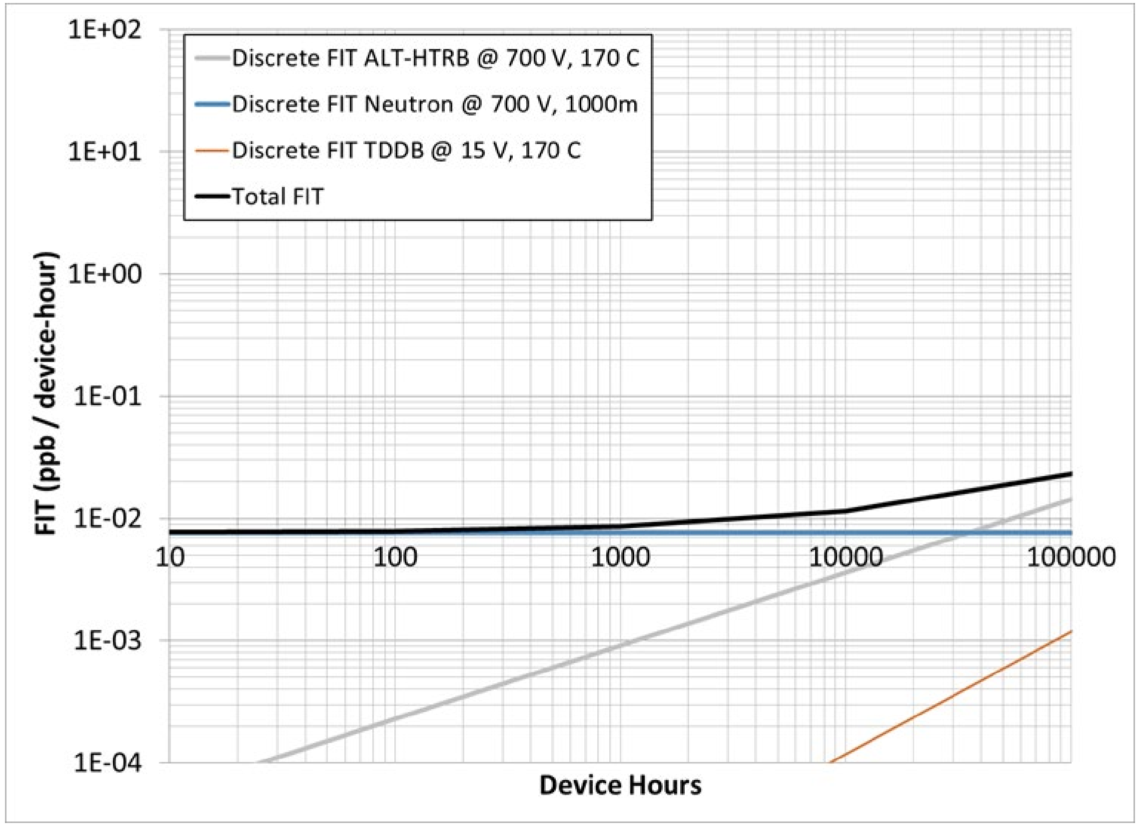


Figure A7.1: Flow Chart 1 – Reliability Test Criteria for New Component

# PUTTING IT ALL TOGETHER – MISSION PROFILE AND RELIABILITY PREDICTION

- The mission profile can also be translated into a FIT rate versus time, using the operational conditions, known failure mechanisms and acceleration factors
- This kind of computation can be very illustrative and can assist with system level reliability assessments



# FIELD RELIABILITY

# WOLFSPEED POWER FIELD RELIABILITY (THRU APR 2021)

| Technology | Fielded Device Hours (Billions)* | FIT Rate (valid field failures per billion device hours)** |
|---|---|---|
| C3Dxxx060 Diode | 6282 | 0.04 |
| C4Dxxx120 Diode | 1096 | 0.16 |
| C6Dxxx120 Diode | 2.16 | 1.85 |
| C2M MOSFET | 202 | 2.14 |
| C3M MOSFET | 99 | 1.21 |
| E3M Automotive MOSFET | 1.19 | 0* (no reported field failures) |

- *Calculated today's date minus confirmed ship date minus 90 days (allowing for time to put into service)
  * 12 hours per day
- **Calculated as: 2 times the number of valid field failures (excludes engineering evaluations, as-received visual defect escapes or issues, as-received test escapes, packaging and assembly quality issues) divided by fielded device hours; includes an additional factor for statistical confidence margin

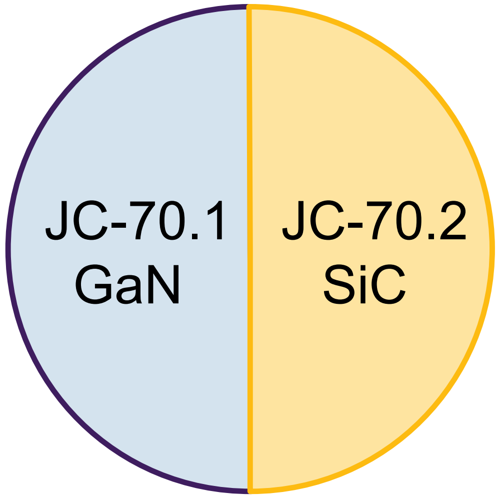
# INDUSTRY CONSORTIA GUIDELINES AND STANDARDS

# INDUSTRY CONSORTIA

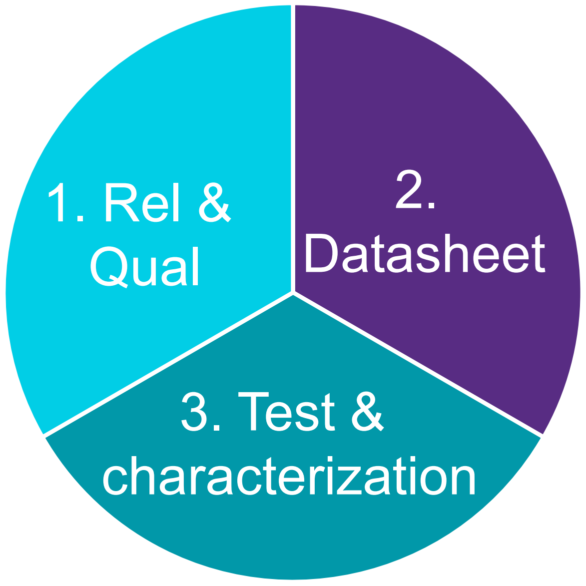
| Consortium | Abbreviation |
|---|---|
| Joint Electron Device Engineering Council | JEDEC |
| Automotive Electronics Council | AEC |
| International Electrotechnical Commission | IEC |
| Japan Electronics and Information Technology Association | JEITA |

# JEDEC

- JC-70 committee formed to create guidelines (JEPs) and standards (JESDs) for power electronic conversion semiconductors (PECS)
- Each subcommittee has 3 task groups (TGs)
- TG702_1: SiC reliability and qualification
  - Kicked off activities at WIPDA 2017
  - Charter established, Teams formed to work on guidelines first, to be followed by standards
  - Currently > 80 members from >36 member companies + SMEs
  - Contact me if interested in participating!
- Task groups are open to paid member companies
  - Also welcome participation from subject matter experts from non-member entities, such as academia
- More guidelines and standards are under development!




Task Groups



# PUBLISHED: NEW JEDEC GUIDELINE ON BTI FOR SIC MOSFETS

**JEDEC PUBLICATION**

**Guideline for evaluating Bias Temperature Instability of Silicon Carbide Metal-Oxide-Semiconductor Devices for Power Electronic Conversion**

**JEP184**



MARCH 2021

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

# CONCLUSION

# CONCLUSION

- SiC power devices have some unique reliability considerations in addition to Si power devices
- Reliability assessments need to be holistic, comprehensive and specific
- The SiC failure mechanisms have been identified and testing methods have been developed, but more work needs to be done
- Successful product qualifications and field reliability show that the reliability science is paying off, and SiC is ready for large volume manufacturing for high reliability applications – the future is now!
- Industry-wide reliability guidelines and standards are being actively developed

**“ We harness the power of Silicon Carbide to change the world for the better. ”**

# THANK YOU