Optimizing SiC MOSFET Chip and Packaging Design to Match Specific Application Requirements

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2010

Si IGBT Low V_{CESAT}

UPS

Si IGBT Low Switching Loss

Motor Drives

2025?

Si IGBT Automotive

???

SiC MOSFET Solar

SiC MOSFET
Energy Storage

SiC MOSFET
Avionics

Si IGBT Servo Drives

Program

Introduction

Applications:

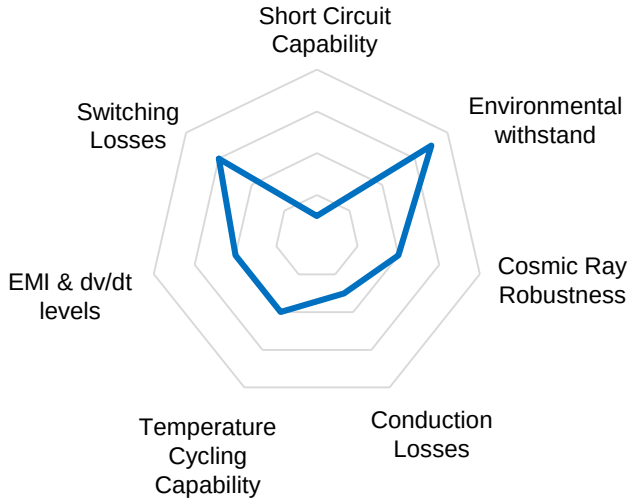
- **Aviation - Cosmic ray robustness.**
- **Servo Motor Drives - Short circuit capability.**
- **Traction/CAV - Low conduction losses.**
- **ESS and Chargers - Low switching losses.**
- **Automotive - Temperature cycling and EMI.**
- **What the future holds for SiC MOSFETs ?**

- **Q&A**

Overview

5 Applications

7 Key Parameters

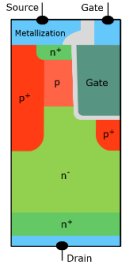


Note Spider diagram "scores" are somewhat subjective

3 Aspects for consideration by design engineers

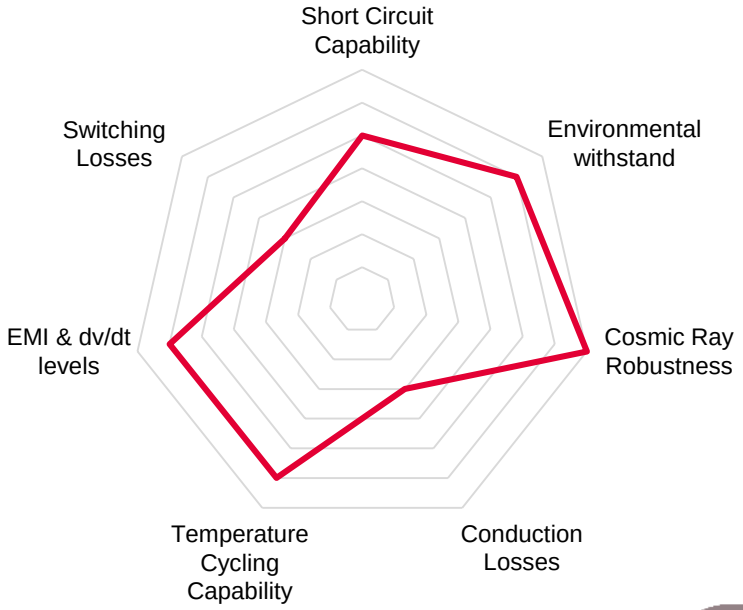
What are the challenges?

Tools to meet challenges



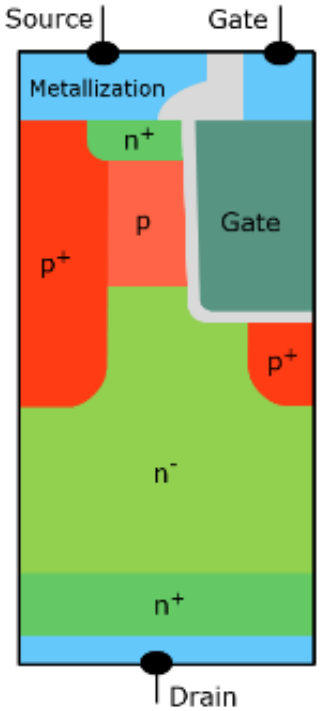
A good fit?

Seven Design Aspects for a Power Converter

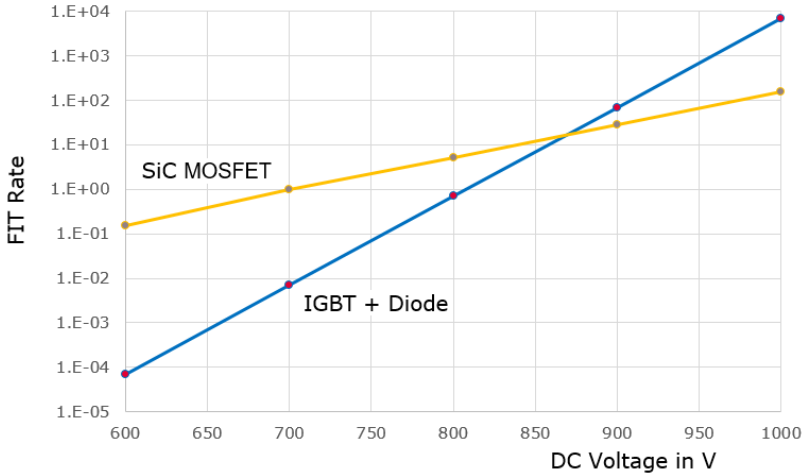


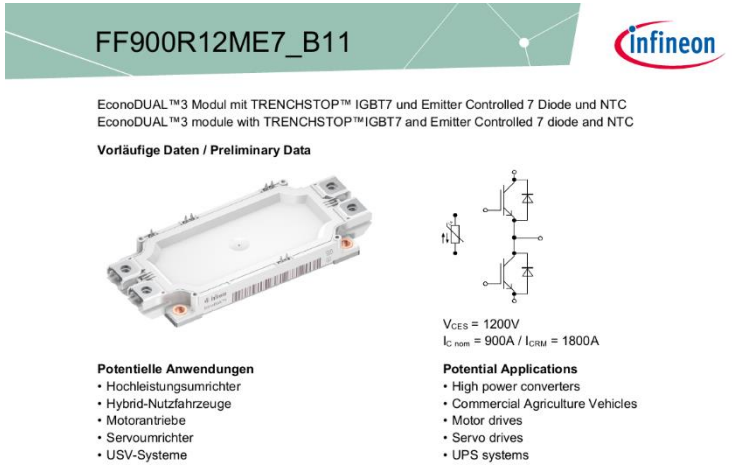
What are the challenges?

What tools do we have to meet the challenges

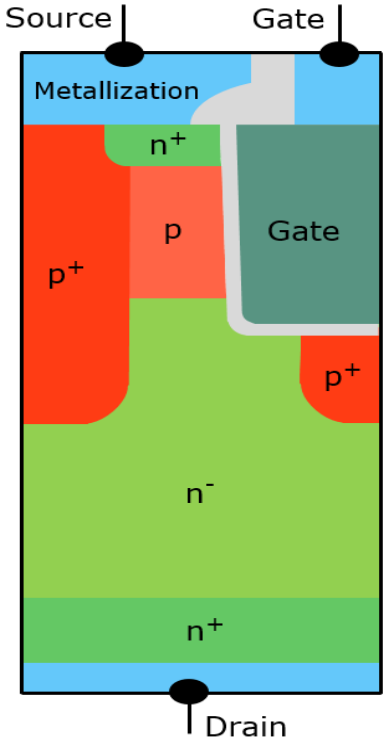


How to ensure a part is a good fit for the end application?





SiC MOSFET – Basic Properties



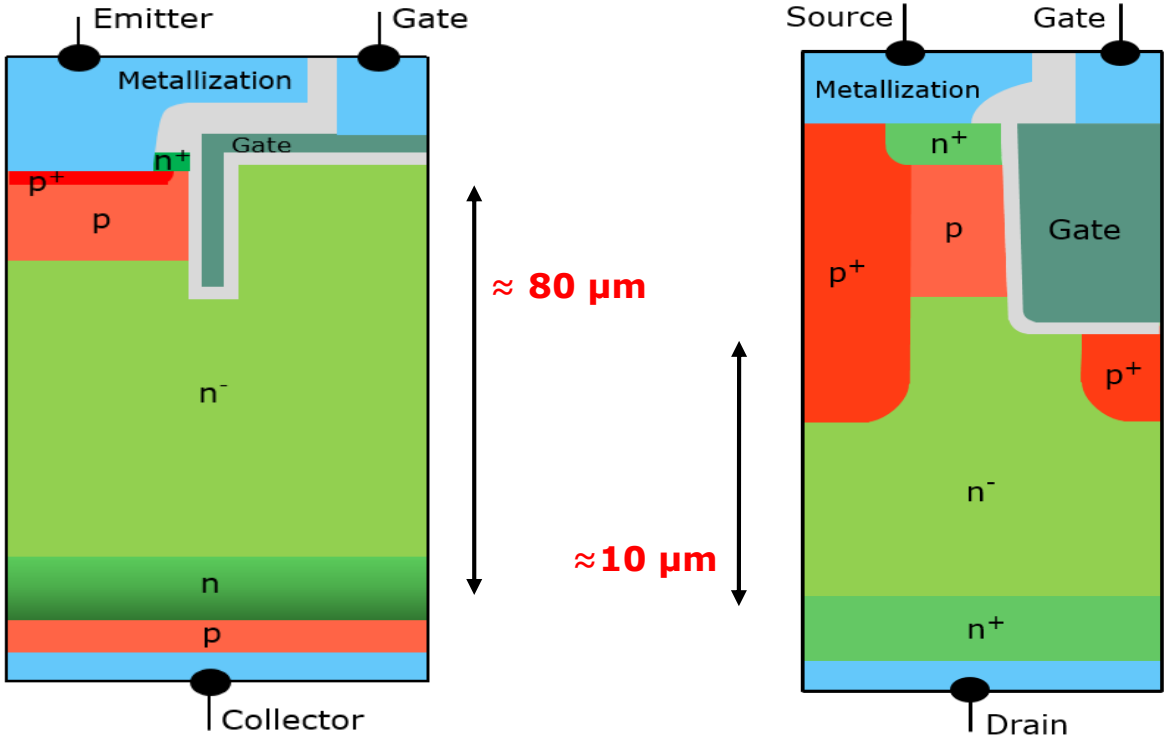
Compared to a Si switch

- There is also a MOS (trench) cell on top of a SiC switch
- However the n^- drift zone can be built much thinner and doped at a higher level resulting in lower Ron and lower switching losses

physical properties	4H-SiC	Si
band gap [eV]	3.26	1.12
break through field [MV/cm]	~2.5	0.25
thermal conductivity [W/cm/K]	~3.4	1.5
ideal bulk mobility [cm²/V/s]	800/115	1400/450
electron saturation vel. [cm/s]	2e7	1e7

- Driftzone Thickness: SiC/Si: ≈ 1/10
- Driftzone Doping: SiC/Si: ≈ 100/1

IGBT Transistor Cell Cross Section Typical sizes for a 1200 V device IGBT and SiC MOSFET



SiC MOSFET – Key Elements

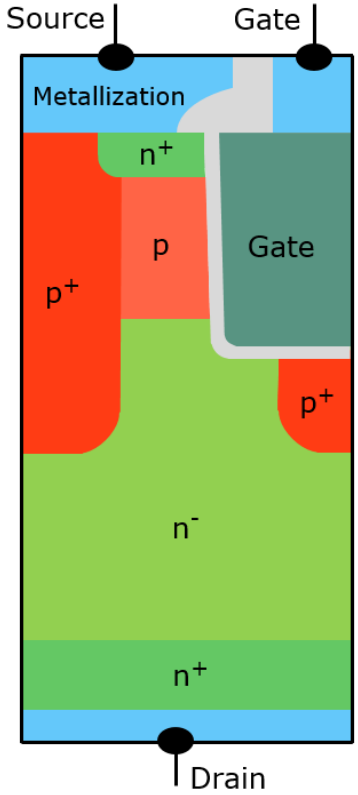
Trench Cell with

- MOS channel in a specific crystal orientation for a good channel mobility.
- Shielding of the gate oxide against high electric field strength in the on and off condition by special p^+ doping (to make the gate oxide stress comparable to Si devices).
- p^+ doped layer also serves as a good body diode (“p-emitter“).

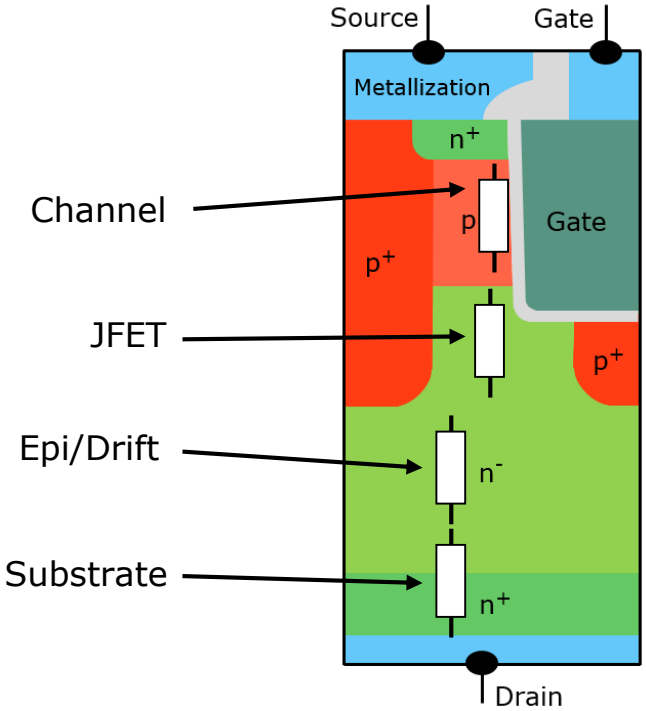
Drift Zone with adequate

- Thickness
- Doping

To ensure required blocking voltage combined with low on state resistance**.**



SiC MOSFET – Four Main Components of R_{DSON}



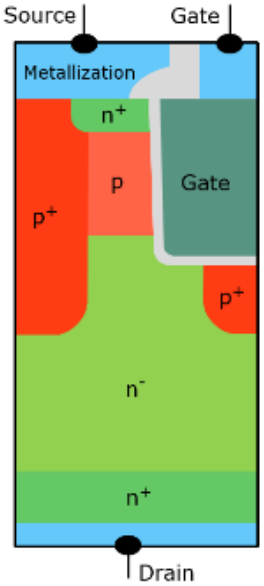
Overview an Example

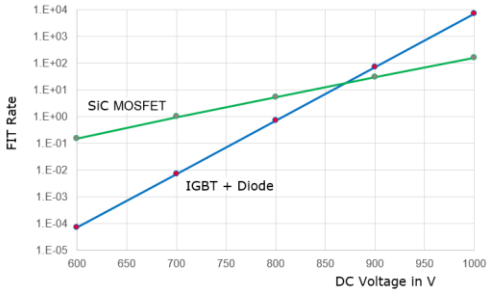
Application
Aviation

Challenge -
Cosmic radiation

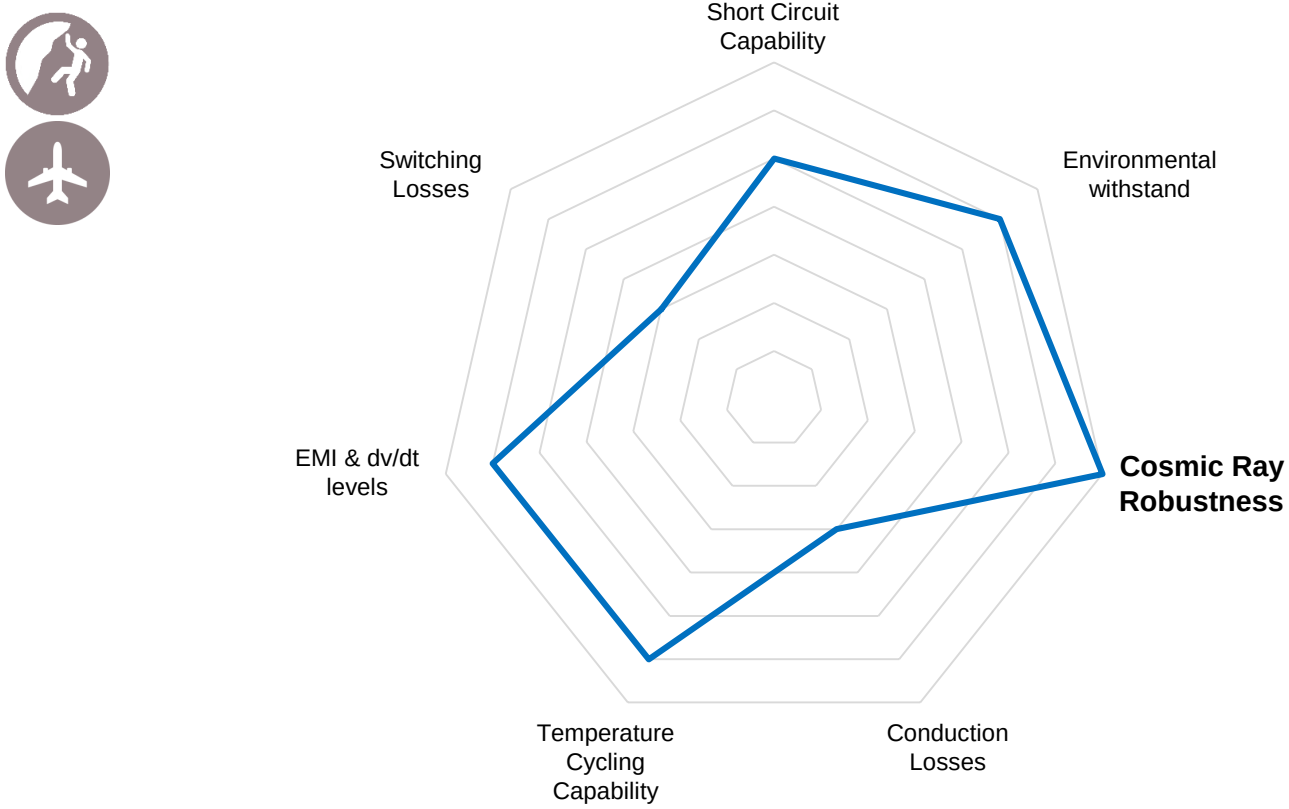
Tools -
Chip Design

A good fit -
Qualification Data

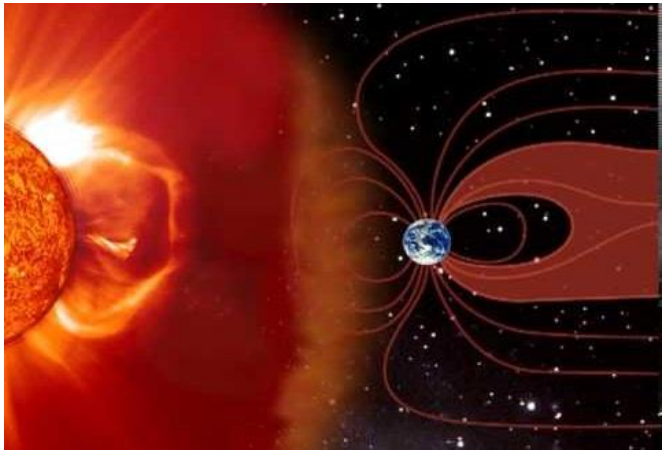




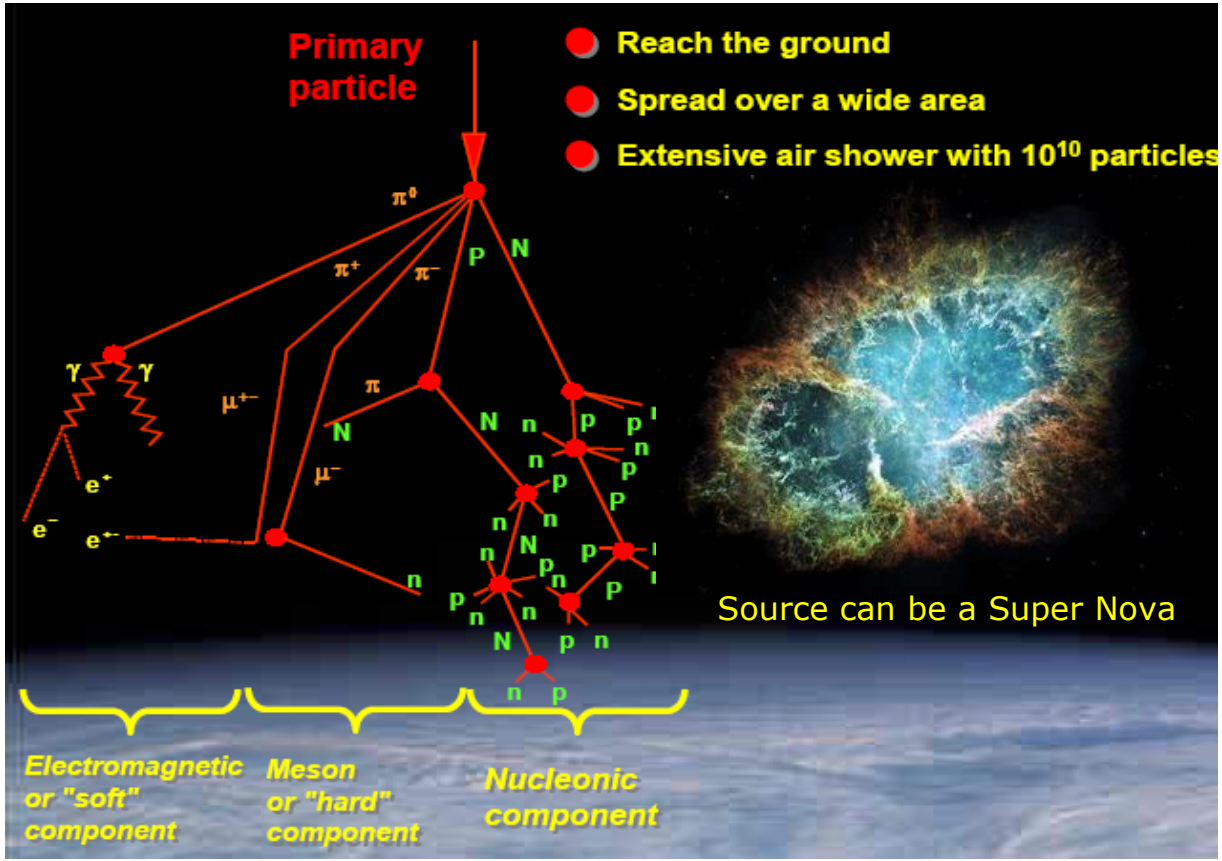
Aviation- Spider Diagram



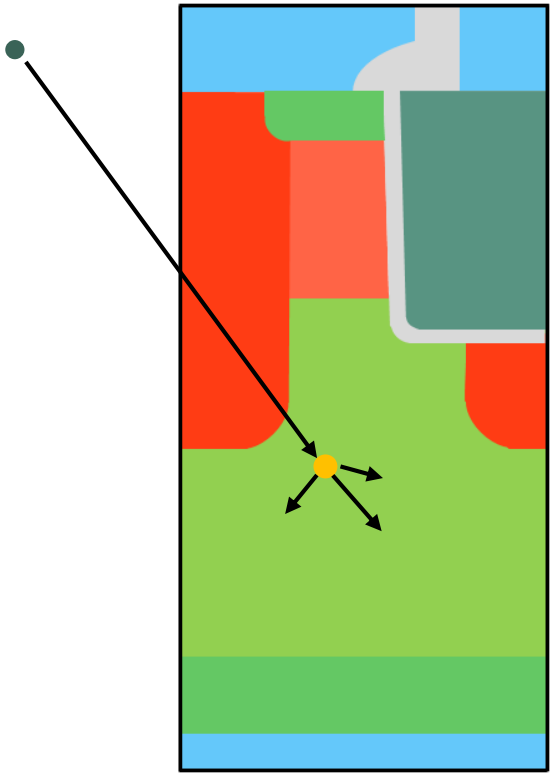
What is **C**osmic **R**adiation CR?

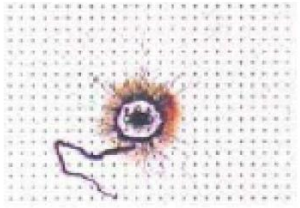


Cosmic **R**adiation CR



Cosmic Radiation

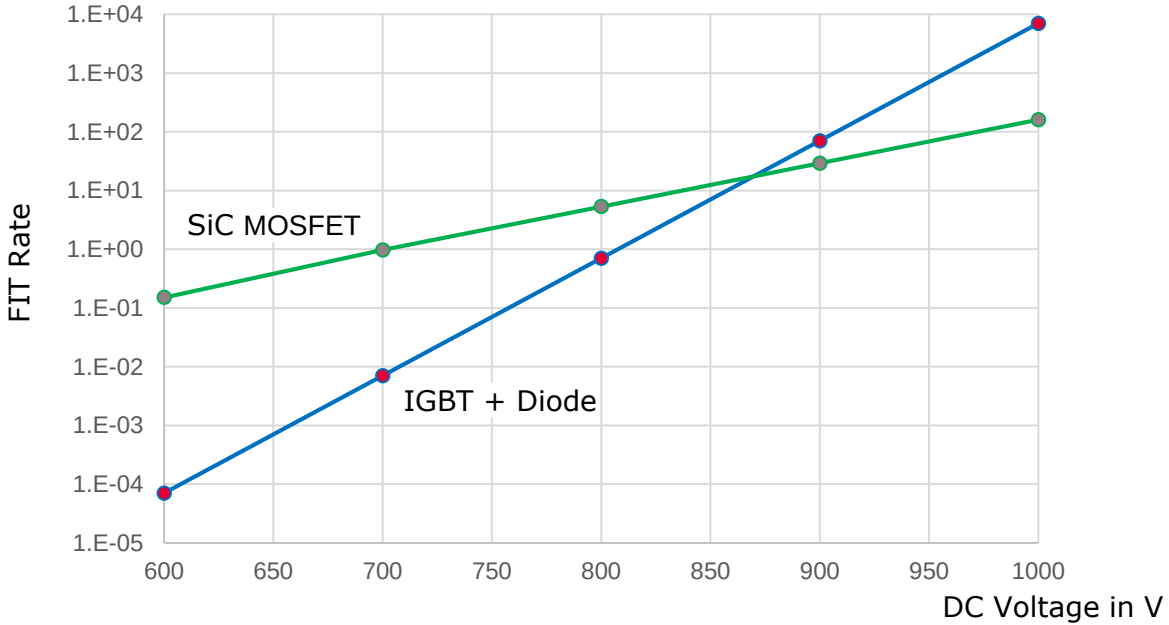




Top side view
of a failure

1 FIT (**F**ailures **I**n **T**ime) = one failure in 10^9 operation hours of the device.
Note only in reverse blocking condition

Typical CR FIT Values for a 1200 V 200 A Si and SiC Based Half Bridge at 25 °C and Sea Level

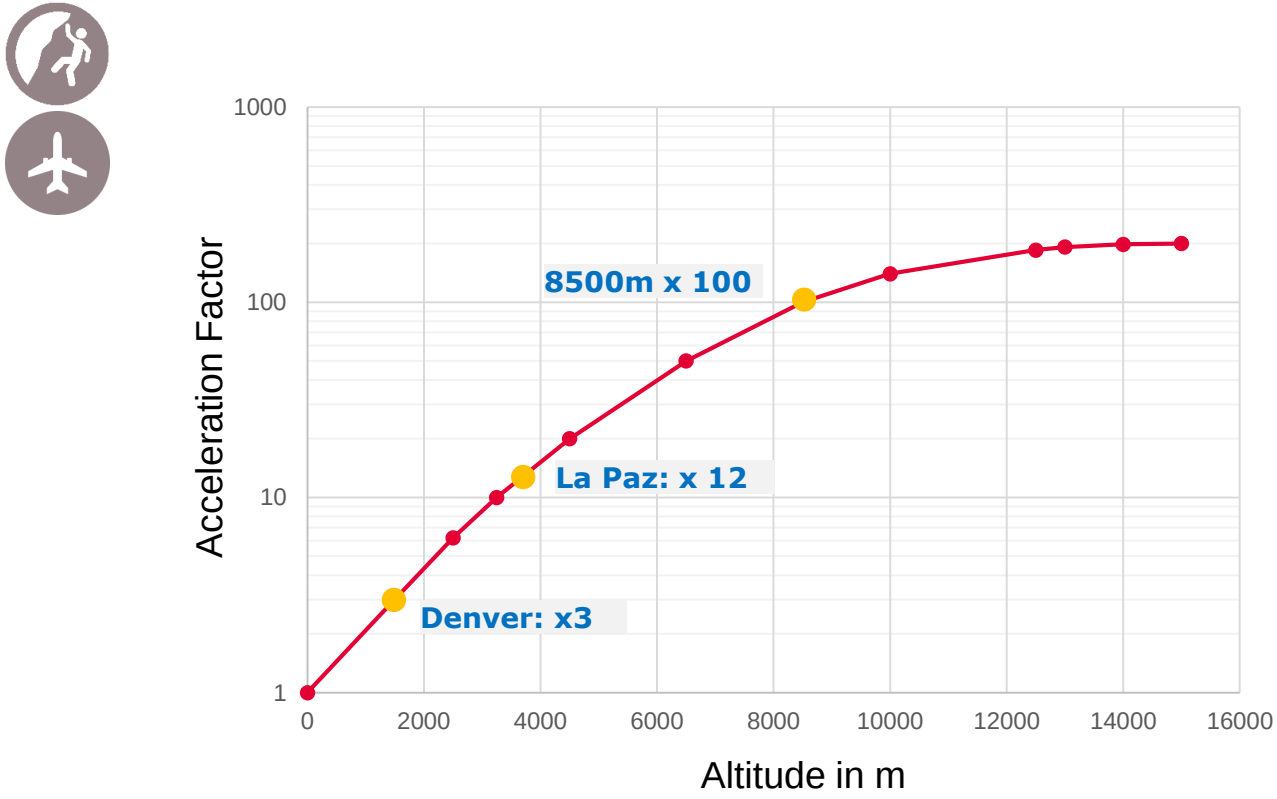


Some differences between SiC MOSFET and Si IGBT + Diode:

- The SiC MOSFET has a smaller active area than the Si IGBT/Diode for the same current, does not need a free wheeling diode, has a much thinner drift zone, but higher electrical field strength.

In this specific example for 1200V class devices the SiC MOSFET has a flatter gradient than the equivalent Si device, however in most cases (depending on the choice of devices and voltage classes) the slopes are quite similar.

So Why Aviation?



So What is the Failure Rate? An Example.

A single module has a failure rate of 10 FIT at sea level

➡ Each converter has 6 modules = 60 FIT

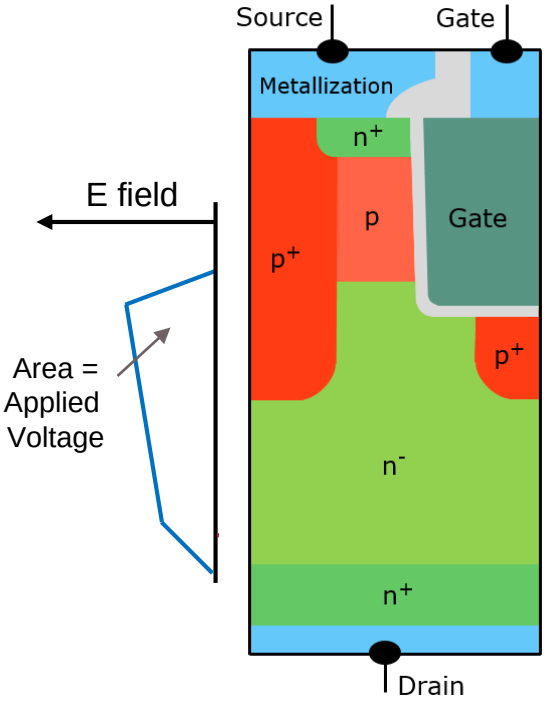
➡ Each aircraft has 8 converters = 480 FIT

➡ Aircraft at 8500m altitude = 48,000 FIT

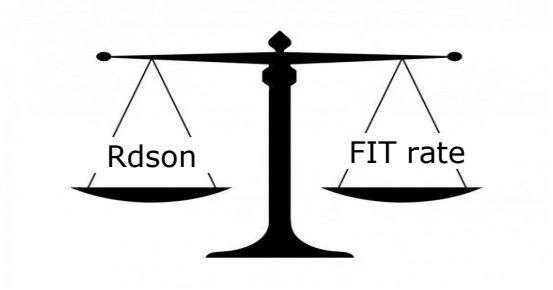
➡ A fleet of 100 aircraft = 4,800,000 FIT

So if each plane operates at altitude 6 hours a day there could, statistically, be a failure every month.

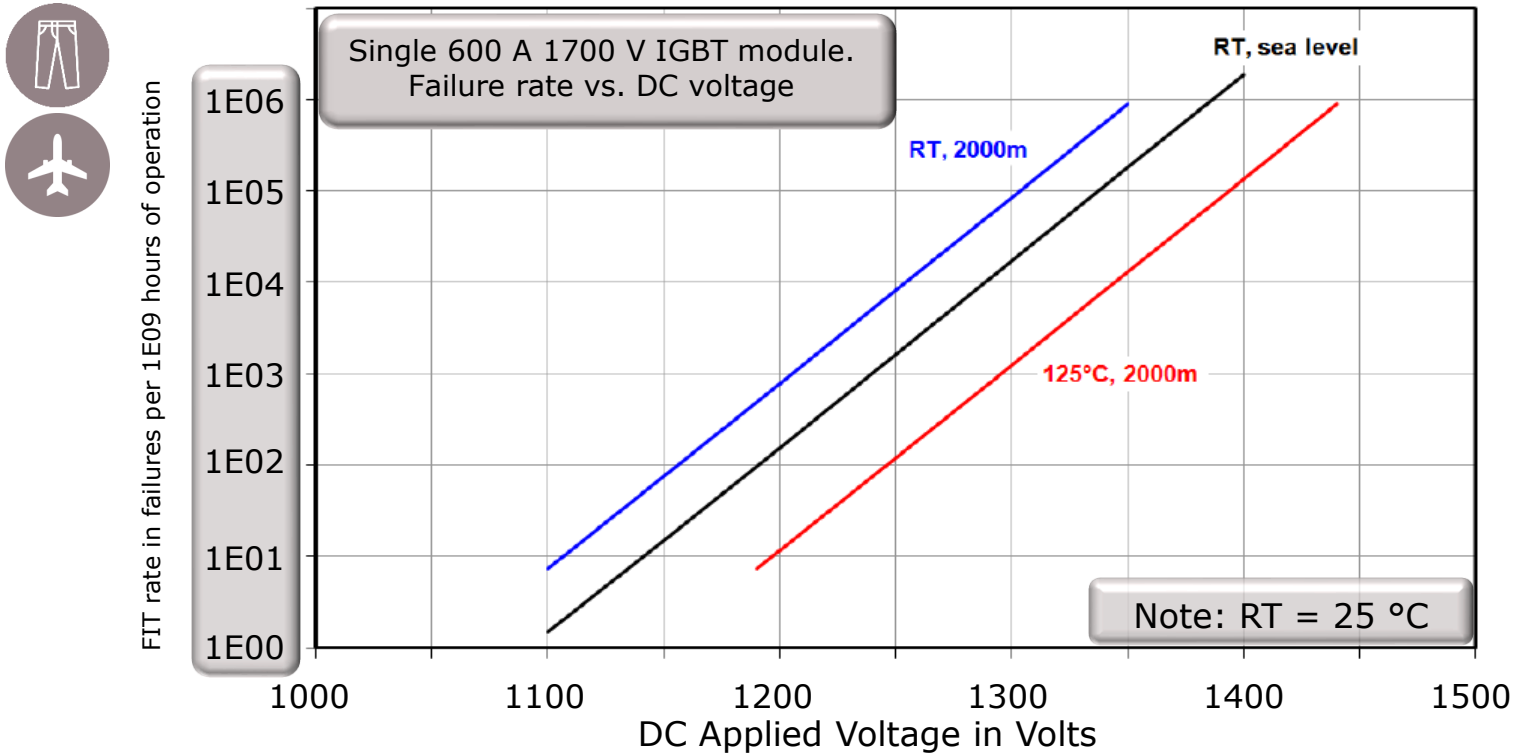
Chip Design Tools



Key is to reduce the field strength in drift region. This can be done by doping in the drift region to flatten out the electric field. The area is still the same the but peak lower.

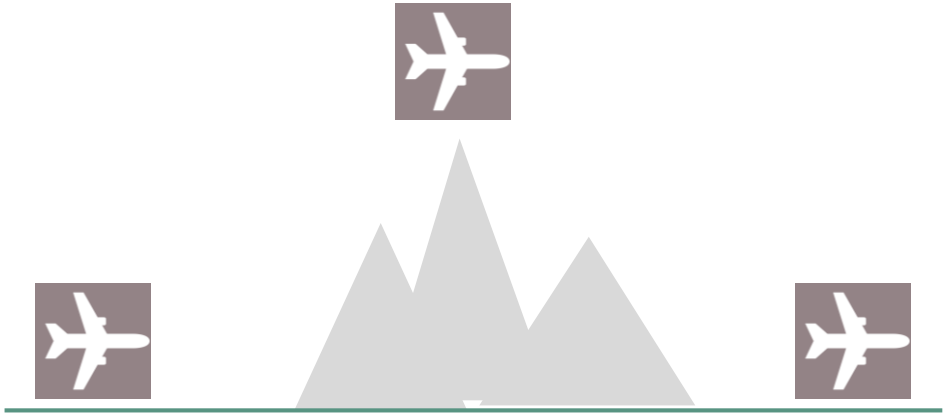


Cosmic Radiation Failure Rates – Typical Values



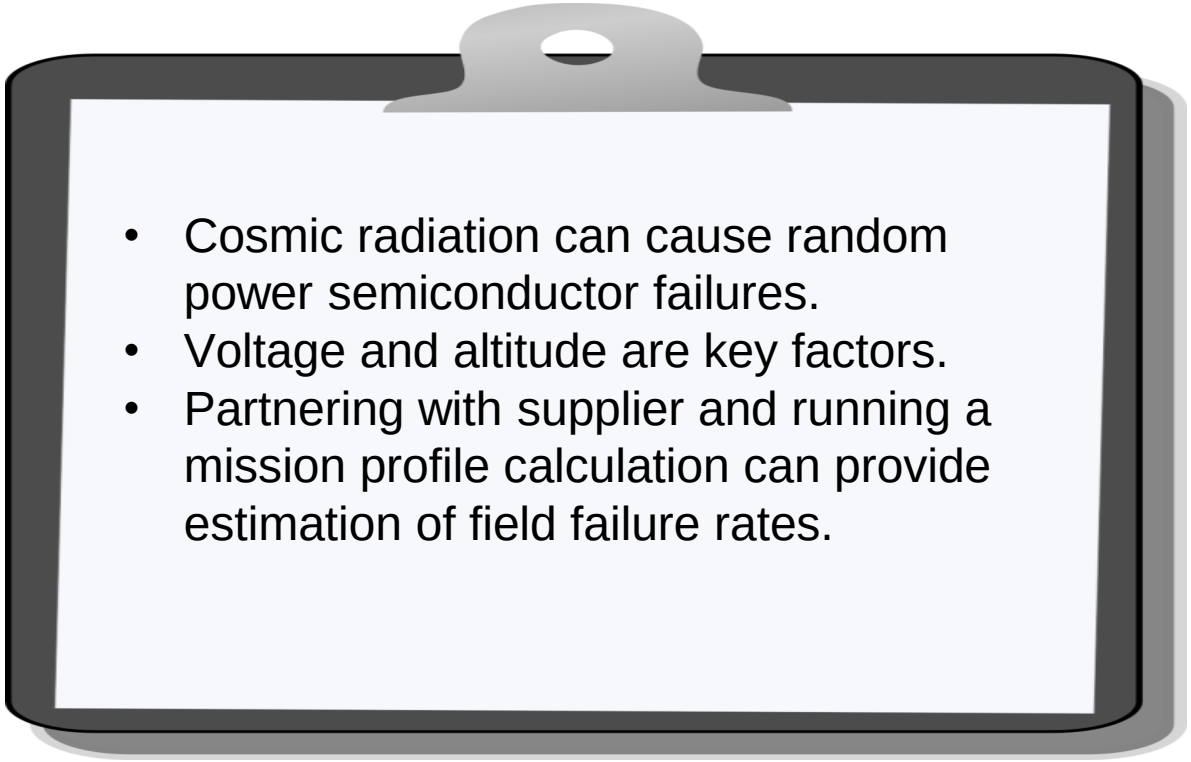
FIT rate for this Si IGBT reduces with: lower voltage, lower altitude and higher temperature.

Failure Rate Estimation Using a Mission Profile



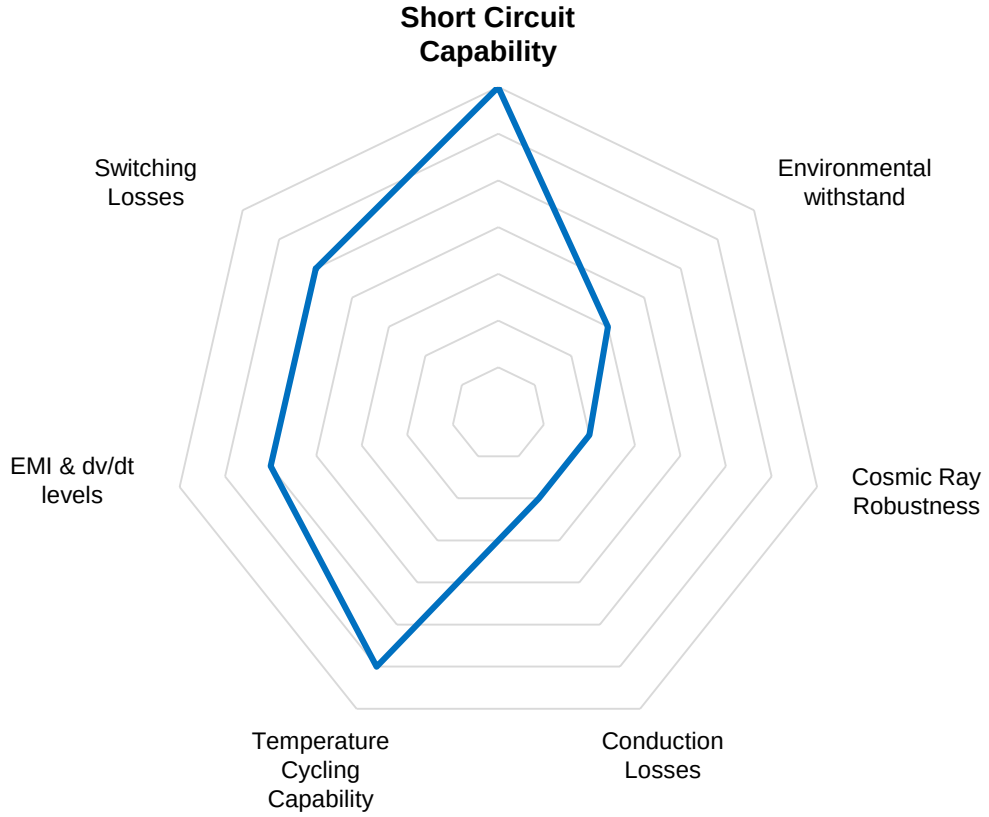
Time each Day in minutes	Altitude in m	Applied Voltage in V	Temperature in °C	FIT rate per day per module
30	5000	800	75	0.002

Summary



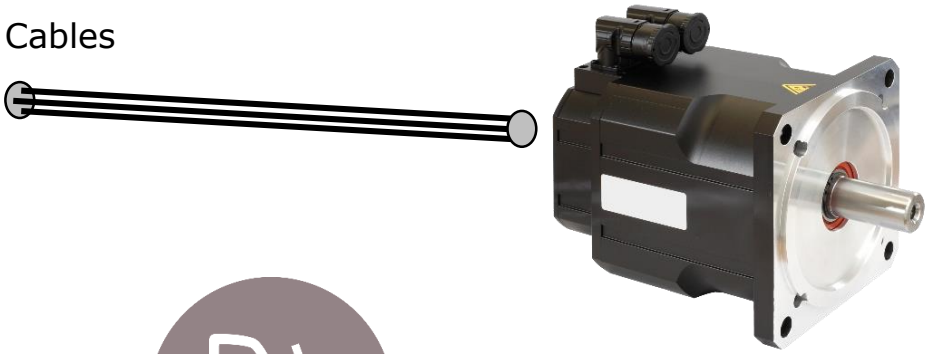
- Cosmic radiation can cause random power semiconductor failures.
- Voltage and altitude are key factors.
- Partnering with supplier and running a mission profile calculation can provide estimation of field failure rates.

Servo Drives - Spider Diagram

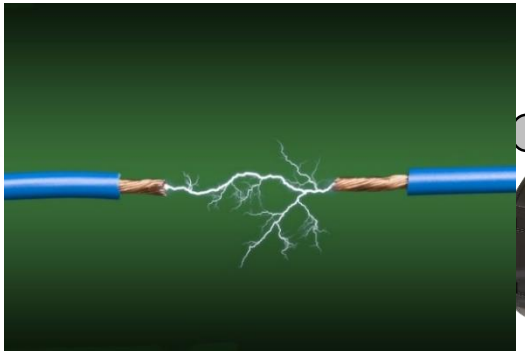


Why Do Servo Motors Need Short Circuit Protection?

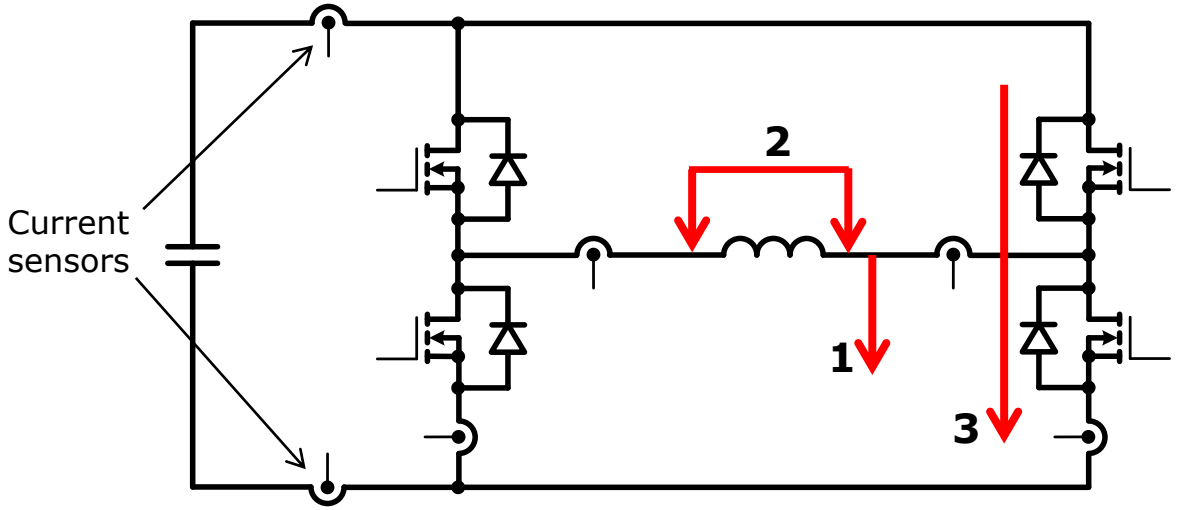
Cables



Why Do Servo Motors Need Short Circuit Protection?



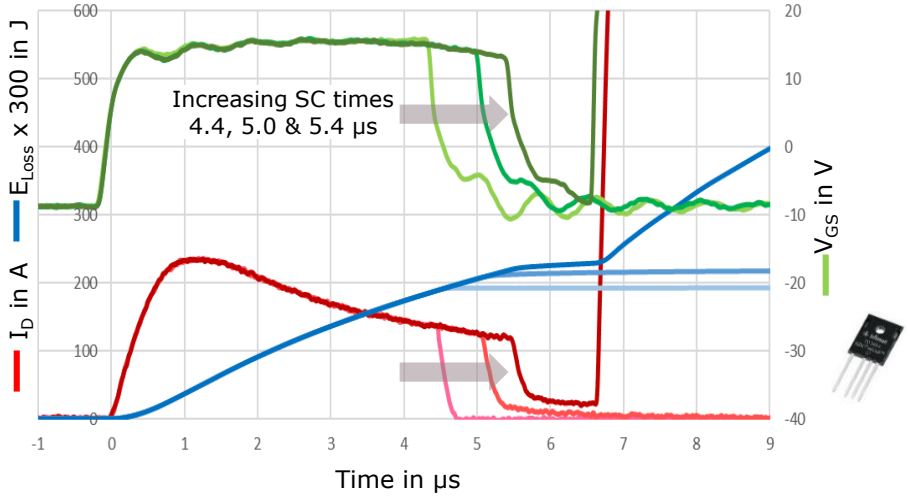
Short Circuit – Three Main Paths



Three main short circuit Paths:
1. Phase to ground
2. Phase to phase
3. Shoot through

Three main locations for current sensors:
- DC Bus
- Power Source
- Output Phase

SiC MOSFET Short Circuit Testing

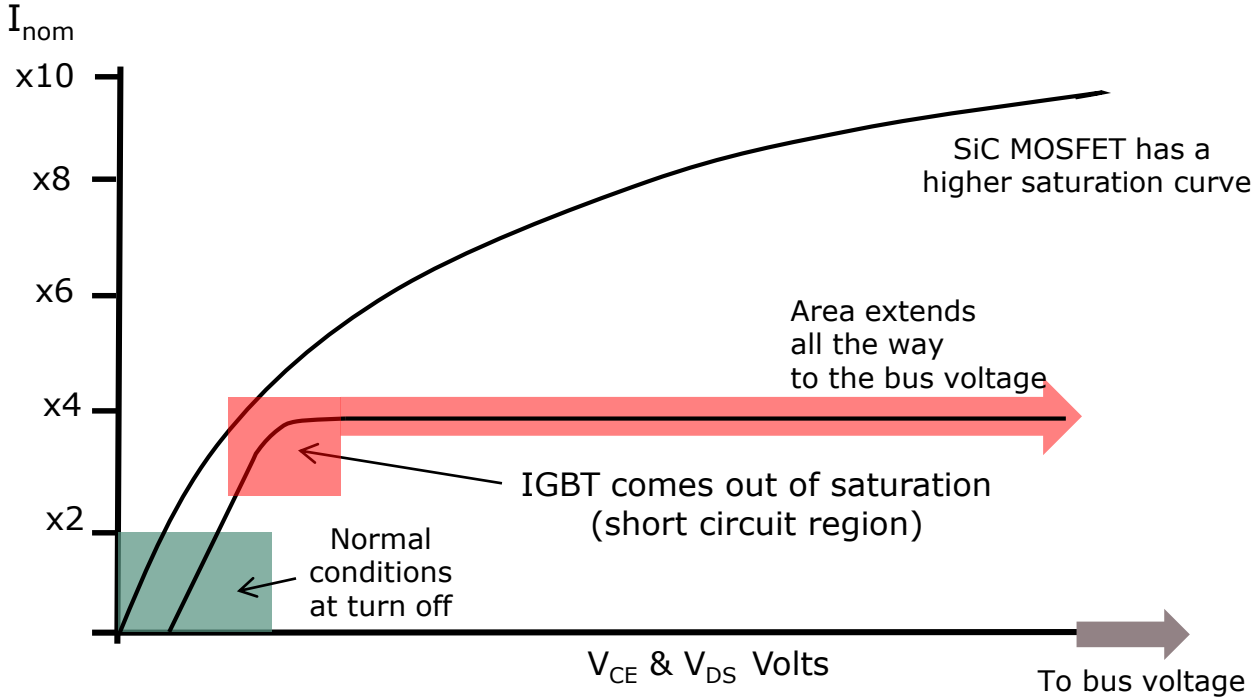


Operating point: V_{GS} =-9 V / +15 V.
VDC=800 V, Isc=240 A@ 25 °C

Failure at
5.4 µs

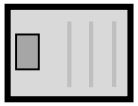
Why More of an Issue for SiC MOSFETS?
Typical IGBT and SiC MOSFET De-Saturation

Short circuit conditions can be detected by measuring the V_{CE} or V_{DS} value when the IGBT/MOSFET is turned on. The IGBT comes out of saturation at lower I_{nom} current levels.

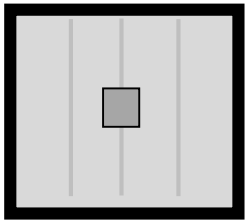


Why More of an Issue for SiC MOSFETS?

Smaller chip size

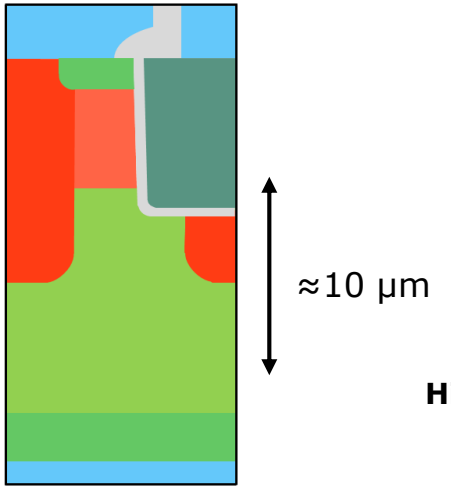


100 A SiC MOSFET
Total Area ≈ 30 mm²



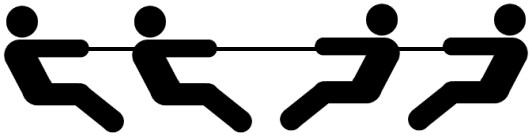
100 A IGBT
Total Area ≈ 115 mm²

Losses in thin layer

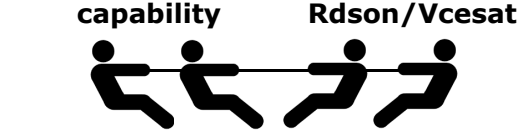


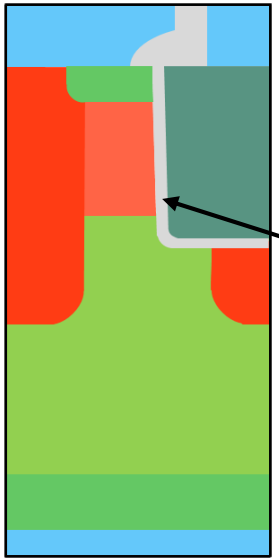
Higher short circuit capability

Lower Rdson



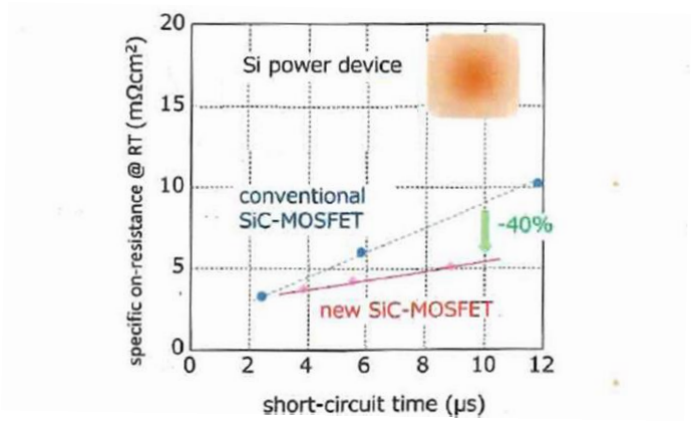
Chip Design Tools to Influence Short Circuit Robustness





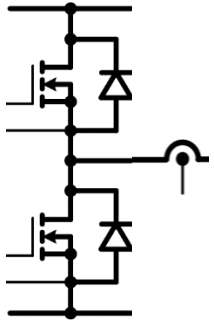
The longer channel and narrower the channel width the lower the short circuit current but higher the Rdson

Chip Design Measures to Influence the Short Circuit Robustness

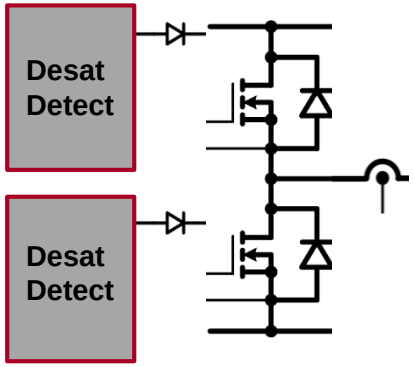


Curves showing Rdson vs. short circuit time for SiC MOSFET chip design. ([8])

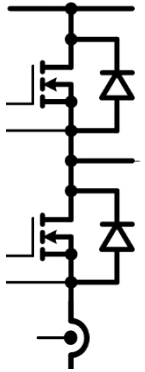
Short Circuit Protection Some Options



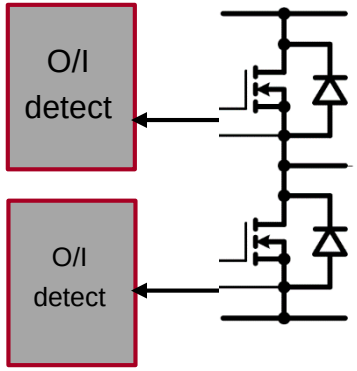
A) No desat detection
Fast current sensors
No shoot through protection



B) Desat detection

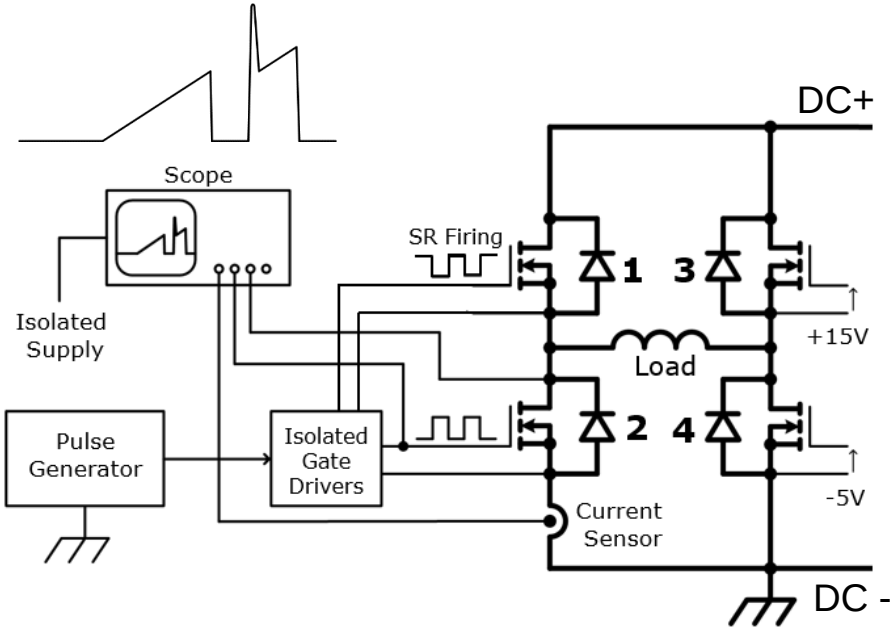


C) Fast emitter
Current sense



D) Chip and module with in-built over current protection.

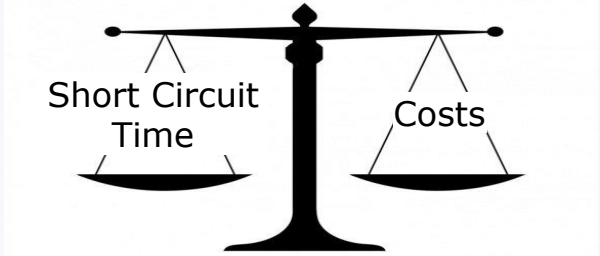
Short Circuit Capability Testing



Example of a Double Pulse Test DPT circuit ([9])

Summary

- Protection under short circuit conditions always has a cost either in terms of system layout, gate driver design or chip performance.
- If required check data sheet carefully and perform **D**ouble **P**ulse **T**est DPT of the device in situ.



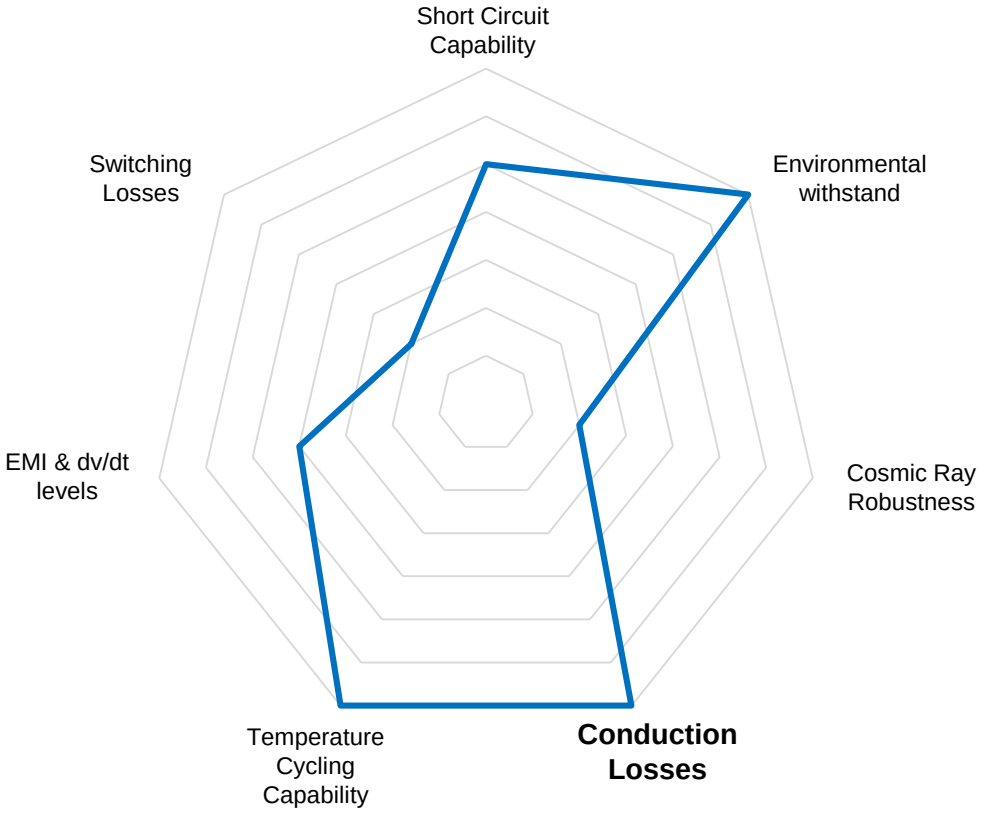

TRUCK


BORDEAUX
CLAVEAU

Requirements of Traction and **C**ommercial, **C**onstruction and **A**gricultural **V**ehicle CAV Drives

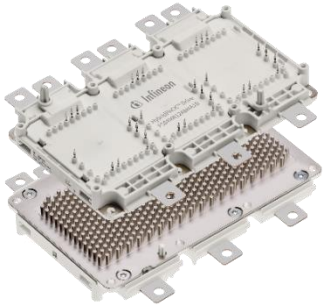
- Long Operating life >20 years and > 60,000 hours.
- High mechanical vibration and shock.
- High cyclical loads and high torque at zero speed/locked rotor.
- Low switching frequency and conduction losses dominate.

Traction Drives- Spider Diagram



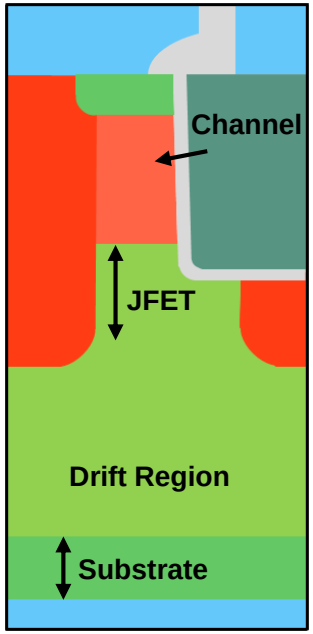
Why Conduction Losses are Dominant for High Power Traction Drives

A 1000A 1700V IGBT
Operating at 800 rms
500Hz Fsw.
Switching losses = 12%
Conduction losses = 88%

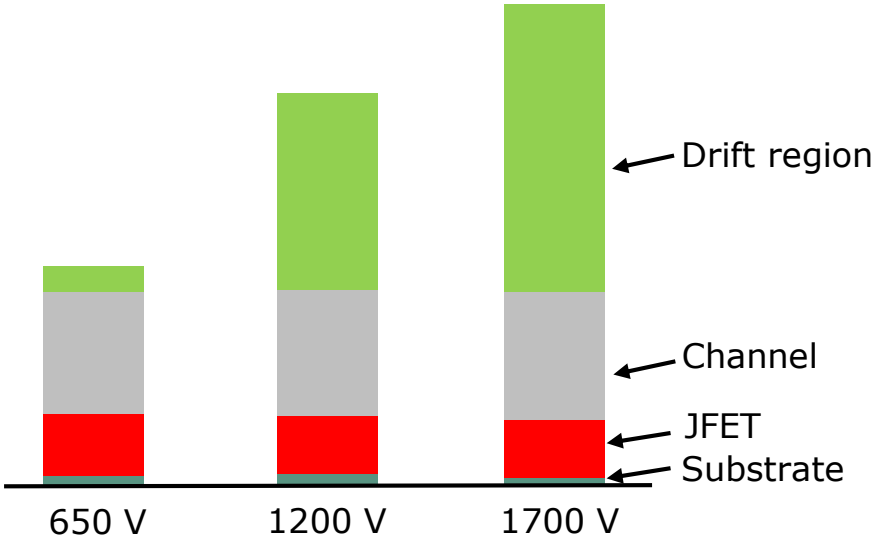


A 3 mΩ 1200V SiC MOSFET
Operating at 300 rms
2000Hz Fsw.
Switching losses = 20%
Conduction losses = 80%

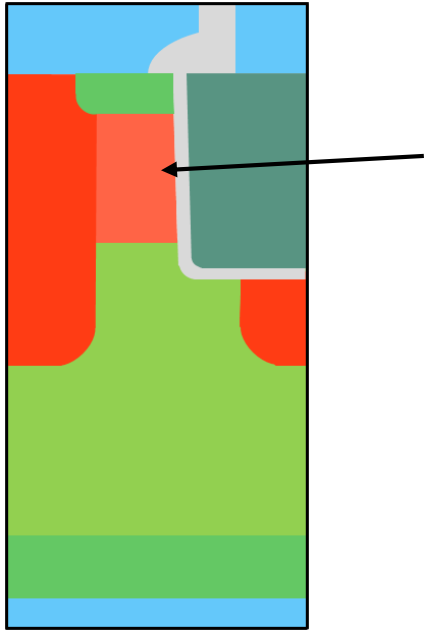
Components of R_{DSON} of a SiC MOSFET



Unlike IGBT R_{DSON} is ≈ linear with current

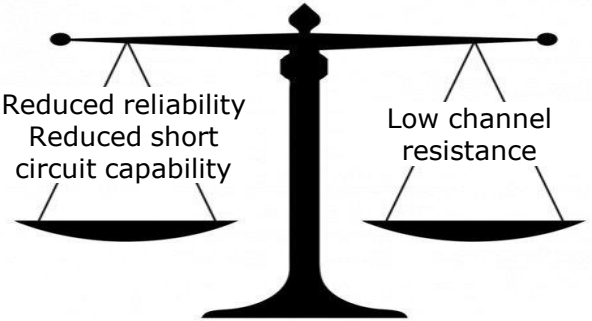


Tools for R_{DSON} Reduction - Channel



Trench gate at 4° for lowest level of crystal defects.

Channel: Higher gate voltage/thinner gate oxide layer = lower gate oxide reliability & lower short circuit capability



Paralleling Devices to Reduce Conduction Losses

Conduction Losses IGBT

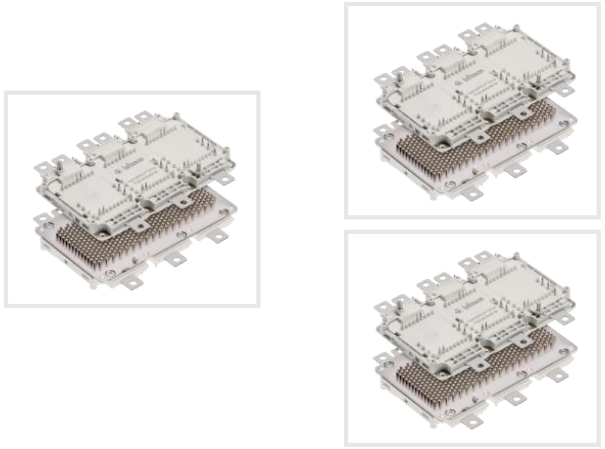
1 module 2 modules

≈ 30% reduction

Conduction Losses SiC MOSFET

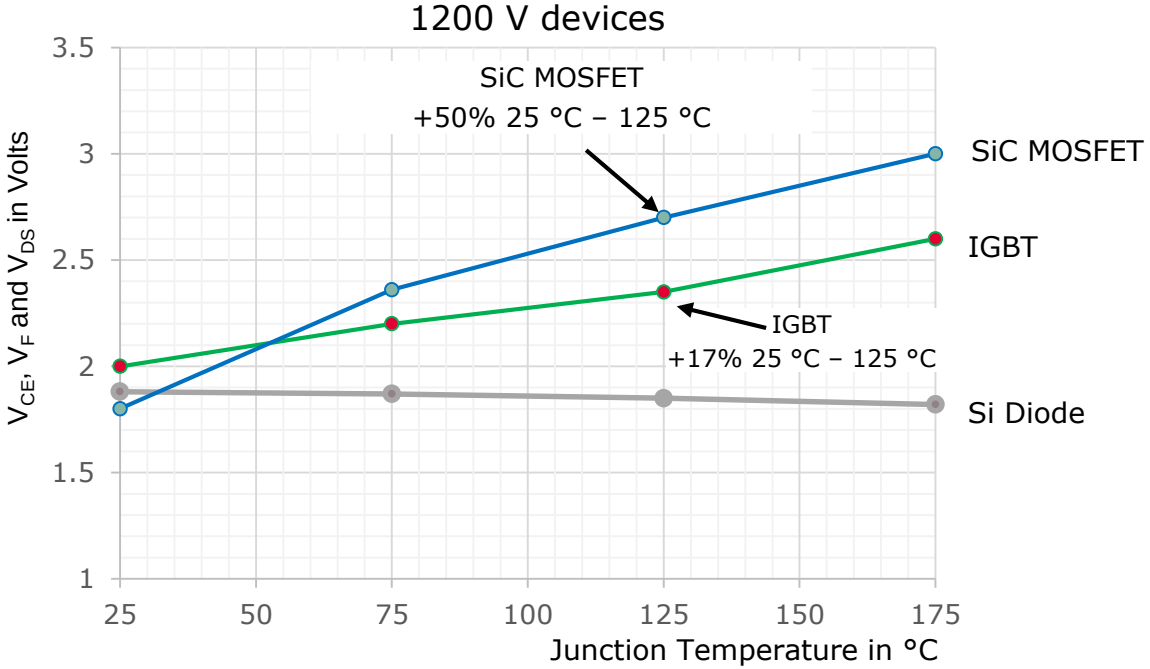
1 module 2 modules

≈ 60% reduction



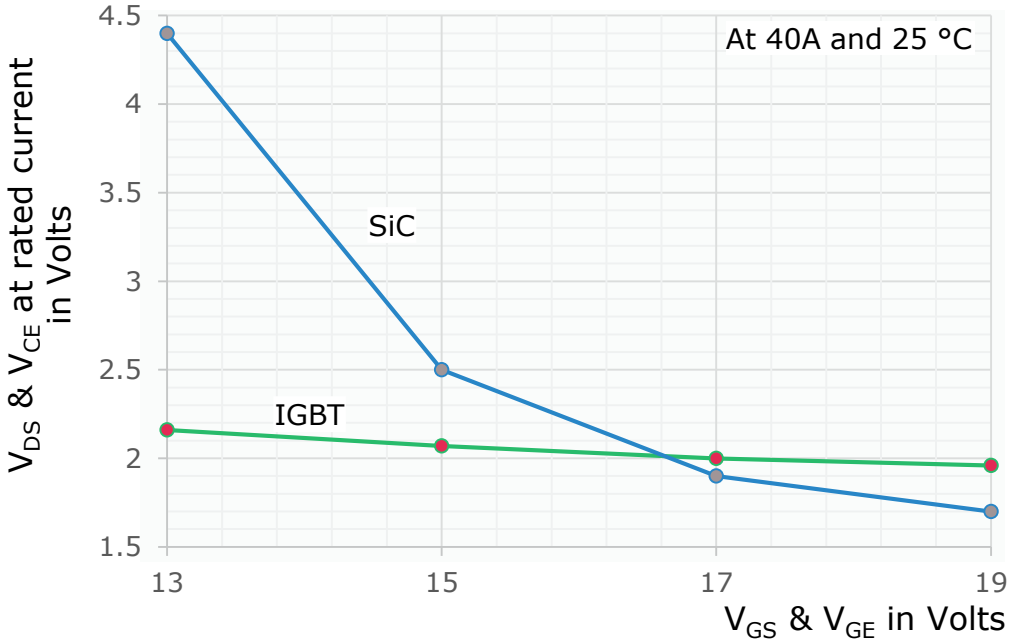
Note loss reduction >50% due to reduced T_j

V_{CE}, V_F and V_{DS} Dependency on Temperature



SiC - much larger dependency of conduction losses with temperature than IGBT and Si Diode

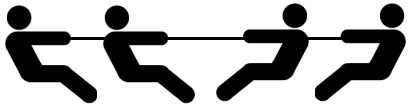
Variation of R_{DSON} / V_{CE} with V_{GS} / V_{GE}



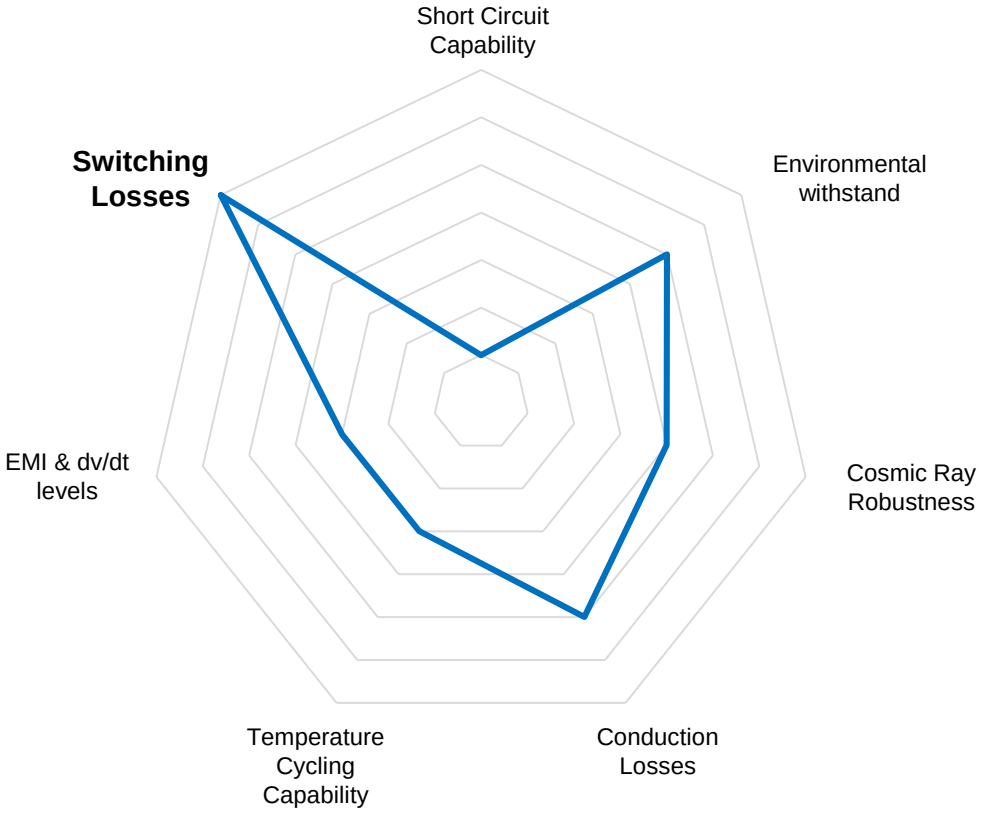
SiC - much larger dependency of conduction losses with gate voltage than IGBT and Si Diode

Gate oxide reliability

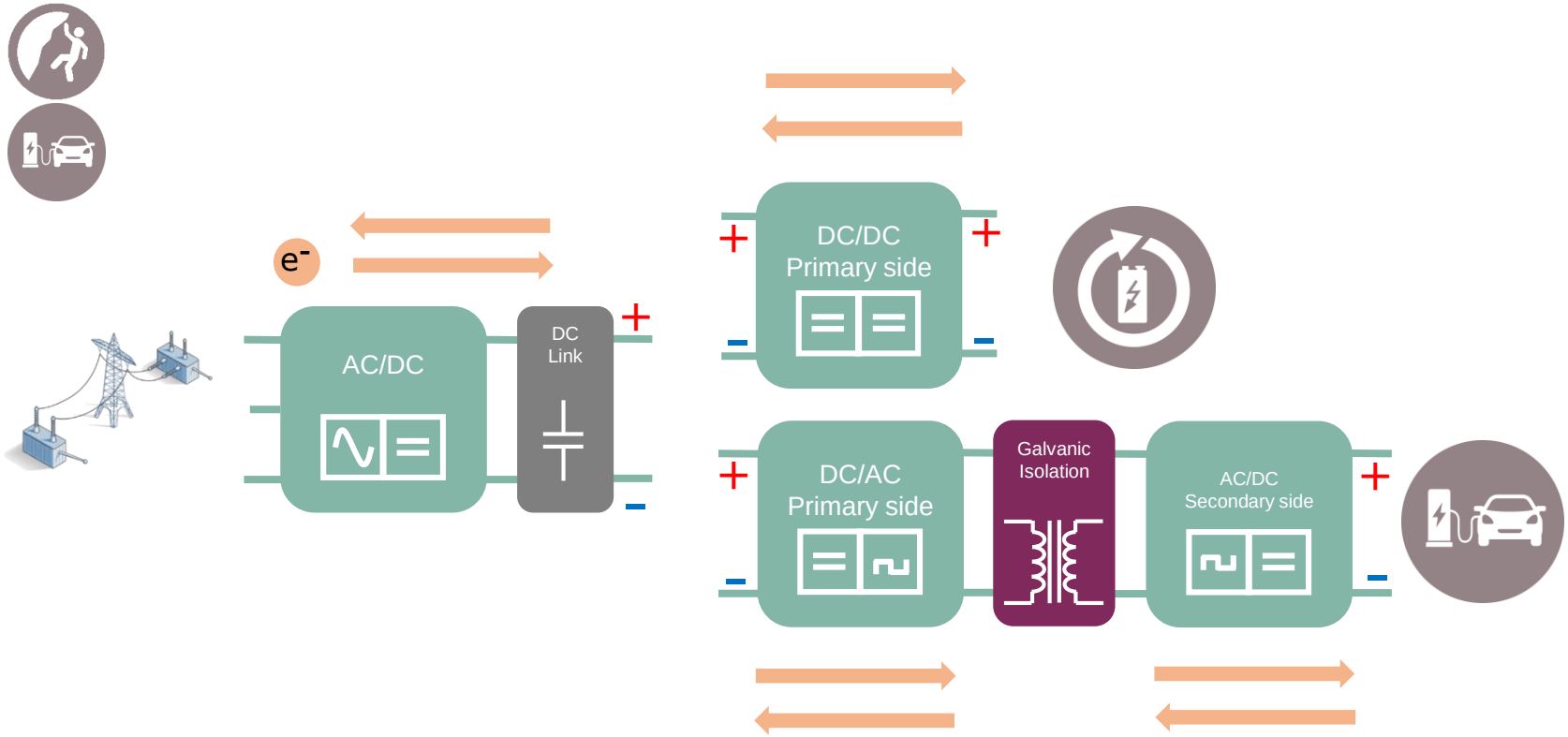
Lower R_{DSON}



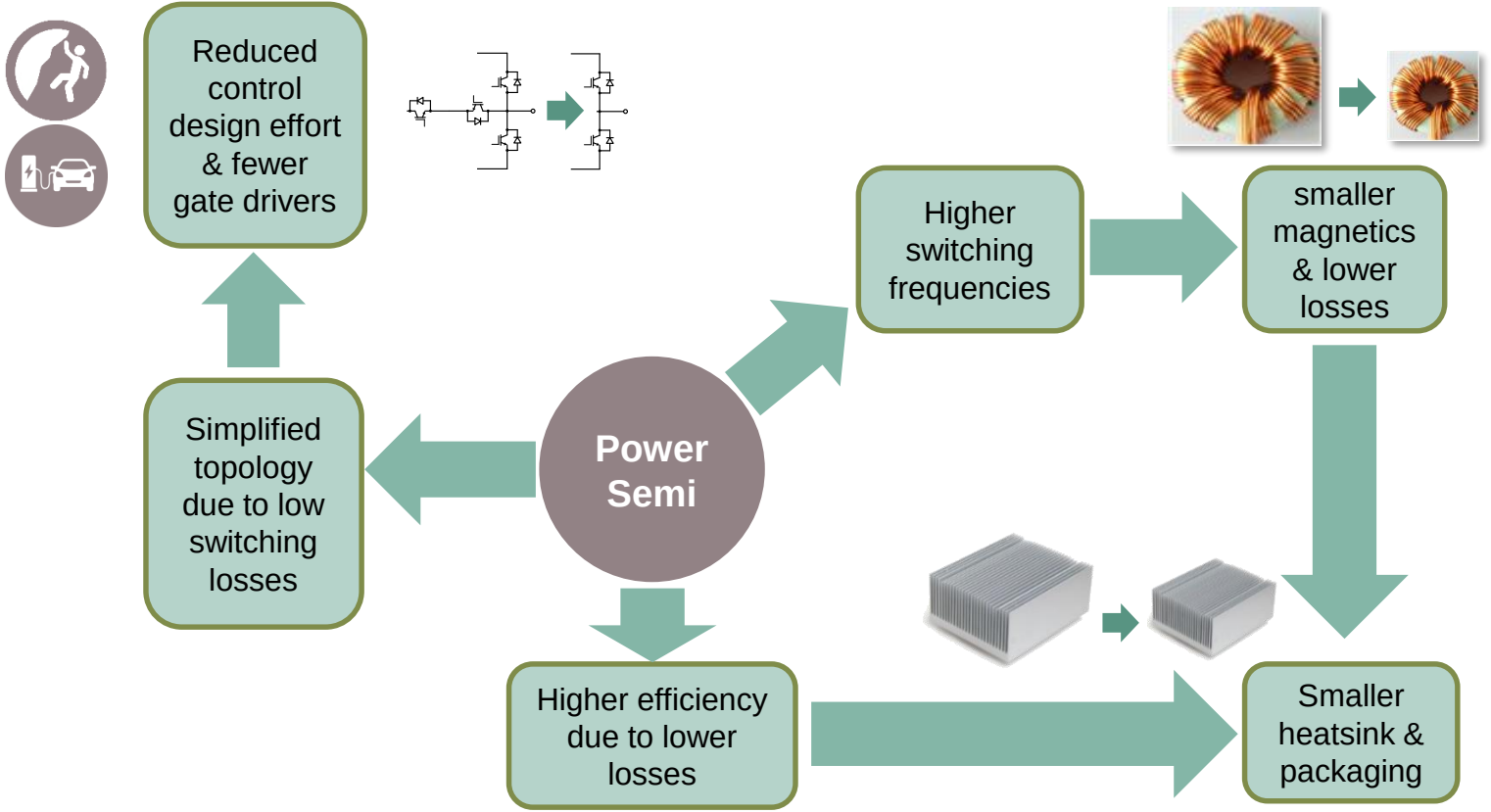
Energy Storage and Chargers – Spider Diagram



A Day at the Office for an Electron

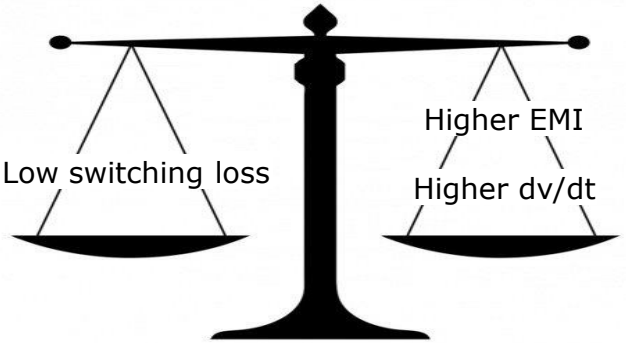


Benefits of Higher Switching Frequencies

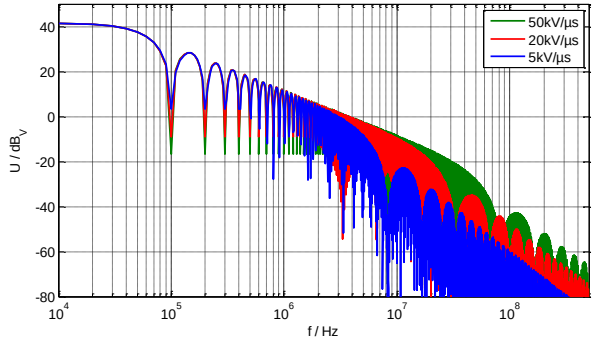


Chip Design Measures for low switching losses

Relax SiC MOSFETs have low switching losses

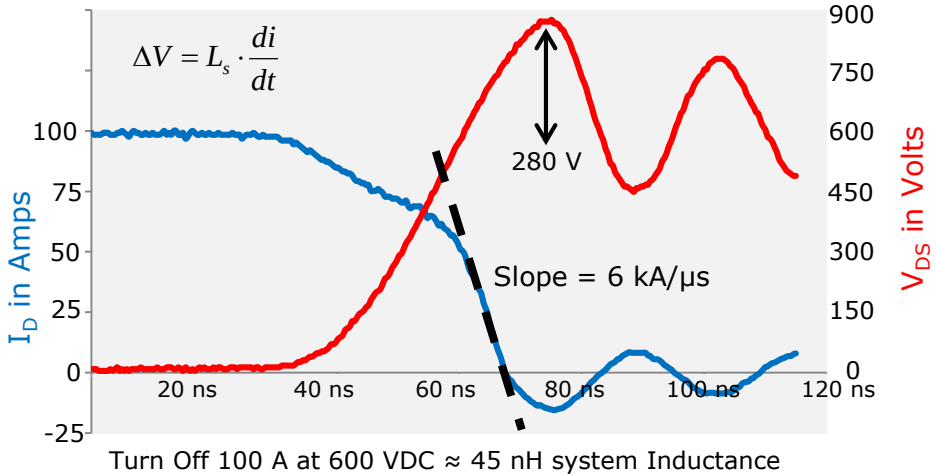


Challenges of Fast Switching



EMI – dv/dt and di/dt

Voltage Over-shoots and RBSOA

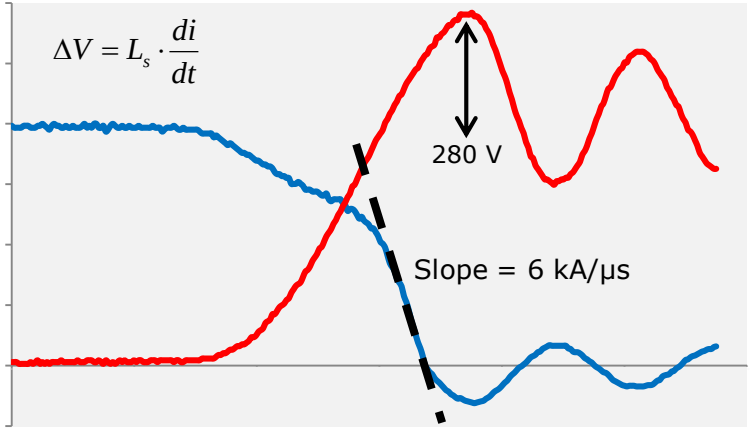


Turn Off 100 A at 600 VDC ≈ 45 nH system Inductance

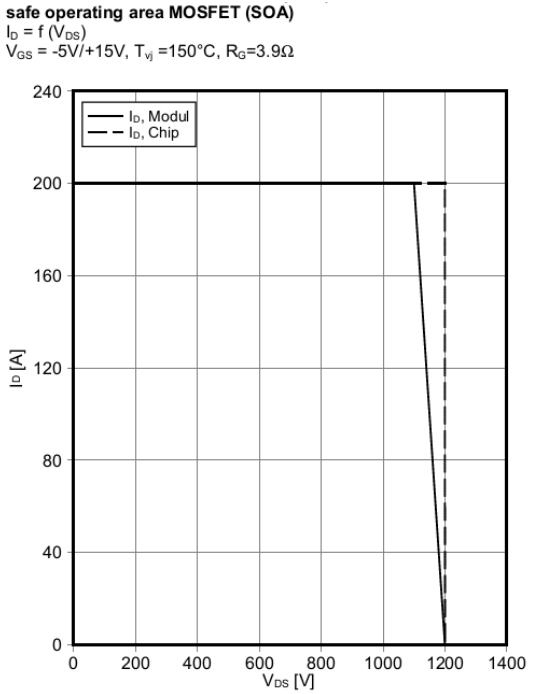
How to Reduce Voltage Overshoots and Oscillations at Turn Off

- Reduce the di/dt level
- Reduce the loop inductance

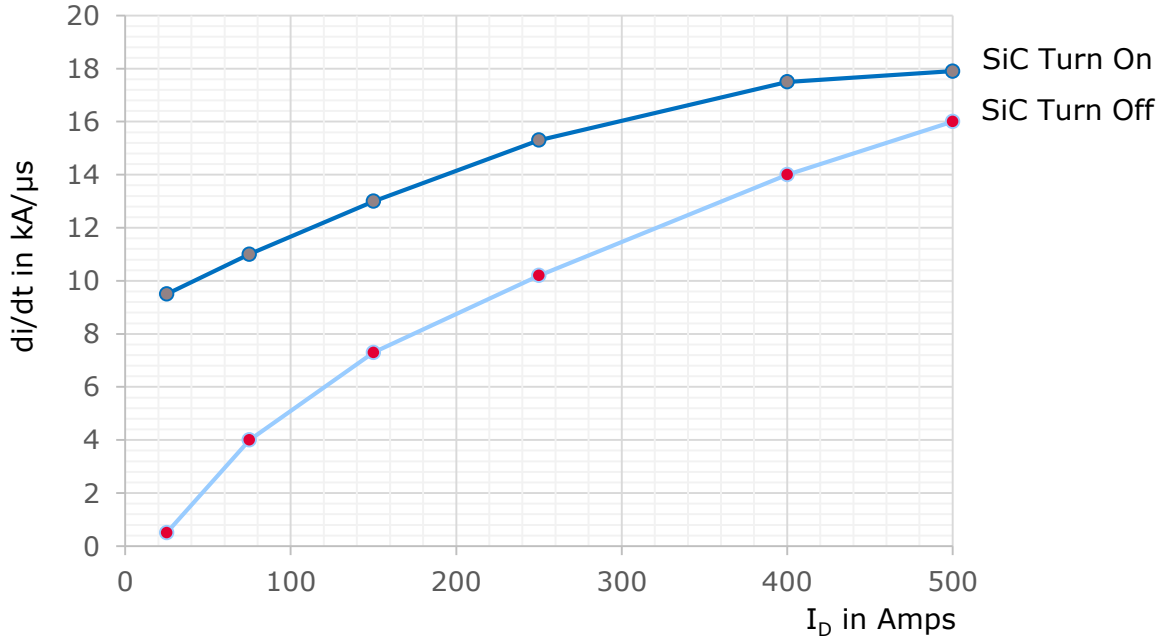
Voltage Over-shoots and SOA



Typical SOA curve for a 100A 1200V SiC MOSFET module

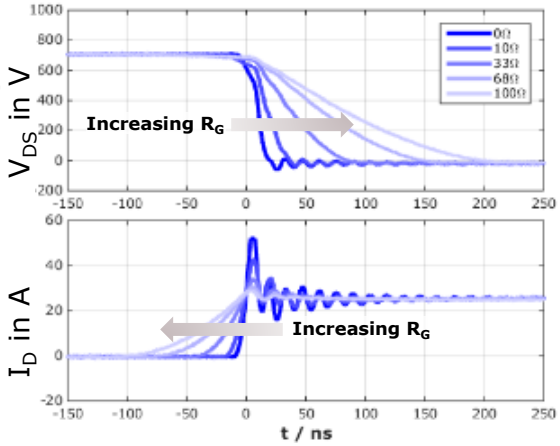


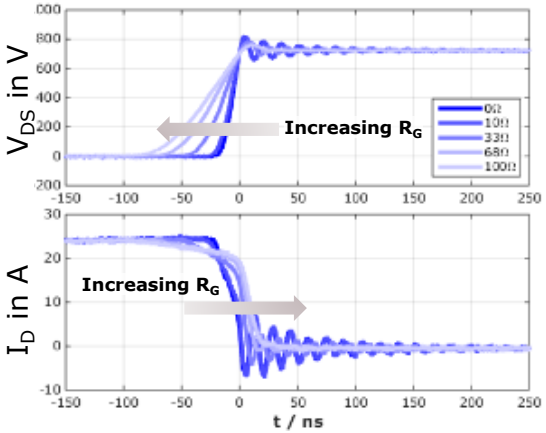
Typical di/dt levels for 200 A SiC MOSFET switching at 150 °C



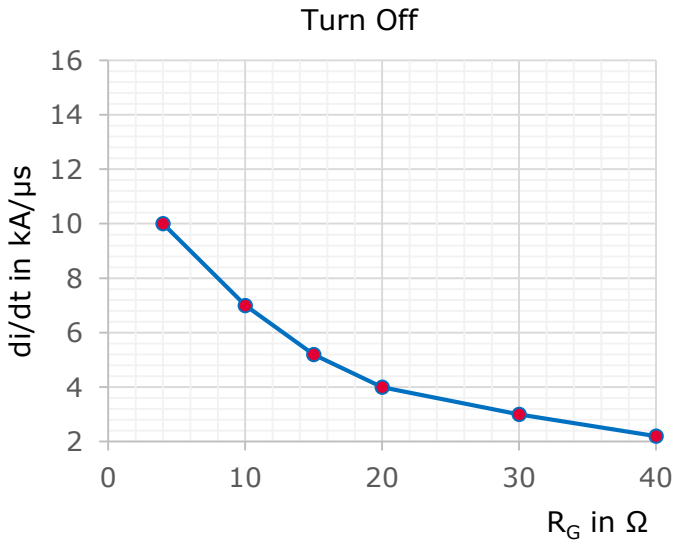
Turn off at 250A with L_S ≈ 30 nH and 10.2 kA/µs ≈ 306V overshoot

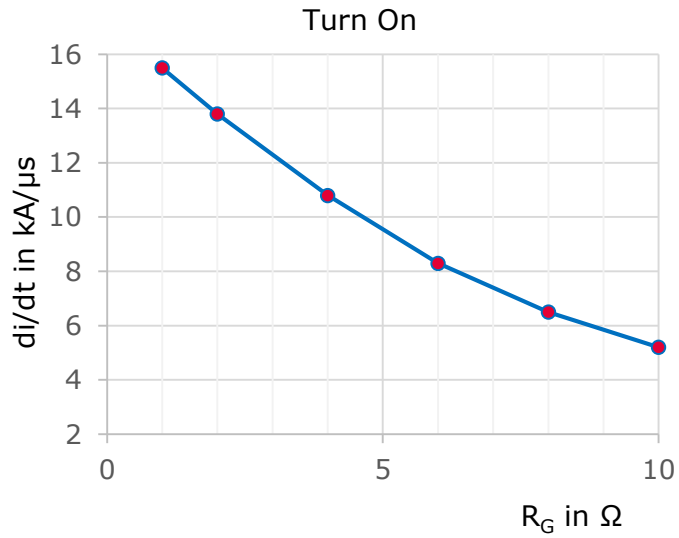
SiC MOSFET Controllability of Switching Speed Using R_G





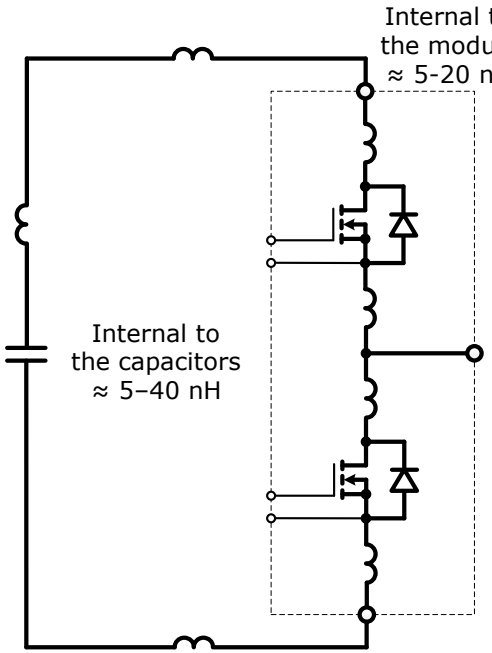
Typical di/dt levels for 200 A SiC MOSFET switching at 150 °C, 250 A with Changing R_G





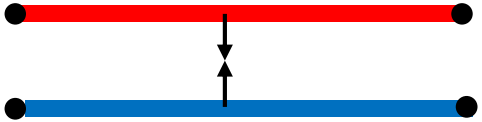
By increasing R_G from 3.9 Ω to 20 Ω the voltage overshoot is reduced from ≈ 306 V to 30 nH x 4 kA/µS ≈ 120 V overshoot

Where is the System Inductance and How to Reduce it?



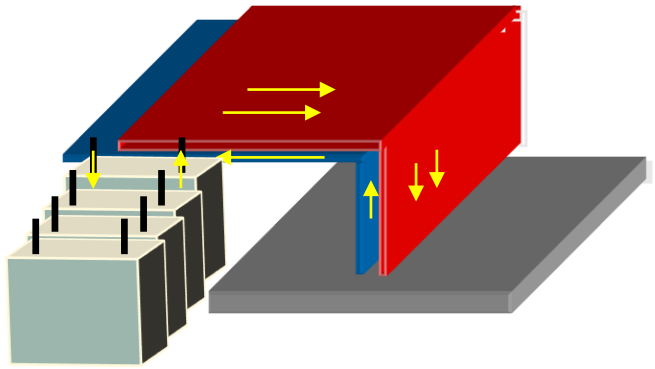
Overlapping go
and return paths

Wide flat planes with
multiple connection points



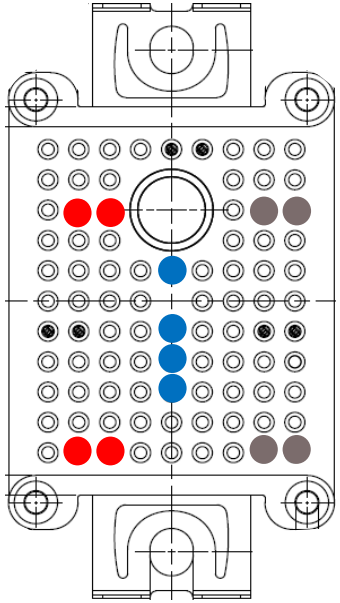
Keep loops as
small as possible

Low Inductance Module Design

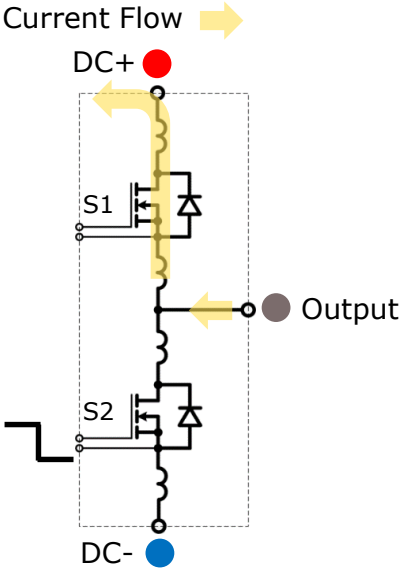


Parallel overlapping planes with multiple connections and small loops

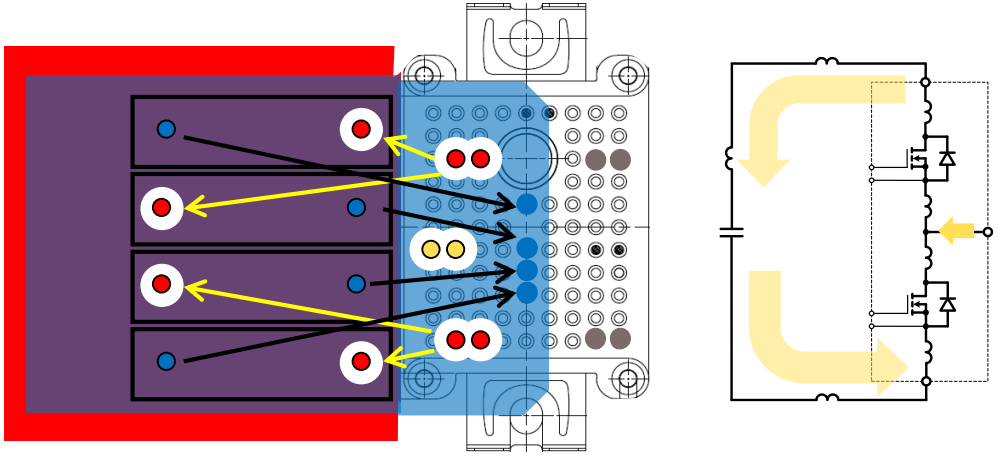
Package Top View



Schematic



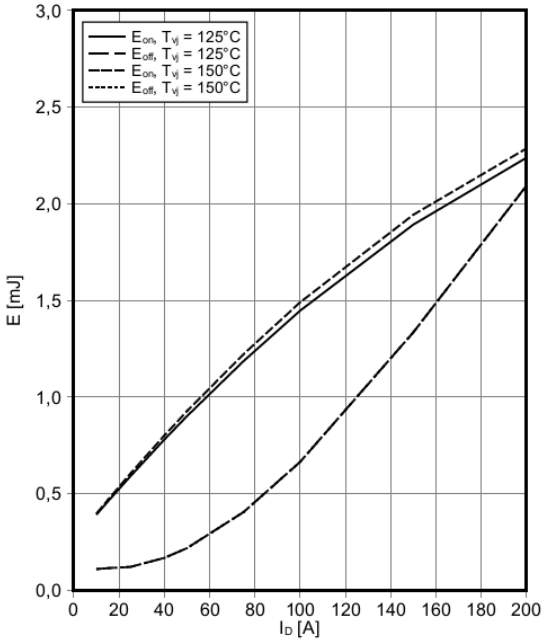
Current Flow in Both PCB DC Bus Layers



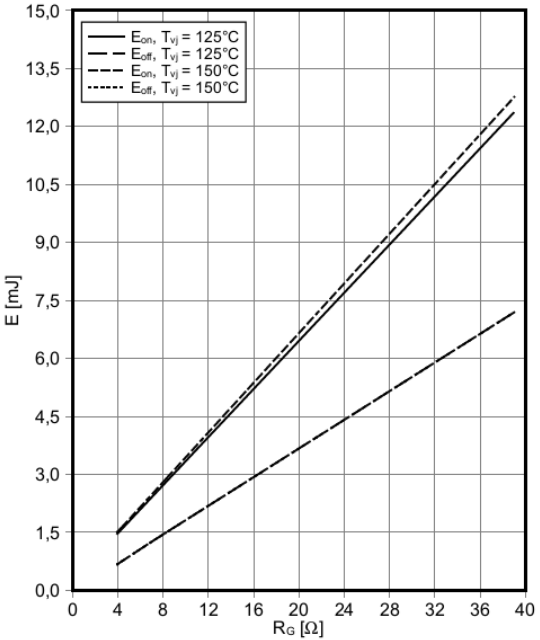
- Short current paths, small current loops, multiple paths in parallel
- If possible, current flowing in opposite planes

Data Sheet Switching Performance Curves

switching losses MOSFET (typical)
$E_{on} = f(I_D)$, $E_{off} = f(I_D)$
V_{GS} = +15 V / -5 V , R_{Gon} = 3,9 Ω, R_{Goff} = 3,9 Ω, V_{DS} = 600 V



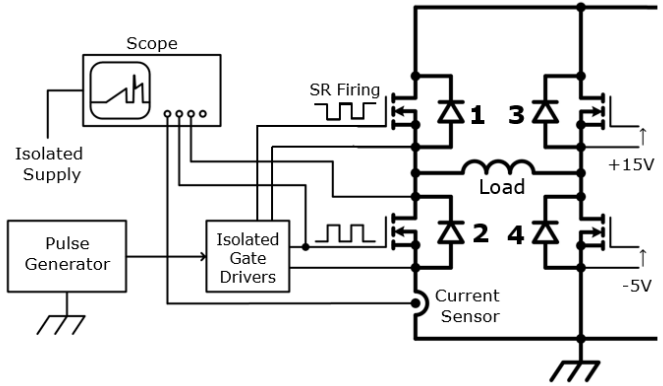
switching losses MOSFET (typical)
$E_{on} = f(R_G)$, $E_{off} = f(R_G)$
V_{GS} = +15 V / -5 V, I_D = 100 A, V_{DS} = 600 V



Typical Curves for 100A 1200V SiC MOSFET Module

How to Confirm Switching Loss Performance

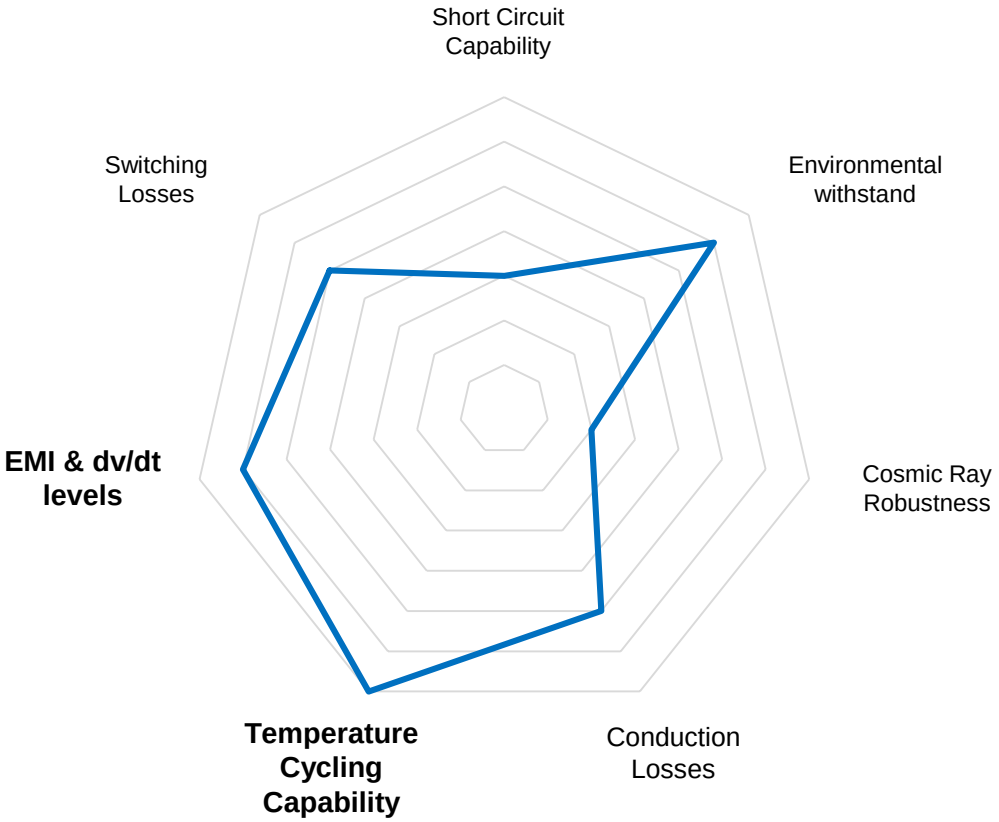
- Switching losses in the final application will be different from data sheet due to different operating conditions and gate driver.
- Strongly recommended to run **D**ouble **P**ulse **T**est DPT in final application system.
- Review di/dt and dv/dt levels and leave margin for higher Rg values if required.



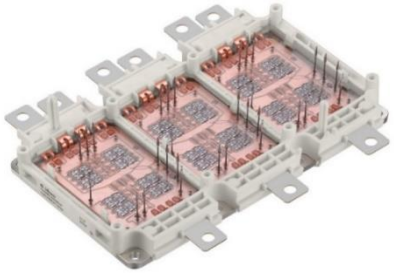
Summary

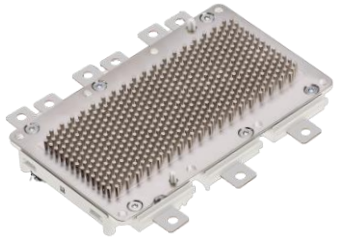
- With magnetics increasing switching frequency can reduce size, cost and weight.
- Chip design compromises especially with increased on state losses are required.
- Increasing gate resistor values can reduce EMI and di/dt levels but at a cost of higher switching losses
- Application factors such as low inductance layout and low EMI design need to be considered.

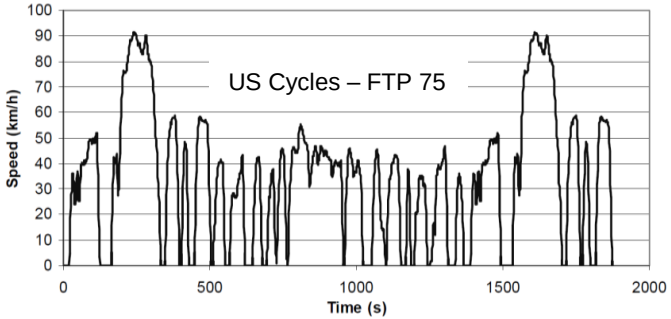
Automotive –Spider Diagram



Challenge Cyclical Load – High Temperature Cycling







What are the Wear Out Mechanisms due to Temperature Cycling? Bond Wire Fatigue.

Bond wire fatigue caused by

a) Thermally induced movement of the bond wire

b) Fatigue of welding area due to by thermal mismatch Al vs. Si

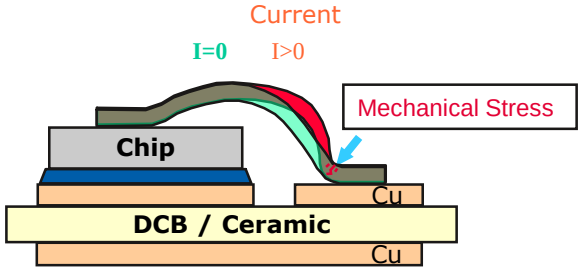
Heating of the wire

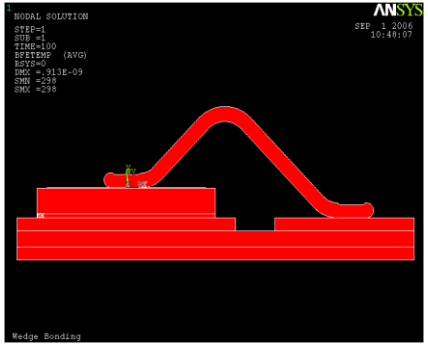
↓

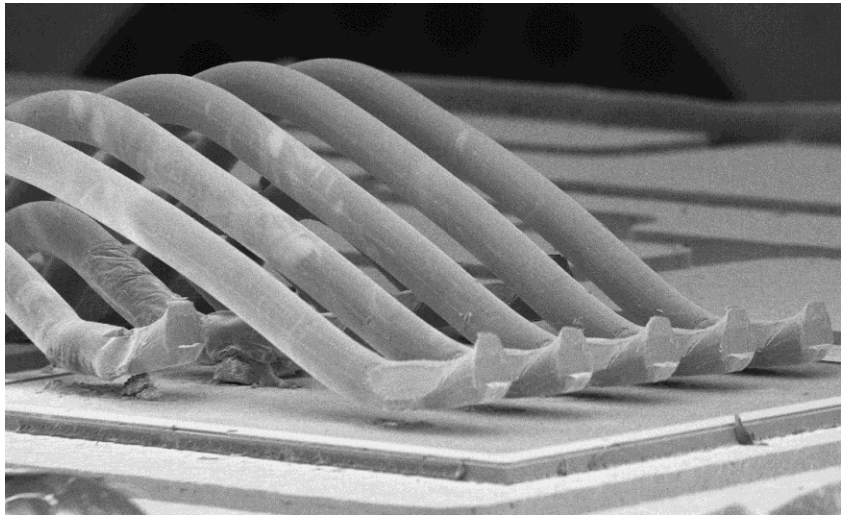
Thermal expansion

↓

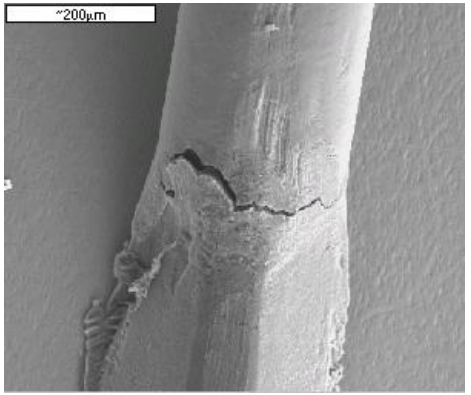
Mechanical Stress







Bond Wire Lift Off

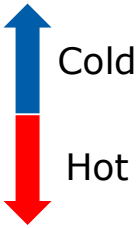


Bond Wire Heel Crack

Chip Solder and SiC Chip
Stress Caused by Temperature Cycling

At 225°C solder is molten
No stress in system

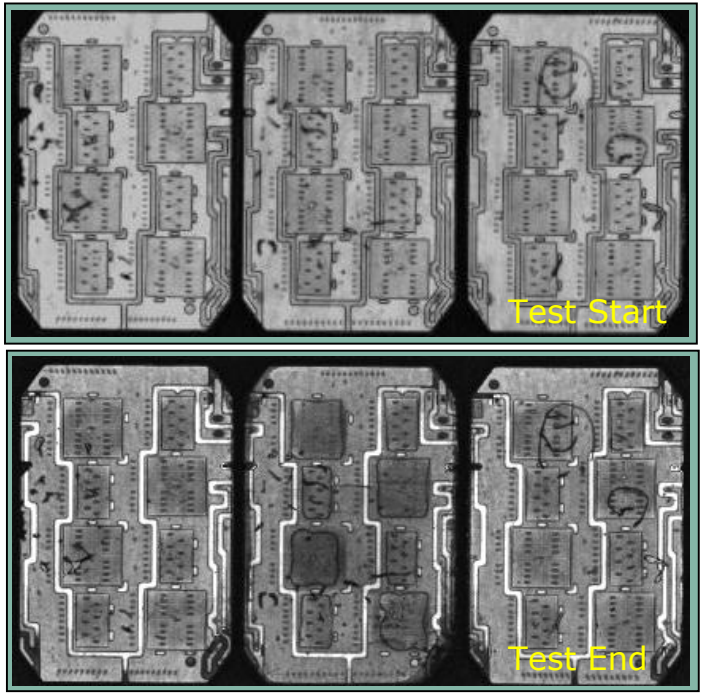
At 100°C solder is solid
stress changes with temperature



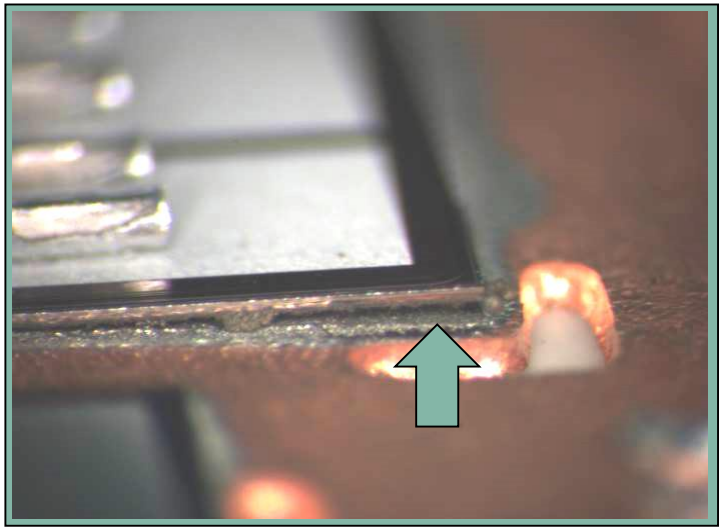
Stress due to several different factors:
CTE values, chip size, materials
and SIC stiffness

	CTE	Young's Modulus
Si	≈ 2.6 x 10^{-6} / °C	≈ 62 GPa
SiC	≈ 4 x 10^{-6} / °C	**≈ 450 GPa**
Solder	≈ 23 x 10^{-6} / °C	≈ 40 GPa
Copper	≈ 17 x 10^{-6} / °C	≈ 117 GPa

Chip Solder Delamination

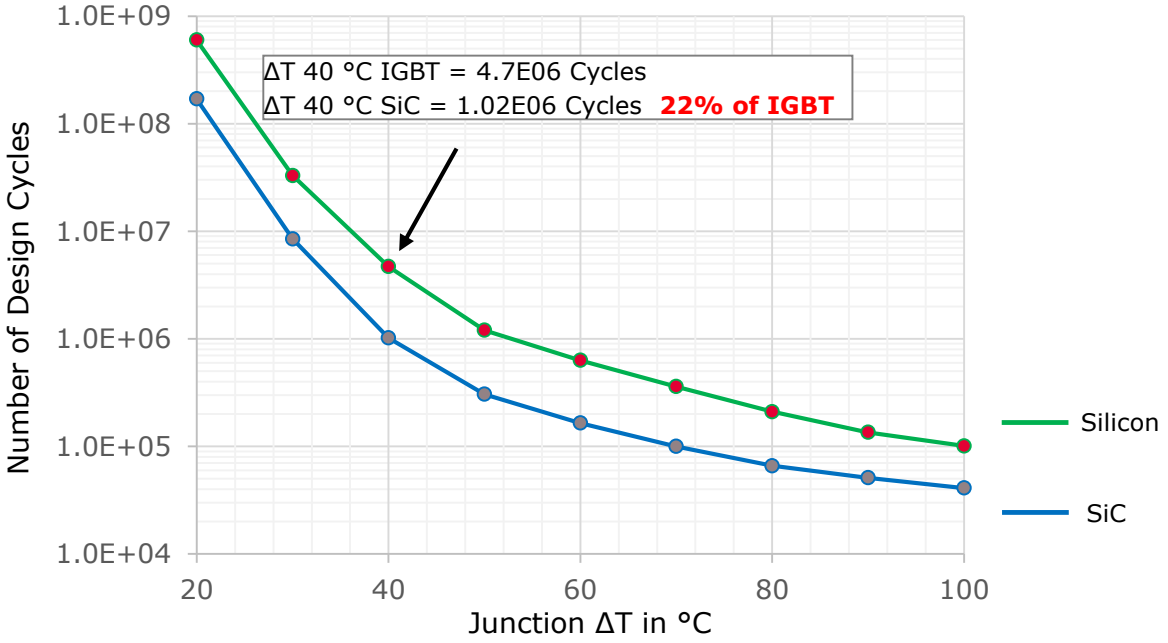


Ultra Sonic scans of the chip soldering layer



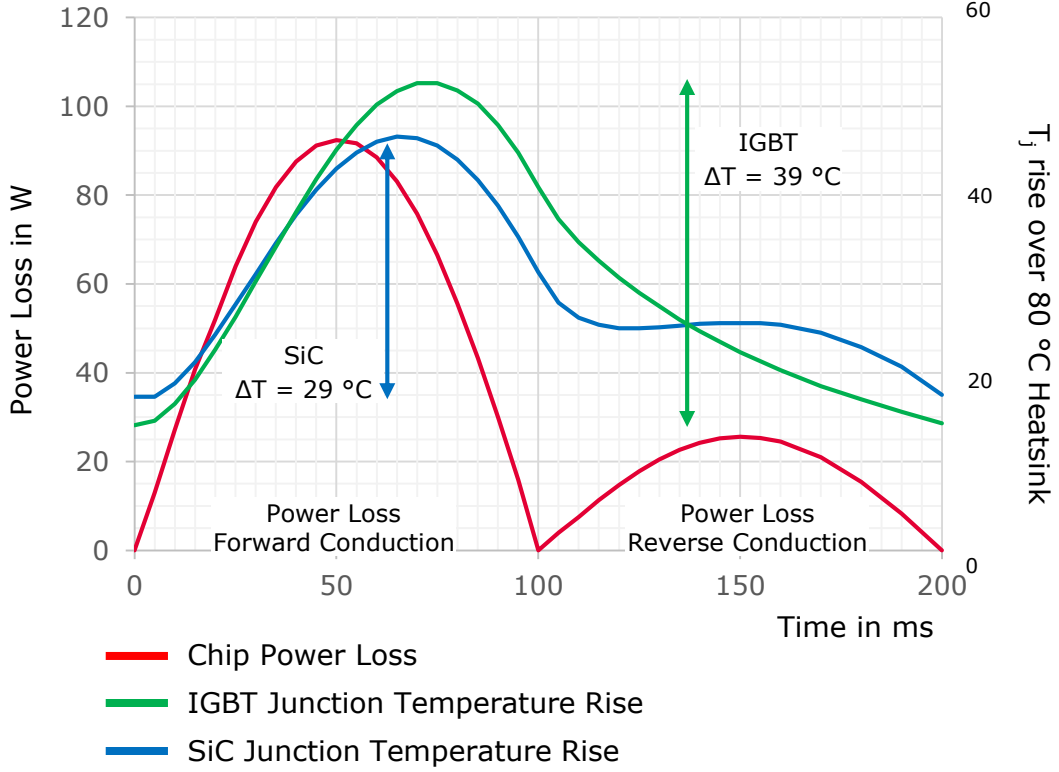
Optical image of delaminated chip solder

Typical Power Cycling Capability Curves SiC & Si IGBT at a Maximum Junction Temperature of 100 °C

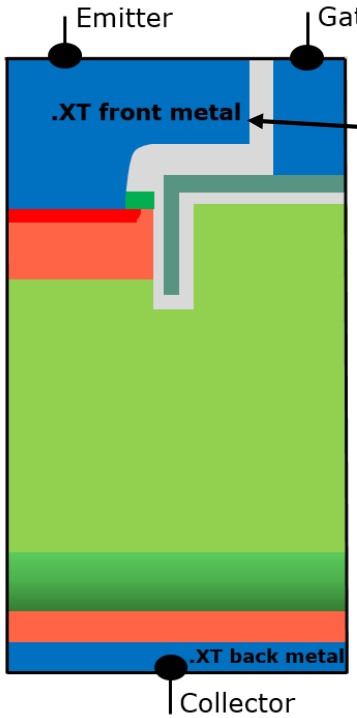


Note: Design cycles = Cycles at which 5% of samples show a 5% increase in forward voltage drop

Ripple Temperature at 5 Hz Operation IGBT & SiC MOSFET



Tools to Increase Lifetime

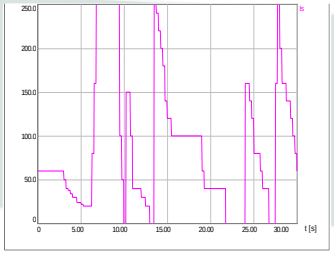


- Reduce Losses
- Improve Cooling
- Improve top side joining technology for Example top side copper and bond wires

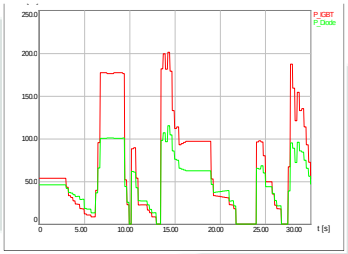
Improve solder connection e.g. diffusion soldering or sintering

How is Lifetime Estimated? 7 Steps A-F

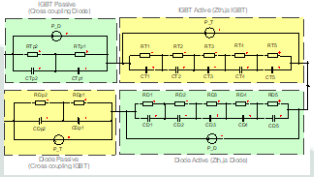
A. Design Targets

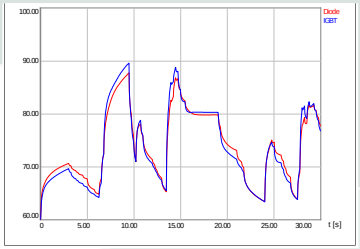


B. Mission Profile

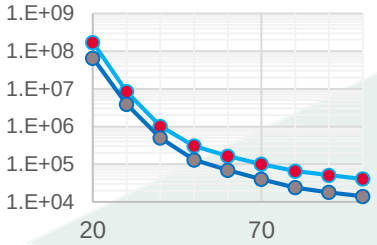


C. Power Losses

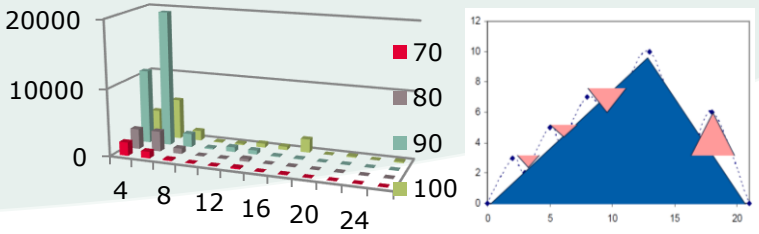




D. T_J Thermal Model

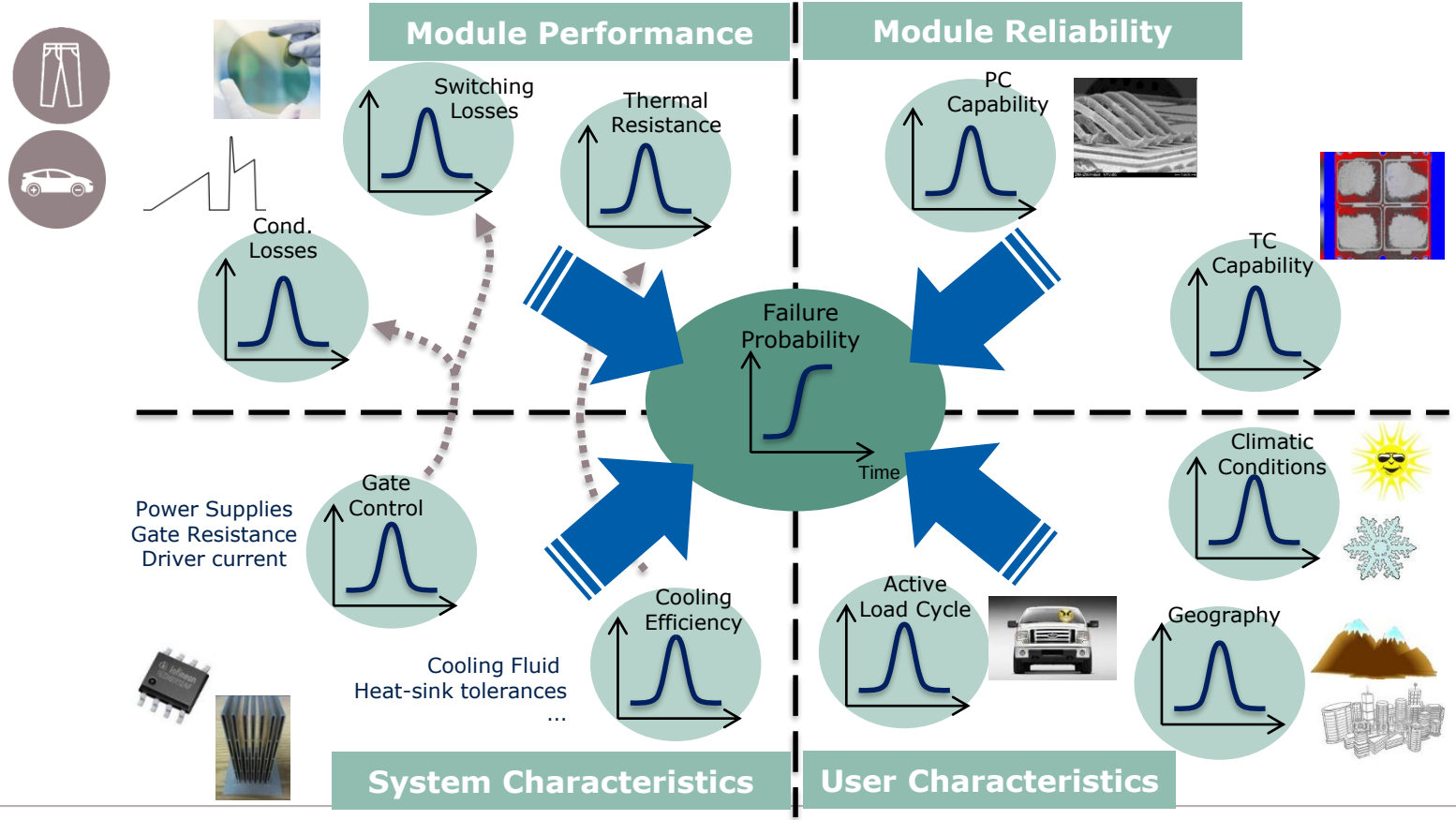


F. Design Life



E. Rain-Flow & Quantization

Statistical Parameters & Life Time Evaluation

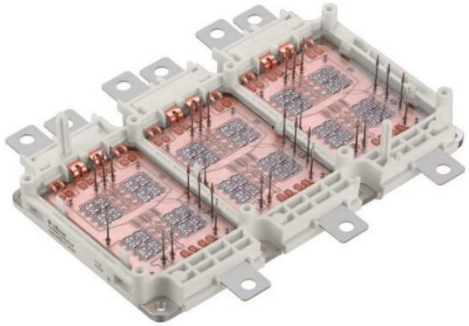


Challenges: EMI / dv/dt

Radiated

EM Susceptibility

Conducted

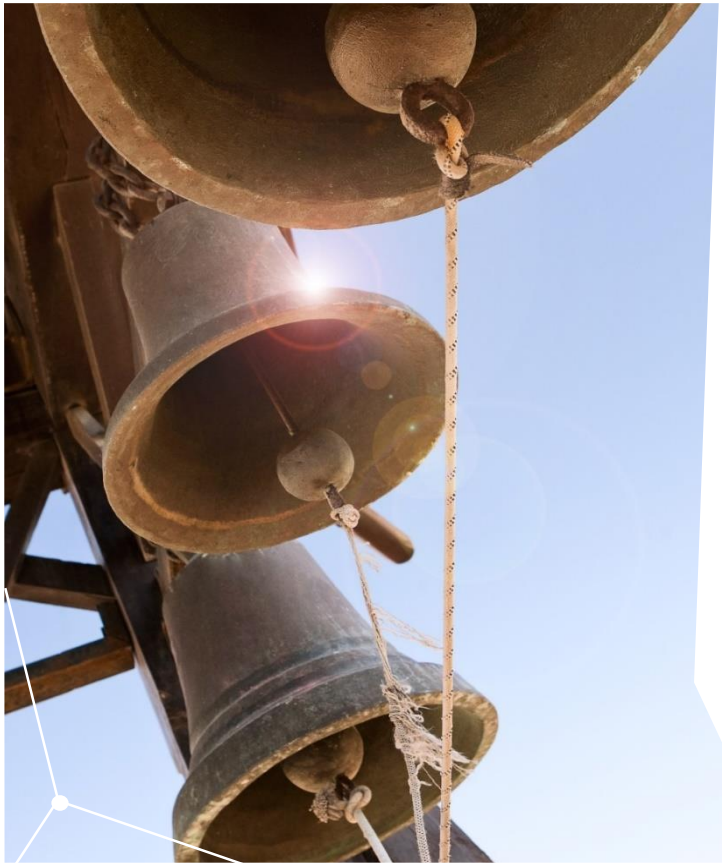


Radiated

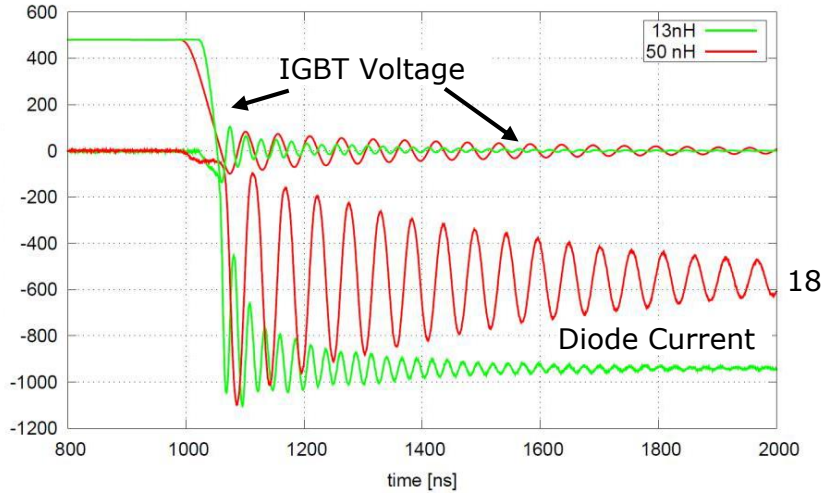
EM Interference

Conducted

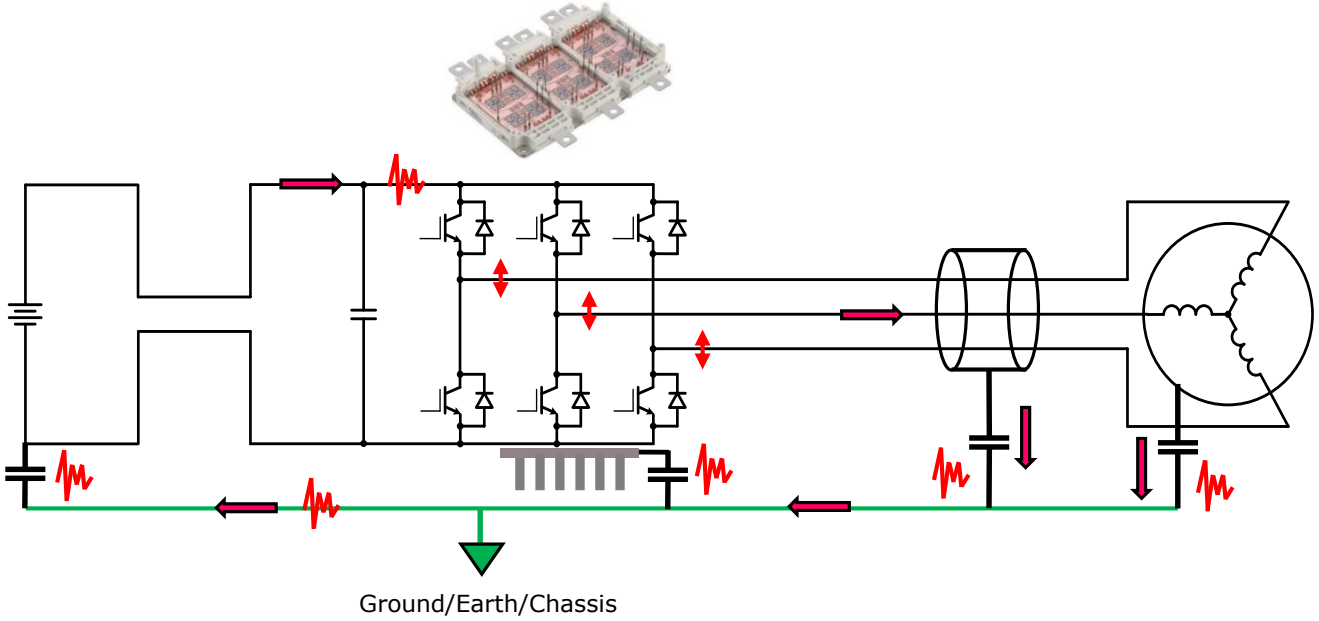
High di/dt and Loop Inductance = Oscillations



Lower inductance = reduced oscillations and EMI

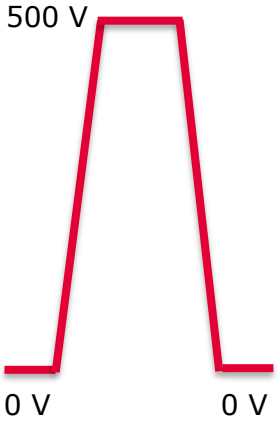


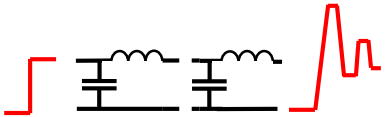
Typical Paths for Parasitic Current Flow and Conducted EMI

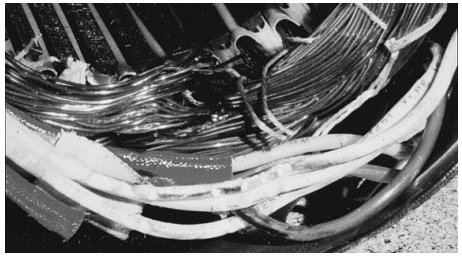


I = C x dv/dt

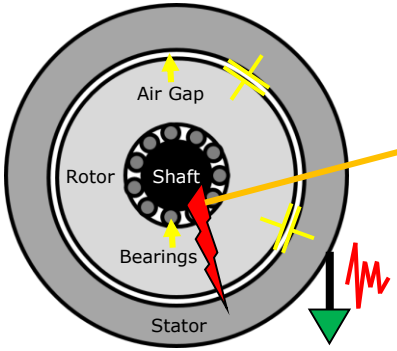
Fast Switching Edges at High dv/dt are Problematic

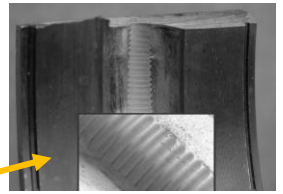






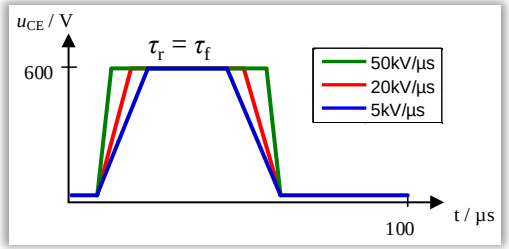
Stress on motor insulation system



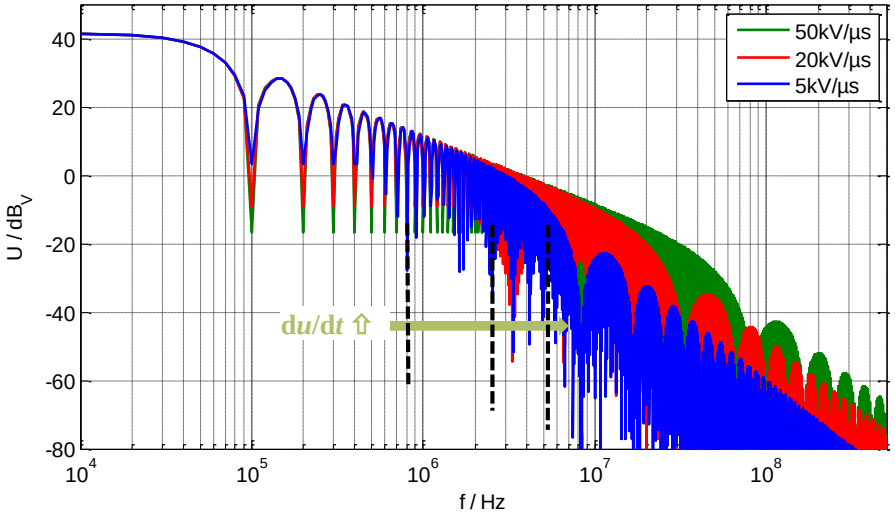


Bearing damage

Ideal Fast Fourier Transformation (FFT) of Trapezoidal Waveform with varying dv/dt slopes.

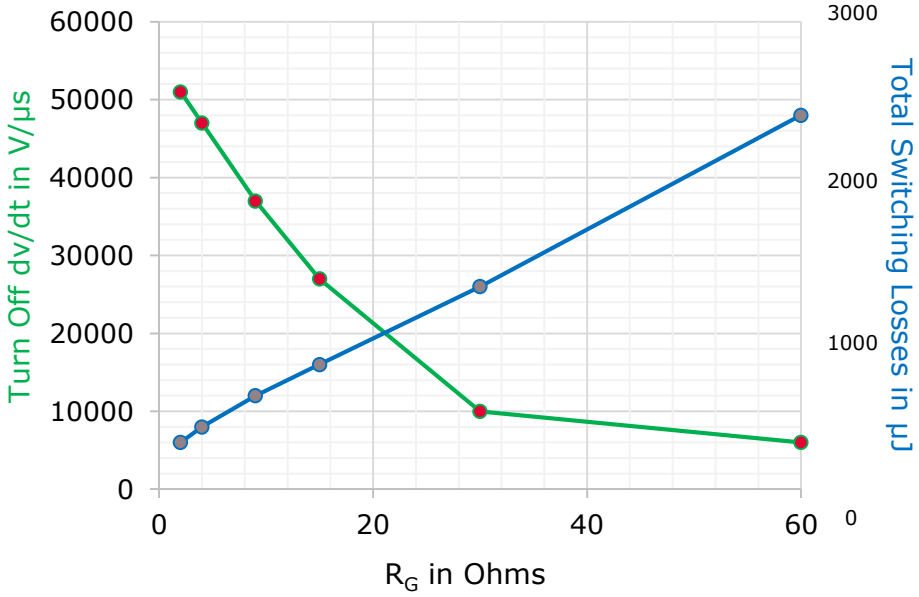


du/dt	5 kV/µs	20 kV/µs	50 kV/µs
τ_r	120 ns	30 ns	12 ns

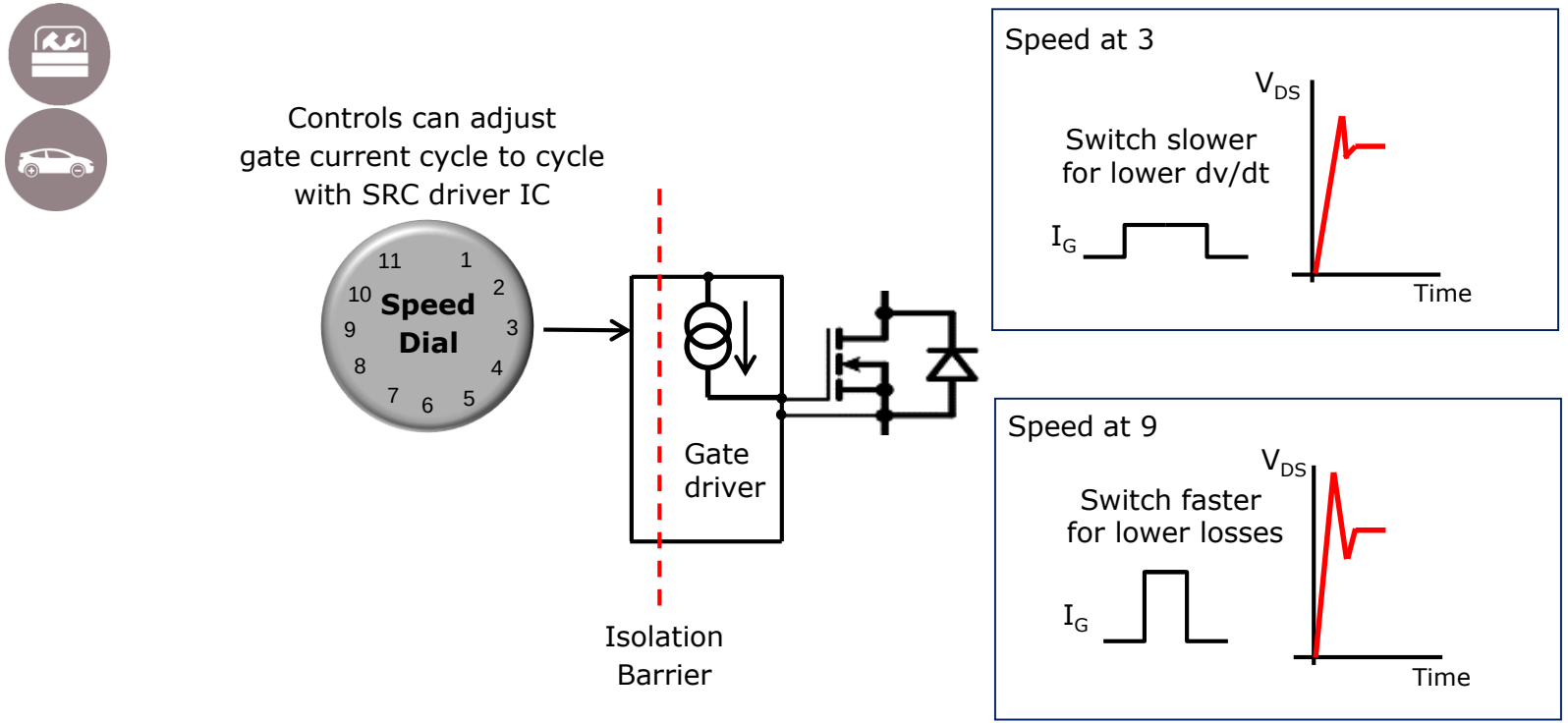


d*v*/d*t* has more effect at the higher frequency region of the spectrum.
Here @10MHz: the difference between d*v*/d*t* = 5 & 20 kV/µs is 15 dB(V)

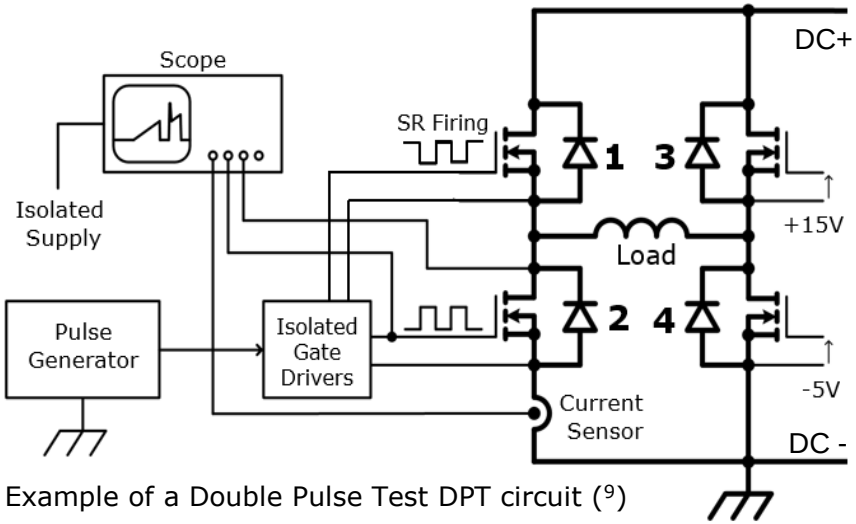
Typical dv/dt levels and Switching Losses vs. R_G for a SiC MOSFET



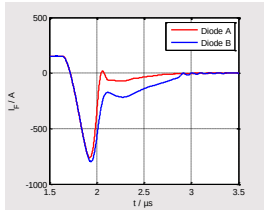
Slew **R**ate **C**ontrol SRC: Adjustable Switching Speed Cycle to Cycle Using Current Source.

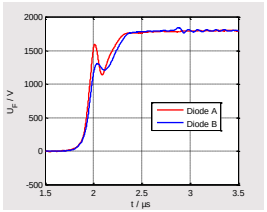


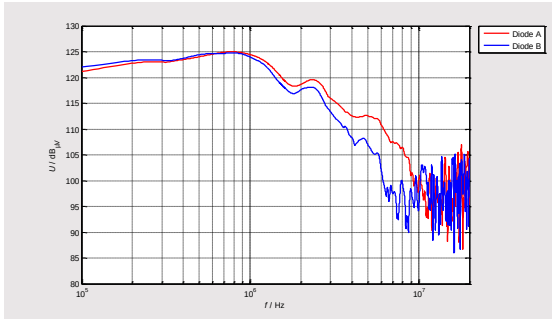
Double Pulse Test Waveforms can be Used to Simulate Plots



Example of a Double Pulse Test DPT circuit ([9])







Summary

- A very complex design challenge, difficult to simulate and measure.
- Keep power switching loops small and minimize inductance.
- Understand capacitance paths to ground and steer/route parasitic currents to selected paths.
- Check switching waveforms using DPT over the full range of currents, voltages and temperatures.
- Switching speeds can be reduced by Rg and Cge/Cgs or new gate driver technology but all will increase switching losses.

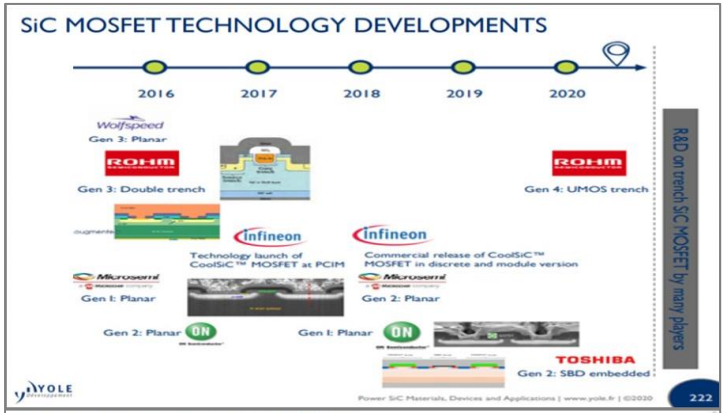
The SiC MOSFET Situation Today

- Different SiC MOSFET concepts exist:

Cell:
- Planar cell MOSFETs and Trench cell MOSFETs.

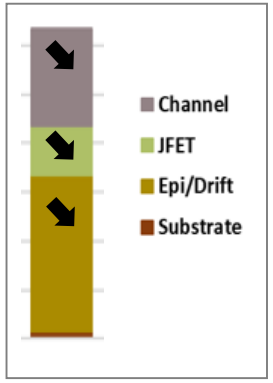
Different Freewheeling **Diode** concepts:
- Freewheeling diode function externally as a SiC schottky diode or as integrated SiC schottky or as p-body diode.

Vertical concept:
- So far conventional uniform drift zone doping.



What else to Come? Strong R_{DSON}* Area Reduction Forseeable

- **Cell** concept:
  - Trend to trench.
  - Most likely advanced trench concepts will follow later step by step (similar to low voltage Si Power MOSFETs).



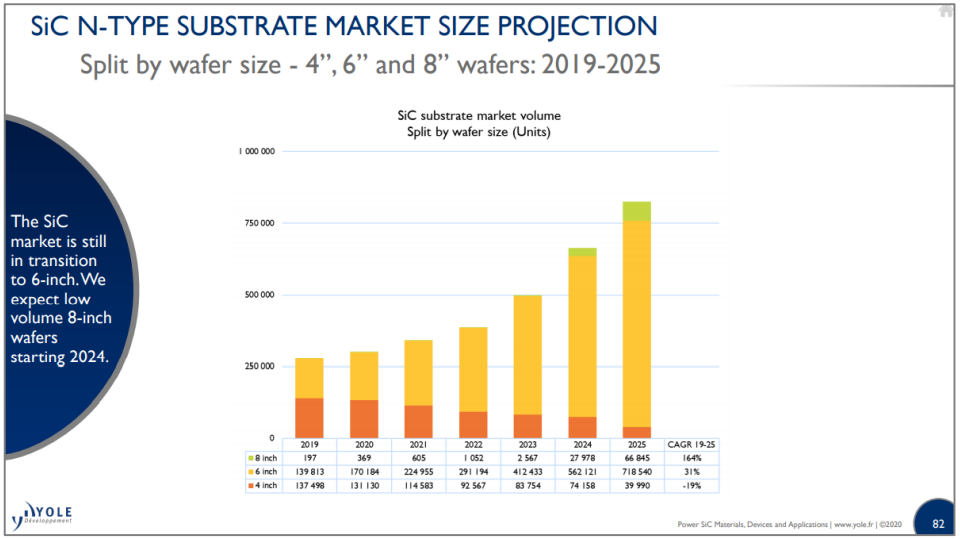
- **Vertical** concept:
  - SuperJunction very attractive from performance perspective, but pro's and con's need to be assessed.

- Higher **junction temperatures** (similar as for Si IGBTs, but even more…), also in this case pro's and con's need to be assessed. Note strong R_{DSON} increase with temperature.

- Advanced **assembly and interconnect** technologies (at least as important as for Si IGBTs).

What else to Come? Strong SiC Production Capacity Increase Foreseeable

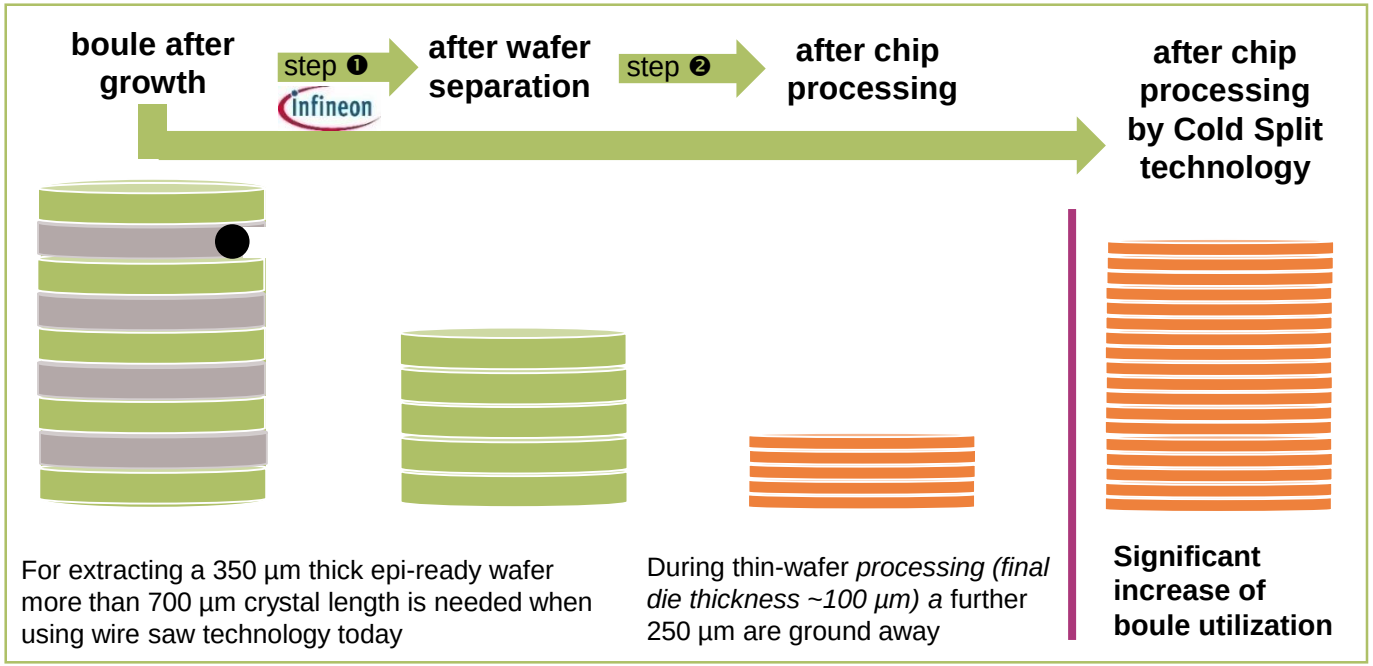
Larger SiC **Wafer Diameter** 150 mm => 200 mm: **more chips out of one wafer**



To overcome the SiC Material Irony –
… Boule and wafer **splitting** to **make more SiC wafers out of a single SiC boule**

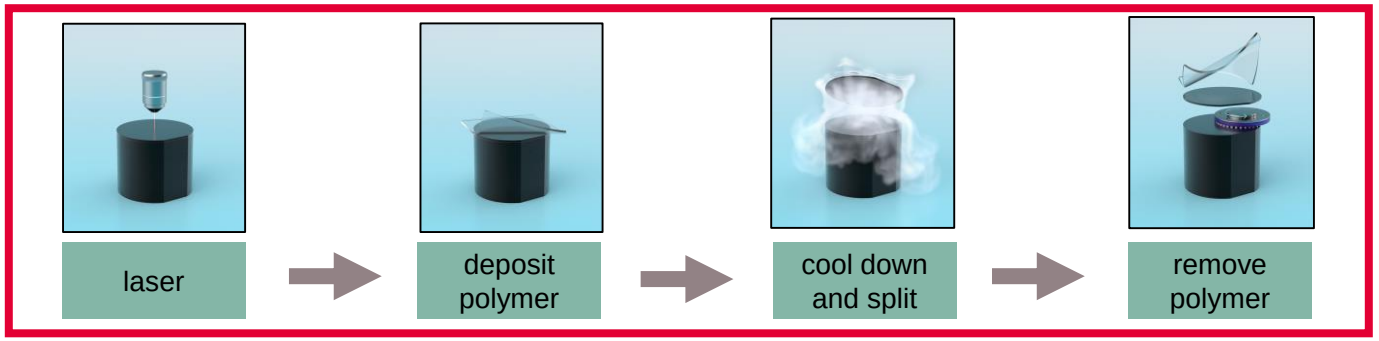
Strong SiC Production Capacity Increase Foreseeable - the SiC material irony

- The SiC boule growth process is expensive and time-consuming
- Today, ¾ of the grown material is turned into dust during processing



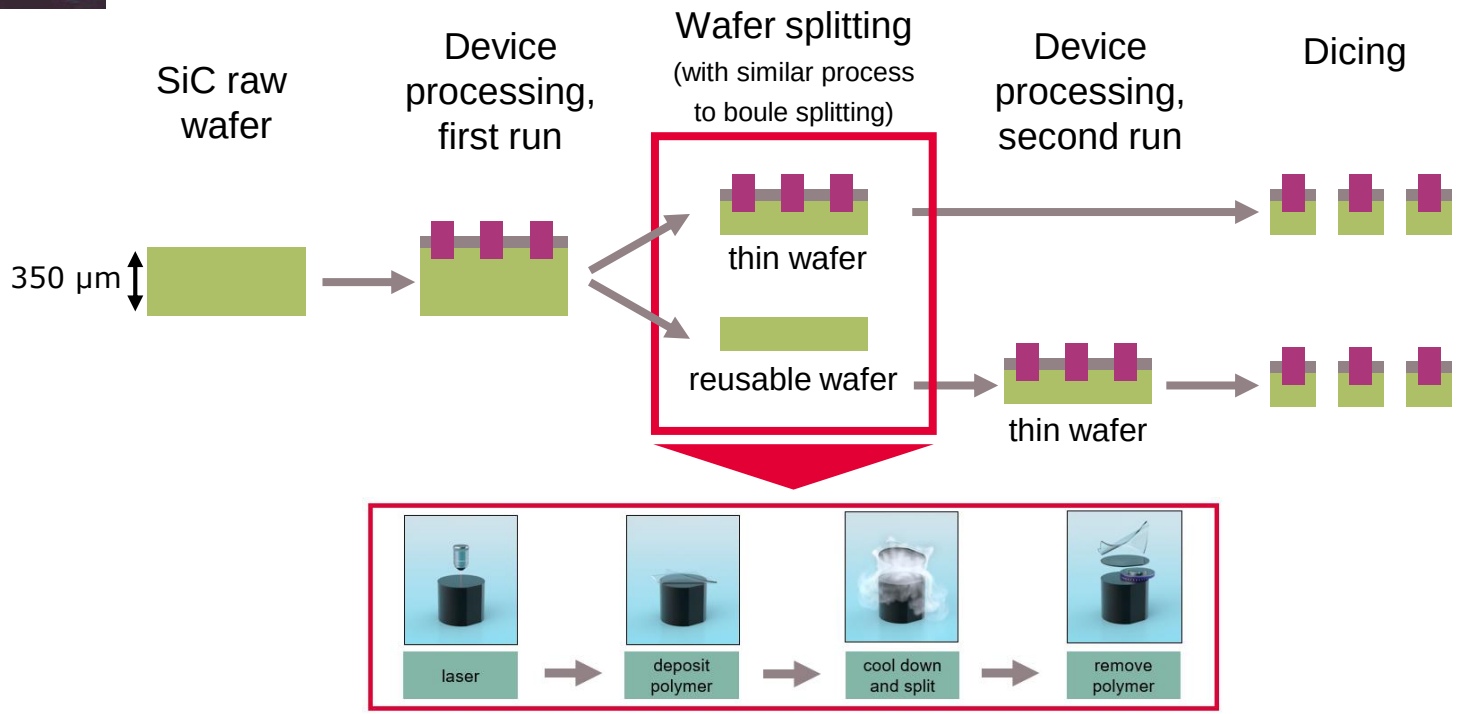
Strong SiC Production Capacity Increase Foreseeable - Cold Split Technology

Cold Split technology at a first glance: **Boule Splitting**



Strong SiC Production Capacity Increase Foreseeable - Cold Split Technology

Cold Split technology “on top“: Wafer Splitting / “**Twinning**“



Summary

- Cell concept: Trend to trench, most likely advanced trench concepts will follow a step at a time.
- Vertical concept: SuperJunction very attractive from performance perspective, however pro's and con's to be assessed.
- Higher junction temperatures may come, if advantageous.
- Advanced assembly and interconnect technologies (at least as important as for Si IGBTs).
- Larger SiC Wafer Diameter 150mm => 200mm: more chips out of one wafer.
- Boule and Wafer Splitting to make more SiC wafers out of a single SiC boule.
- *A bright future ahead … for SiC / WBG for sure, but also Si IGBTs with cost and performance improvements they will remain very important.*

Q&A

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SiC MOSFET application notes on Infineon website at: https://www.infineon.com/cms/en/product/power/wide-band-gap-semiconductors-sic-gan/silicon-carbide-sic/coolsic-mosfet/#!documents Then page down for application notes
Application notes and data can also be obtained from your local sales representative.

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