GaN power devices and applications reliability

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Outline

- Device structure
- Failure mechanisms
- The gaps for power management usage in traditional silicon qualification
- Addressing the gaps and assuring application reliability with JEP180
  - Broad coverage: switching locus
  - Validating switching lifetime
  - Validating application-use reliability (DHTOL)
- Reliability for unusual and extreme conditions
  - Short circuit withstand
  - Surge robustness without avalanche
Benefits of GaN

GaN enables high-frequency power converters for a wide range of power levels, where power density, efficiency and solution size matters!

GaN’s low Rsp with zero reverse recovery allows a low-capacitance die that can switch more efficiently and shrink power-supply size.
Every device has failure mechanisms that need to be understood and engineered. High electric fields cause Time Dependent Breakdown (TDB). High fields and hot carriers cause charge trapping. Switching causes stress from reverse recovery, high slew rates, and hot-carrier wearout. A known GaN failure mode is the increase in $R_{ds-on}$ on the timescales of switching. This dynamic $R_{ds-on}$ increase is due to charge trapping. Reliability engineering consists of making FETs reliable to stresses seen in application.
Steps to achieving reliable GaN

<table>
<thead>
<tr>
<th>Component level</th>
<th>Power supply level</th>
</tr>
</thead>
<tbody>
<tr>
<td>Use the established framework for Si qualification and reliability</td>
<td>Show that GaN is reliable for the actual switching application</td>
</tr>
<tr>
<td>Address GaN Failure mechanisms and calculate lifetimes</td>
<td>Use JEDEC guidelines for measuring dynamic Rds-on and selecting a stress test circuit</td>
</tr>
<tr>
<td></td>
<td>Assure robustness for extreme operating conditions like lightning surge and short circuit</td>
</tr>
</tbody>
</table>

**Standards**
- JESD47, AEC-Q100, JEP122
- JEP122, JEP180, literature
- JEP180: Switching Reliability Evaluation for GaN Power Devices
- JEP173: Dynamic ON-Resistance Test Method
- JEP182: Continuous Switching Test Method
- IEC 61000-4-5, VDE0884-11

# Failure modes are caused by failure mechanisms

<table>
<thead>
<tr>
<th>Level</th>
<th>Failure mode</th>
<th>Failure mechanism</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component level</td>
<td>Increase in leakage current</td>
<td>Time Dependent Breakdown (TDB)</td>
</tr>
<tr>
<td></td>
<td>Lower efficiency and overheating due to increase in dynamic $R_{ds-on}$</td>
<td>Charge trapping</td>
</tr>
<tr>
<td></td>
<td>Hard-failure</td>
<td>Time Dependent Breakdown (TDB)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hot-carrier wear-out (switching)</td>
</tr>
<tr>
<td>Power supply level</td>
<td>Third quadrant related (1)</td>
<td>None found</td>
</tr>
<tr>
<td></td>
<td>Hard-commutation related</td>
<td>Reverse recovery</td>
</tr>
<tr>
<td></td>
<td>Miller turn-on shoot-through (2)</td>
<td>Device hold-off at high slew rate</td>
</tr>
<tr>
<td></td>
<td>GaN device interaction with driver and system</td>
<td>Avalanching of Si FET during turn-off due to $C_{oss}$ mismatch in Cascode GaN</td>
</tr>
</tbody>
</table>

(2) "Optimizing GaN performance with an integrated driver", www.ti.com/lit/wp/styy085/styy085.pdf
Component failure mechanisms

1. Time dependent breakdown
   - High fields cause defect generation over time, increasing the leakage currents and causing eventual hard-failure
   - Well known and studied for dielectrics used in Si IC’s

2. Charge trapping
   - Charge is trapped due to high voltages and by hot electrons created by hard-switching
   - This increases on-resistance by repelling channel electrons, which increases channel resistance.
   - Dynamic Rds-on is high on the timescales of switching. It is difficult to measure on a tester, since the traps discharge quickly.

3. Hot carrier wearout (discussed later)
What does traditional Si qualification mean?

1. How long is the device qualified for?

<table>
<thead>
<tr>
<th>Use case</th>
<th>Qualification condition</th>
<th>Use condition</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Tj (°C)</td>
<td>Time (h)</td>
</tr>
<tr>
<td>Traditional</td>
<td>125</td>
<td>1000</td>
</tr>
<tr>
<td>Power (Si)</td>
<td>150</td>
<td>1000</td>
</tr>
<tr>
<td>Power (GaN)</td>
<td>150</td>
<td>1000</td>
</tr>
</tbody>
</table>

2. Is traditional testing representative of actual-usage?
   • *It does not consider the switching conditions of power management.*

3. Will there be many field returns?
   • Statistics below are based upon qualification testing with zero fails out of 3x77 parts.
   • Assumes that the applied stress is representative of actual-use

<table>
<thead>
<tr>
<th>Metric</th>
<th>Value</th>
<th>Confidence</th>
<th>criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fail% (LTPD†)</td>
<td>&lt;1%</td>
<td>90%</td>
<td>0 fails/231 for non-accelerated time</td>
</tr>
<tr>
<td>FIT rate¶</td>
<td>&lt;50</td>
<td>60%</td>
<td>0 fails/18.2M run hours</td>
</tr>
</tbody>
</table>

Traditional qualification *is a good manufacturing, quality and reliability milestone.*

† LTPD=Lot Tolerant Percent Defective
¶ 1 FIT=1 fail in 1E9 device hours

Application reliability: not traditionally covered


<table>
<thead>
<tr>
<th>state</th>
<th>mode</th>
<th>coverage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static</td>
<td>off</td>
<td>HTRB</td>
</tr>
<tr>
<td></td>
<td>on</td>
<td>HTGB</td>
</tr>
<tr>
<td>Switching</td>
<td>(hard) turn-on</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(soft) turn-off</td>
<td></td>
</tr>
<tr>
<td>deadtime</td>
<td>3Q</td>
<td></td>
</tr>
</tbody>
</table>

**Static Switching Deadtime Static**

<table>
<thead>
<tr>
<th></th>
<th>Static</th>
<th>Switching</th>
<th>Deadtime</th>
<th>Static</th>
</tr>
</thead>
<tbody>
<tr>
<td>HS</td>
<td>on</td>
<td>~soft</td>
<td>off</td>
<td>off</td>
</tr>
<tr>
<td>LS</td>
<td>off</td>
<td>off</td>
<td>3Q</td>
<td>on</td>
</tr>
</tbody>
</table>

**Switching Deadtime SW Static**

<table>
<thead>
<tr>
<th></th>
<th>static</th>
<th>dead time</th>
<th>sw</th>
<th>static</th>
</tr>
</thead>
<tbody>
<tr>
<td>HS</td>
<td>off</td>
<td>off</td>
<td>hard</td>
<td>on</td>
</tr>
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<td>on</td>
<td>3Q</td>
<td>off</td>
<td>off</td>
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Switching reliability: JEP180

- Traditional qualification does not consider the switching stress of power supplies
- JEP180 assures that GaN parts will operate reliably in the intended application

**Key aspects**

<table>
<thead>
<tr>
<th>Component level</th>
<th>Power supply level</th>
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<tr>
<td>How to obtain broad coverage</td>
<td>How to validate switching lifetime</td>
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<tr>
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<td>How to validate application-use reliability</td>
</tr>
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**Approach**

- Classify switching-stress type with switching locus
- Harsher stress condition covers milder use-case
- Chose a test-vehicle circuit appropriate for accelerating the desired switching-stress type
- Run Accelerated Lifetime Testing for the technology platform to generate a model and calculate lifetime
- Run Dynamic HTOL testing for application operating modes by using a product-vehicle circuit

JEDEC JEP180, “Guideline for Switching Reliability Evaluation Procedures for Gallium Nitride Power Conversion Devices”, Fig. 1
Obtaining broad coverage: fundamentals

• Power management circuits apply switching stimuli to devices
• Switching stimulus causes stress, which excites failure mechanisms.
• Failure mechanisms are linked to the type of switching stress. For example, hard-switching creates hot carriers, exciting hot-carrier wearout and charge trapping mechanisms.
• Classifying the switching stress type allows broad coverage. It also allows the relevant stress to be applied by circuits\(^1\) that are better suited for accelerating the desired failure modes.
• Broad coverage is achieved by linking switching stimuli to failure mechanisms through the switching locus curve

\(^1\) JEDEC JEP182 “Test Method for Continuous-Switching Evaluation of Gallium Nitride Power Conversion Devices”
Switching locus curve - introduction

• The switching locus curve is familiar to many engineers
• Switching locus curve shows the trajectory of the $i_D$-$v_{DS}$ waveform during a switching cycle
• A common example is the load line for resistive-load switching

Source: Fig. 2, JEDEC JEP180
Switching locus curve – hard switching

Hard-switching creates hot-carriers, which can excite different failure mechanisms vs off-state

Switching locus: classify switching stress

A broad category of circuits have similar loci and subject FETs to similar switching stress. This allows focus on the stress seen by the device, and the selection of a circuit better suited to reliability testing.

High-side device in a buck converter (hard turn-on). Turn-off is not hard since the channel is off while Vds rises ($i_D$ is from Coss charging).

Low-side device in a buck converter (soft turn-on and turn-off)

Boost converter: Interchange high and low-side loci

Switching locus figures source: Fig. 2, JEDEC JEP180
Broad hard-switching coverage

- All hard-switched circuits turn on the switch in the same manner
- This is shown by the identical switching locus curves for the same slew-rate
- Switches under both buck and boost operation get the same switching stress.

(simulation)
Validating switching reliability: JEP180

- Traditional qualification does not consider the switching stress of power supplies
- JEP180 assures that GaN parts will operate reliably in the intended application

**Key aspects**

- How to obtain broad coverage
- How to validate switching lifetime
- How to validate application-use reliability

**Approach**

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Source: Fig. 1, JEDEC JEP180
Literature summary on switching lifetime

A. Ikoshi et al. (Panasonic), "Lifetime Evaluation for Hybrid-Drain-embedded Gate Injection Transistor (HD-GIT) under Practical Switching Operations", IRPS 2018, p4E2-1

N. Modolo et al. (U. Padova), "A Generalized Approach to Determine the Switching Reliability of GaN HEMTs on-Wafer Level", IRPS 2021

M. Lin et al. (TSMC) "New Circuit Topology for System-Level reliability of GaN", ISPSD 2019, p299

D. Gandhi (Navitas), "Systematic Approach to GaN Power IC Reliability, APEC PSMA Industry session IS11, 2019

TI switching lifetime: following slides

600 V – 650V FETs
Charge trapping: dynamic $R_{ds-on}$ with aging

- Charge trapping causes higher dynamic $R_{ds-on}$, which results in more self-heating and lower efficiency
- Device aging can increase trap density and result in higher dynamic $R_{ds-on}$
- Need to validate that new traps are not being generated with aging
Validating dynamic Rds-on reliability

Hard-switching test system, for dynamic Rds-on (and hot-carrier wearout) reliability
Dynamic Rds-on does not increase with aging

- Low duty-cycle stress provides high trap filling and higher sensitivity to charge trapping\(^1\)
- It provides an early detection method for aging by making dRon sensitive to early-stage traps (less electrically active).
- Stable dRon at low duty cycle demonstrates lack of new trap creation and excellent material quality with aging.

Challenges in determining switching lifetime

• The complexity of the switching transition
• The dependence of the stress rate on the application
• The lack of a broad modeling approach

Stress using a test-vehicle circuit suitable for accelerated stress

Evaluate switching lifetime for broad application use
Calculating switching stress

- Prior-art uses fixed parametric values, e.g. $V_{bus}$, peak current, etc.
- We integrate the switching waveform with wearout acceleration factors to calculate the switching stress.
- Integration captures the complexity of the switching waveform.

$$\Delta Stress = \nu_{DS} \times AF^V \times i_{Device} \times AF^I \times \Delta time$$

(AF = Acceleration Factor)

$$Stress[1] = \sum_{t (start)}^{t (end)} \Delta Stress(t)$$

[1] Builds upon Ikoshi et. al, IRPS 2018, 4E.2-1 that wearout from switching stress is cumulative.

**Hot carrier wearout: switching lifetime model**

- Hard switching generates hot carriers, which can cause wearout
- TI tests for hot carrier wearout by using accelerated hard-switching

### Stress using a test-vehicle circuit suitable for accelerated stress

### Evaluate switching lifetime for broad application use

**Construct switching stress model**

- **Voltage acceleration**
  - Exponential model (TDDB): \( TTF \propto e^{-\beta_V(V_{DS})} \)
  - \( \beta_V = 0.109 \)

- **Current acceleration**
  - Exponential model: \( TTF \propto e^{-\beta_I(I_{ch})} \)
  - Power-law model: \( TTF \propto (I_{ch})^{-n} \)
  - \( \beta_I = 0.283 \)
  - \( n = 3.1 \)

- **Temperature acceleration**
  - Arrhenius model: \( TTF \propto e^{\frac{E_a}{kT}} \)
  - \( E_a = 0.7 \text{ eV} \)

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Lifetime extrapolations: hard switching

- Exponential model was used (was more conservative – lower lifetime)
- Over 1 billion years switching lifetime for 400 V, 8 A hard-switching at 100 kHz
- Hot carrier wearout is not an issue!
Validating switching reliability: JEP180

- Traditional qualification does not consider the switching stress of power supplies
- JEP180 assures that GaN parts will operate reliably in the intended application

### Key aspects

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<td>Run Dynamic HTOL testing for application operating modes by using a product-vehicle circuit</td>
<td></td>
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</tbody>
</table>

### Switching locus
- Charge trapping and Hot-electron wearout

### Power-supply level failure modes

Source: Fig. 1, JEDEC JEP180
Literature summary on DHTOL


A. Ikoshi et al. (Panasonic), “DHTOL Life Tests for GaN Hybrid-Drain ΓΙTs”, APEC Industry Session IS16-02, 2018

T. McDonald, “Reliability and qualification of CoolGaN”, Infineon whitepaper

TI DHTOL summary: following slides

Power-supply level stresses

Third quadrant

Hard-commutation (reverse recovery)

Miller turn-on shoot-through

GaN device interaction with driver (and other system components)
Reliable power-supply operation: DHTOL testing

H-bridge circuit
- Recycle power
- Both hard and soft-switching stress at high power
- In-system stress modes

Application half-bridge boards under stress
Validating in-system reliability (DHTOL, JEP180)

LMG34xx TI GaN half-bridges run at 480V/125C, 150 kHz, 100 V/ns slew rate and maximum-power hard-switching stress conditions for 1000h.

<table>
<thead>
<tr>
<th>Rds-on (mohm)</th>
<th>Power (kW)</th>
<th>no. of half-bridges</th>
<th>no. of parts</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>3.8</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td>50</td>
<td>1.9</td>
<td>12</td>
<td>24</td>
</tr>
<tr>
<td>150</td>
<td>1.4</td>
<td>12</td>
<td>24</td>
</tr>
</tbody>
</table>

64 parts ran from multiple lots of the LMG34xx product family

Reliable in-system operation for **both hard and soft switching**: stable running with efficiency within 0.1%
Reliable operation under all conditions

During operation, abnormal or extreme conditions can occur

- The load can short circuit
  - Overcurrent protection would turn the FET off in a latched or cycle-by-cycle manner
- A line surge can occur from an event like a lightning strike
  - The power FET needs to be surge robust
- The supply voltage may dip
  - If the supply voltages go below a threshold, UVLO protection would pause power FET switching until the voltage recovers.
- The die temperature may get too high, such as if there is a cooling issue
  - If the die temperature exceeds the threshold, overtemperature protection turns the power FET off and notifies the system.
Short-circuit robustness

- A 10-μs withstand time was traditionally required for an external hardware protector to sense the short circuit and turn off the power device\(^1\). Driver ICs are faster now, with response times of less than 0.5 μs\(^2\).

- A GaN HEMT has a smaller active volume and higher saturation current than an IGBT, so heats up faster during short circuit. For a 400 V hard short circuit, the fail time could be less than 1 μs\(^3\).

- There are two broad approaches being followed:
  - Reduce \(I_{\text{dsat}}\) or \(I_d\), which increases the short-circuit withstand time
  - Turn off the power FET earlier

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\(^1\) "Robustness in Short-Circuit Mode: Benchmarking of 600 V GaN HEMTs with Power Si and SiC MOSFETs", Badawi et. al, ECCE 2016
\(^2\) e.g. TI UCC21750 at https://www.ti.com/product/UCC21750
Reduced drain current increases SC withstand time

(a) $I_D(SAT)$ reduction by process change

Remove segments of 2DEG near source. (some increase in $R_{ds}$-on)

“Short-Circuit Capability Demonstrated for GaN Power Switches”, D. Bisi et al., APEC 2021

(b) $I_D$ reduction by lowering gate-source voltage

Lower $V_{gs}$ increases short-circuit (SC) withstand time

Integration allows to turn off the FET earlier

- Integration of GaN power FET in a low-inductance package with a Si driver and protection allows fast detection and turn-off.
- Built-in protection eliminates delay needed for external components.

Surge robustness: No avalanche? No problem!

- Power line disturbances can occur due to lightning strikes, malfunction, load and capacitor bank switching, etc.
- Silicon devices use their avalanche rating property to survive these events.
- The use of avalanche is historical. It arises because silicon FETs do not have much voltage headroom above their maximum voltage rating. When a surge strikes, they break down (by impact-ionization).
- Over the years, the silicon industry has improved the ability of power FETs to survive avalanche breakdown. As a result, avalanche ability has become associated with surge protection.
- GaN has good transient overvoltage capability. This allows GaN FETs to switch through surge without avalanche breakdown and disruption. It also improves system reliability, since MOV degradation can cause failure of Si FETs by subjecting them to higher levels of avalanche.

“No avalanche? No problem! GaN FETs are surge robust”, available at https://e2e.ti.com/blogs_/b/powerhouse/posts/no-avalanche-no-problem-gan-fets-are-surge-robust
GaN has transient overvoltage capability

- GaN can exceed its rated voltage for short bursts
- In GaN, the voltage rating is not limited by avalanche
- GaN FET manufacturers are including a transient voltage rating in the datasheet for 600-650 V GaN FETs

<table>
<thead>
<tr>
<th>Part</th>
<th>V_{DS(tr)} Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>GS66508B</td>
<td>V_{DS(transient)}</td>
<td>750 V</td>
</tr>
<tr>
<td>InnoSwitch4</td>
<td>V_{MAX(NON-REPEETITIVE)}</td>
<td>750 V</td>
</tr>
<tr>
<td>NV6117</td>
<td>V_{DS(TRAN)}</td>
<td>800 V</td>
</tr>
<tr>
<td>TPH3212PS</td>
<td>V_{DSS(TR)}</td>
<td>800 V</td>
</tr>
<tr>
<td>IGT60R070D1</td>
<td>V_{DS,pulse}</td>
<td>800 V</td>
</tr>
<tr>
<td>LMG3410R050</td>
<td>V_{DS(TR)}</td>
<td>800 V</td>
</tr>
</tbody>
</table>

- The $V_{DS(tr)}$ rating is being used for ringing of flyback converters\(^{(1)}\).
- Hard-switching circuits need different validation since the channel turns on multiple times during the surge strike and subjects the FET to hot-carrier stress.

\(^{(1)}\) "Surge-robust flyback power supplies with GaN", K. Varadarajan et. al., APEC 2020
TI’s active-power surge test

- Device: TI LMG3410R070
- Load: 1 kW
- Hard switching at 100kHz
- 105°C device case temperature.
- 720V surge peak at the device terminals

LMG3410 Half-bridge EVM card

- Devices tested under:
  - Hard-switching
  - Soft-switching
  - Third quadrant
  - Hard commutation
TI GaN: Robust to surge

- The IEC 61000-4-5 standard specifies the surge waveform
- The VDE 0884-11 standard specifies the application of 50 strikes
- We applied additional 50 strikes to assure margin
- Parts had very stable efficiency and there was no hard failure

Surge-robust design with GaN

Due to different stresses, there are two transient overvoltage ratings: $V_{DS(tr)}$ for FET off, and $V_{DS(surge)}$ for hard turn-on.

For surge-robust design, select components to keep bus voltage at device below these ratings.

- Bus voltage at device < 570 V with 4 kV surge strike
- It is straightforward to limit the voltage, even for severe surge conditions, with margin

$V_{DS(tr)}$

$V_{DS(surge)}$

$V_{bus(nominal)}$

Peak bus voltage

Margin for ringing

Surge strike

Switched node voltage

4 kV setting

$V_{IN}$

$V_{SW}$

$V_{Filter} < 570$ V
(voltage across GaN FET)

(simulation)

$L_{par} = 0.5 \mu H, C_{in} = 47 \mu F$

420 V varistor

400V DC

Load
Conclusion

• All devices have failure mechanisms which need to be understood, and be engineered for reliable operation
• For GaN, key mechanisms are TDB, charge trapping and hot-carrier wearout
• Traditional qualification does not consider switching stress of power supplies
• The GaN industry developed the JEDEC JEP 180 guideline to assure that GaN power FETs will operate reliably in the intended application
• JEP180 guides on how to validate reliability for the intended application. TI and other GaN suppliers are now conducting the types of validation recommended and showing that GaN FETs are reliable for application use.
• GaN FETs are also reliable under abnormal or extreme conditions of short circuit and surge.

GaN FETs are reliable and ready to use