GaN power devices and applications reliability

Presented at the PowerAmerica Wide Bandgap Devices and Applications Short Course

Nov 17, 2021

Sandeep R. Bahl, PhD

Distinguished Member of Technical Staff, Texas Instruments

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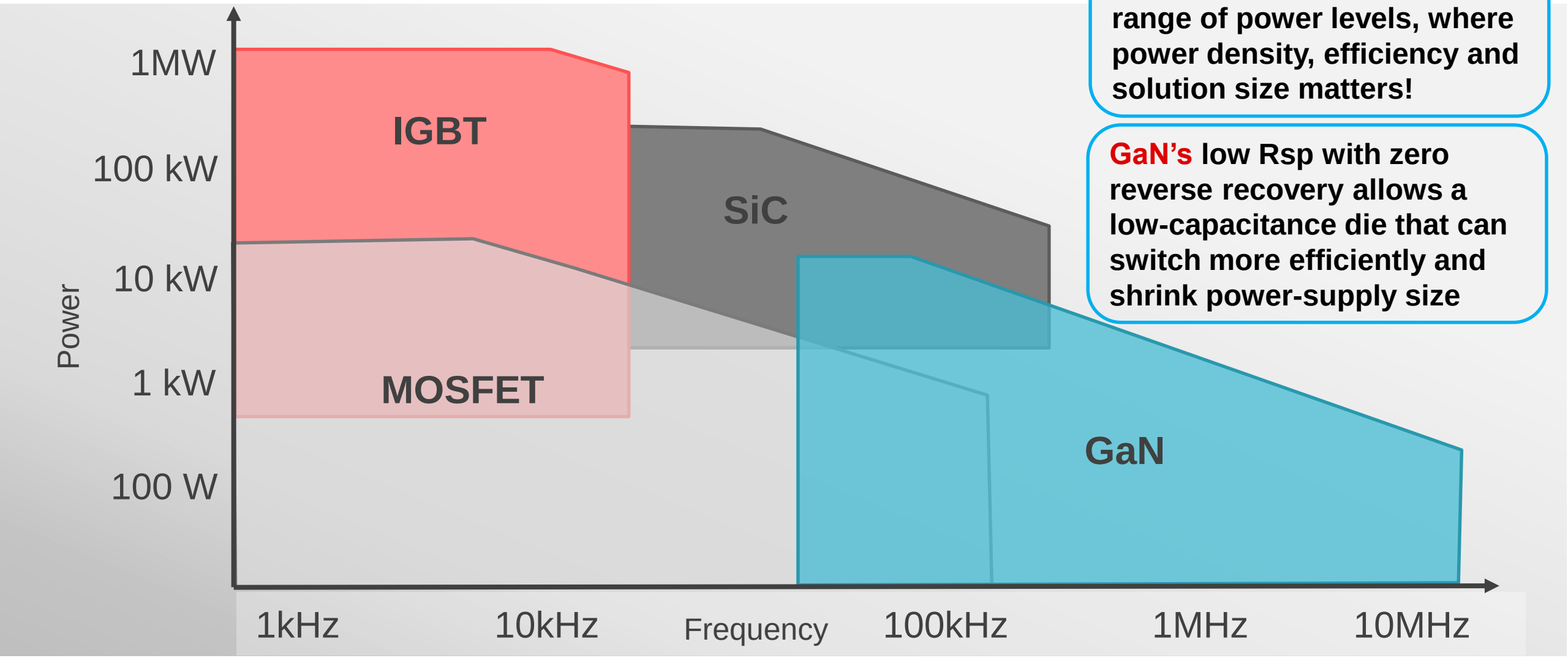
Outline

- Device structure
- Failure mechanisms
- The gaps for power management usage in traditional silicon qualification
- Addressing the gaps and assuring application reliability with JEP180
  - Broad coverage: switching locus
  - Validating switching lifetime
  - Validating application-use reliability (DHTOL)
- Reliability for unusual and extreme conditions
  - Short circuit withstand
  - Surge robustness without avalanche

Benefits of GaN

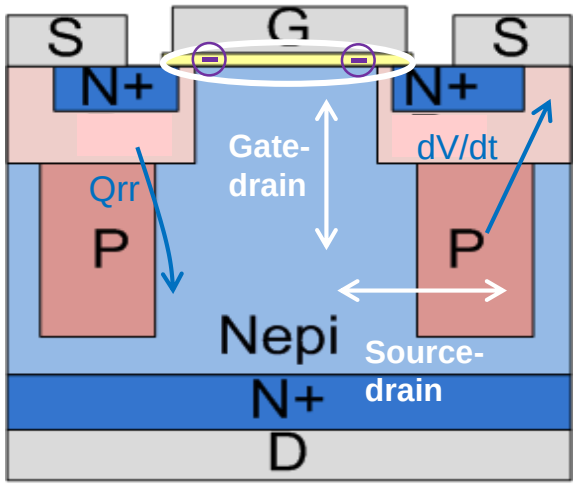


GaN enables high-frequency power converters for a wide range of power levels, where power density, efficiency and solution size matters!

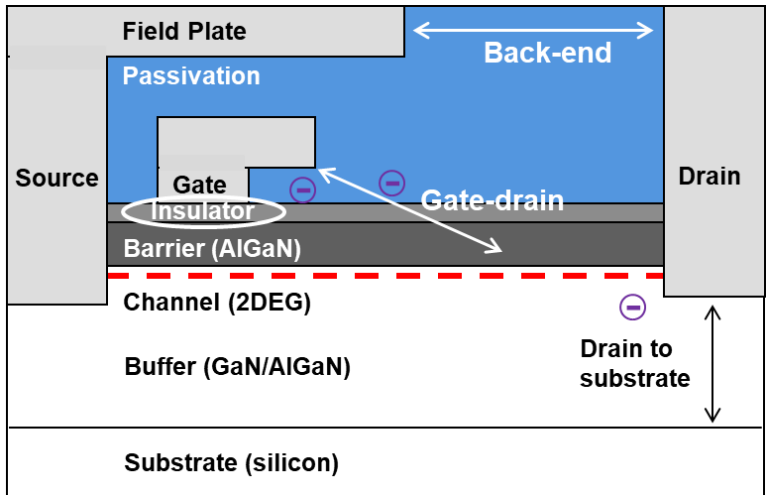
GaN's low Rsp with zero reverse recovery allows a low-capacitance die that can switch more efficiently and shrink power-supply size

Device Reliability Engineering

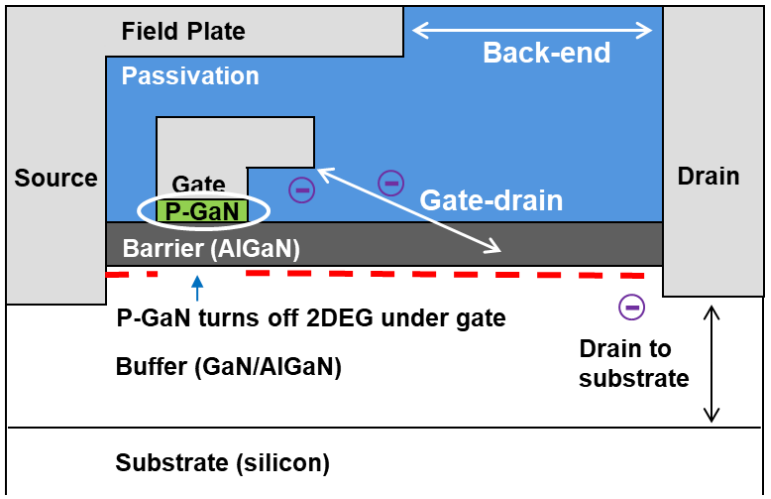
Si SJ FET



Depletion mode GaN FET



Enhancement mode GaN FET



- Every device has failure mechanisms that need to be understood and engineered
- High electric fields cause Time Dependent Breakdown (TDB)
- High fields and hot carriers cause charge trapping
- Switching causes stress from reverse recovery, high slew rates, and hot-carrier wearout
- A known GaN failure mode is the increase in Rds-on on the timescales of switching. This dynamic Rds-on increase is due to charge trapping.
- Reliability engineering consists of making FETs reliable to stresses seen in application

Steps to achieving reliable GaN

		Standards
Component level	Use the established framework for Si qualification and reliability	**JESD47, AEC-Q100, JEP122**
	Address GaN Failure mechanisms and calculate lifetimes	**JEP122**, **JEP180,** literature
Power supply level	Show that GaN is reliable for the actual switching application	**JEP180:** Switching Reliability Evaluation for GaN Power Devices
	Use JEDEC guidelines for measuring dynamic Rds-on and selecting a stress test circuit	**JEP173:** Dynamic ON-Resistance Test Method **JEP182**: Continuous Switching Test Method
	Assure robustness for extreme operating conditions like lightning surge and short circuit	**IEC 61000-4-5, VDE0884-11**

"*Achieving GaN Products With Lifetime Reliability*", TI Technical Whitepaper, available at www.ti.com/lit/wp/snoaa68/snoaa68.pdf

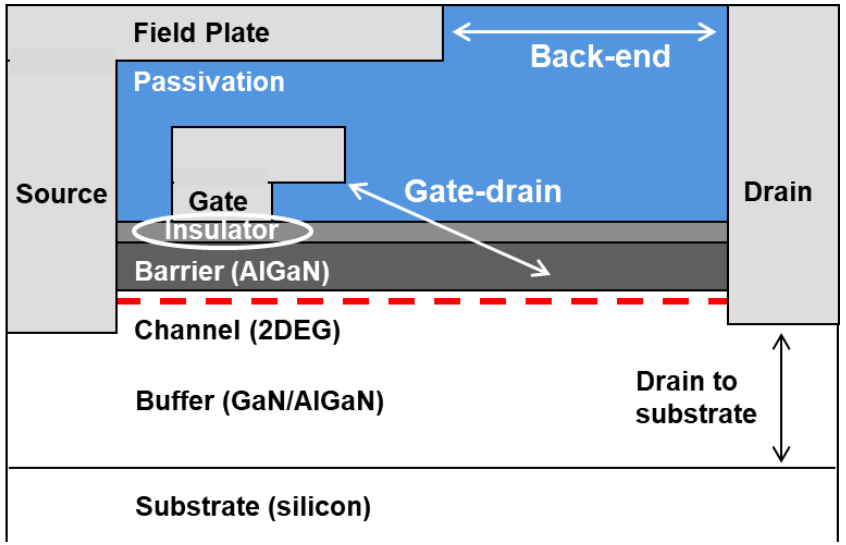
Failure modes are caused by failure mechanisms

Level	Failure mode	Failure mechanism
Component level	Increase in leakage current	Time Dependent Breakdown (TDB)
	Lower efficiency and overheating due to increase in dynamic Rds-on	Charge trapping
	Hard-failure	Time Dependent Breakdown (TDB)
		Hot-carrier wear-out (switching)
Power supply level	Third quadrant related (1)	None found
	Hard-commutation related	Reverse recovery
	Miller turn-on shoot-through (2)	Device hold-off at high slew rate
	GaN device interaction with driver and system	Avalanching of Si FET during turn-off due to Coss mismatch in Cascode GaN

(1) "*Does GaN Have a Body Diode? - Understanding the Third Quadrant Operation of GaN*", www.ti.com/lit/an/snoaa36/snoaa36.pdf
(2) "*Optimizing GaN performance with an integrated driver*", www.ti.com/lit/wp/slyy085/slyy085.pdf

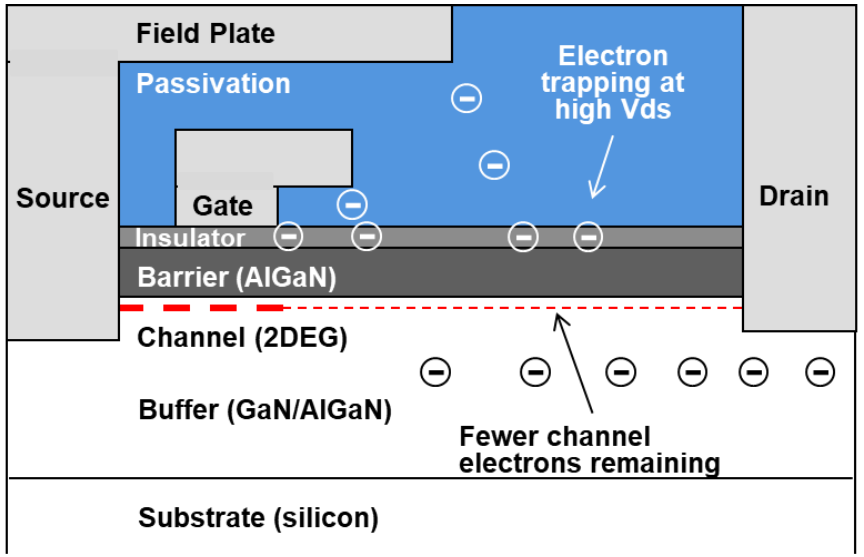
Component failure mechanisms

1. Time dependent breakdown



- High fields cause defect generation over time, increasing the leakage currents and causing eventual hard-failure
- Well known and studied for dielectrics used in Si IC's

2. Charge trapping



- Charge is trapped due to high voltages and by hot electrons created by hard-switching
- This increases on-resistance by repelling channel electrons, which increases channel resistance.
- Dynamic Rds-on is high on the timescales of switching. It is difficult to measure on a tester, since the traps discharge quickly.

3. Hot carrier wearout (discussed later)

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What does traditional Si qualification mean?

1. **How long is the device qualified for?**

Use case	Qualification condition			Use condition	
	Tj (°C)	Time (h)	Ea (eV)	Tj (°C)	Time (y)
Traditional	125	1000	0.7	55	8.9
Power (Si)	150	1000	0.7	105	1.1
Power (GaN)	150	1000	0.1-1.8	105	0.2-41

2. **Is traditional testing representative of actual-usage?**
   - *It does not consider the switching conditions of power management*.
3. **Will there be many field returns?**
   - Statistics below are based upon qualification testing with zero fails out of 3x77 parts.
   - Assumes that the applied stress is representative of actual-use

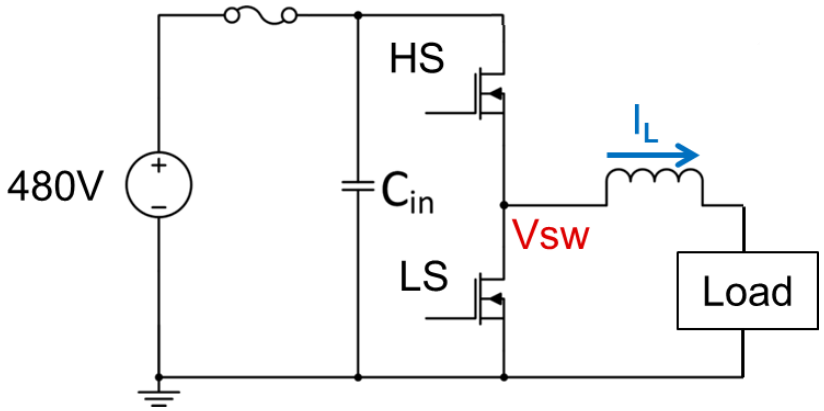
Metric	Value	Confidence	criteria
Fail% (LTPD†)	<1%	90%	0 fails/231 for non-accelerated time
FIT rate¶	<50	60%	0 fails/18.2M run hours

Traditional qualification is a good manufacturing, quality and reliability milestone.

† LTPD=Lot Tolerant Percent Defective
¶ 1 FIT=1 fail in 1E9 device hours

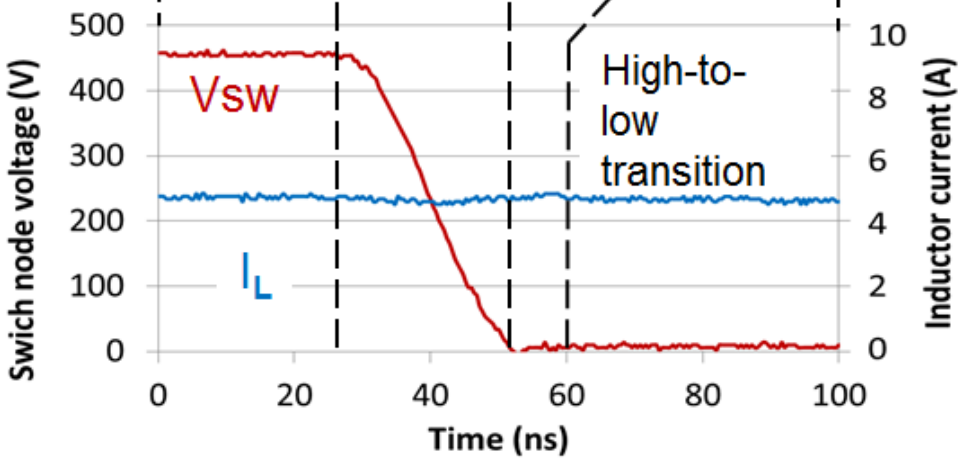
"*A comprehensive methodology to qualify the reliability of GaN products*", available at www.ti.com/lit/wp/slyy070/slyy070.pdf

Application reliability: not traditionally covered

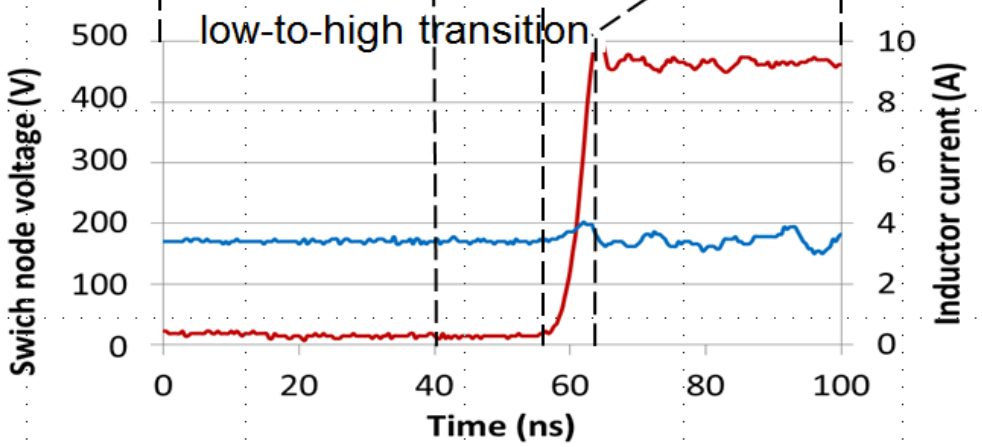


state	mode	coverage
Static	off	HTRB
	on	HTGB
Switching	(hard) turn-on	
	(soft) turn-off	
deadtime	3Q	

	Static	Switching	Dead time	Static
HS	on	~soft	off	off
LS	off	off	3Q	on



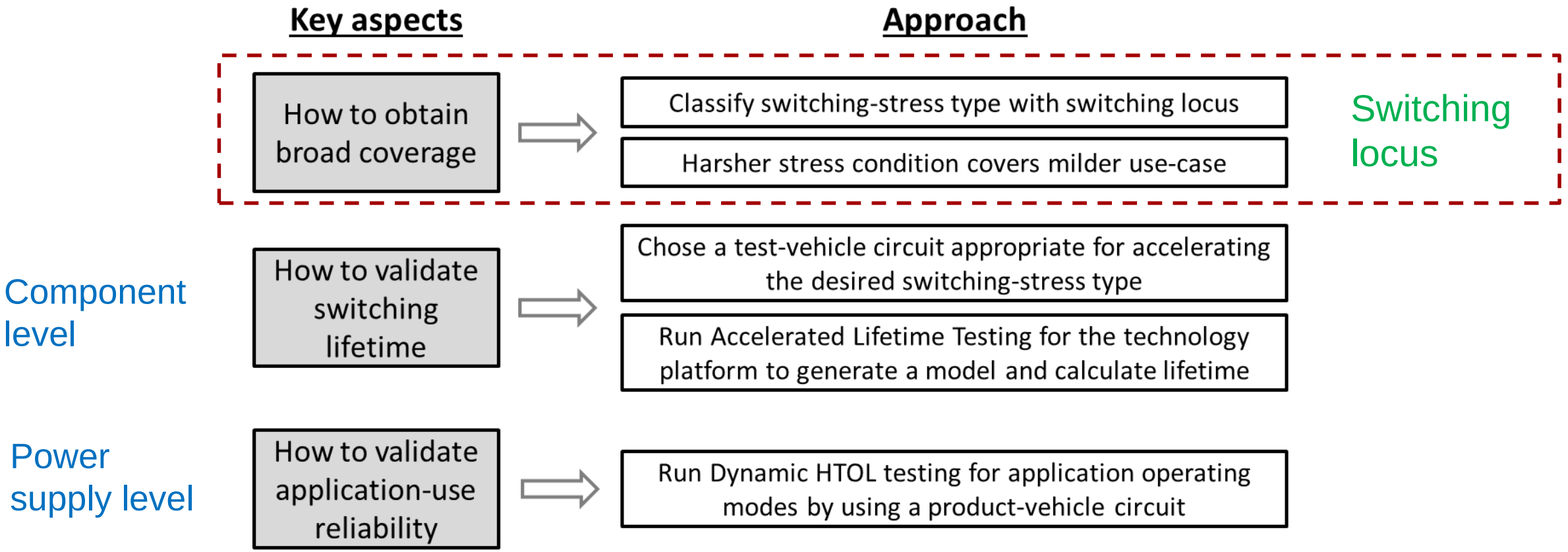
	static	dead time	sw	static
HS	off	off	hard	on
LS	on	3Q	off	off



"*System-level reliability validation of GaN devices for power management*" APEC 2017, available at www.ti.com/lit/ml/slyy135/slyy135.pdf

Switching reliability: JEP180

- Traditional qualification does not consider the switching stress of power supplies
- JEP180 assures that GaN parts will operate reliably in the intended application



JEDEC JEP180, "*Guideline for Switching Reliability Evaluation Procedures for Gallium Nitride Power Conversion Devices*", Fig. 1

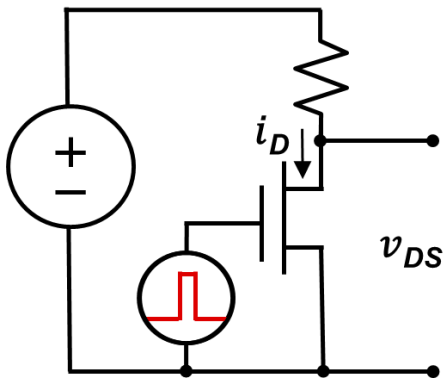
Obtaining broad coverage: fundamentals

- Power management circuits apply switching stimuli to devices
- Switching stimulus causes stress, which excites failure mechanisms.
- Failure mechanisms are linked to the type of switching stress. For example, hard-switching creates hot carriers, exciting hot-carrier wearout and charge trapping mechanisms.
- Classifying the switching stress type allows broad coverage. It also allows the relevant stress to be applied by circuits(1) that are better suited for accelerating the desired failure modes.
- Broad coverage is achieved by linking switching stimuli to failure mechanisms through the *switching locus curve*

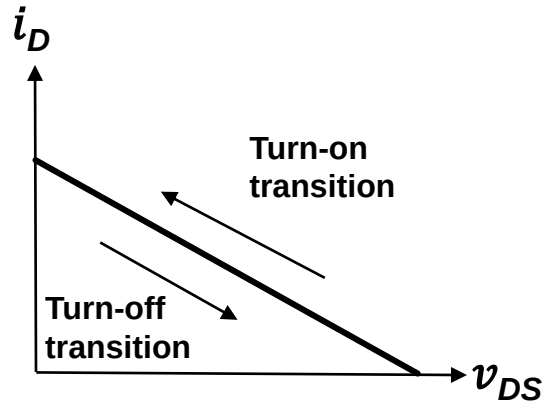
(1) JEDEC JEP182 "*Test Method for Continuous-Switching Evaluation of Gallium Nitride Power Conversion Devices*"

Switching locus curve - introduction

- The switching locus curve is familiar to many engineers
- Switching locus curve shows the trajectory of the i_D-v_{DS} waveform during a switching cycle
- A common example is the load line for resistive-load switching

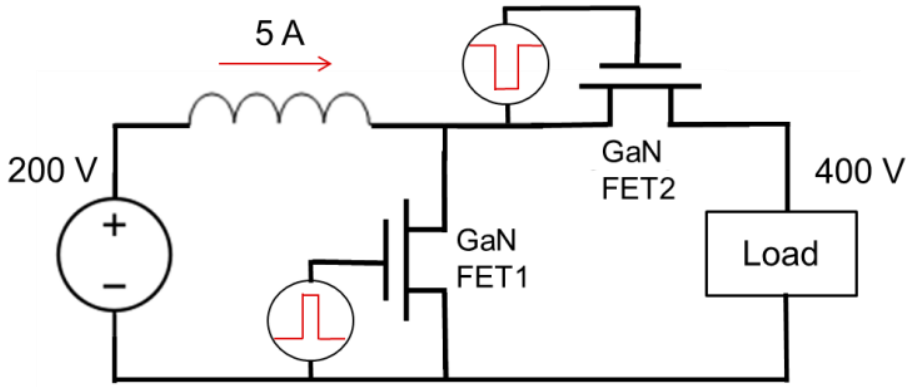


Switching locus curve for resistive switching

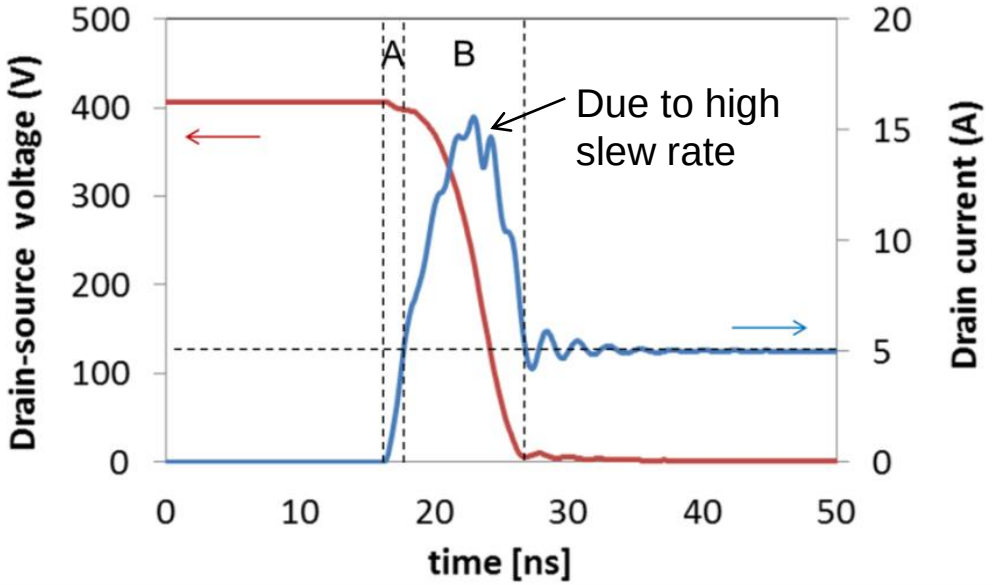


Source: Fig. 2, JEDEC JEP180

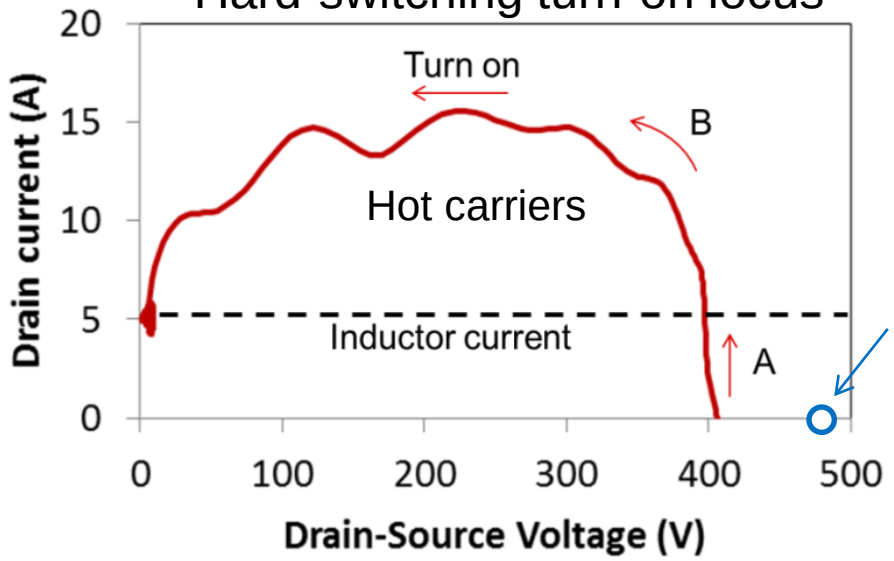
Switching locus curve – hard switching



FET1 V_{DS} and I_D



Hard-switching turn-on locus



Typical High Temperature Reverse Bias (HTRB) test (off-state)

Hard-switching creates hot-carriers, which can excite different failure mechanisms vs off-state

"*Product-level Reliability of GaN Devices*", IEEE IRPS 2016, available at www.ti.com/lit/ml/slyy093/slyy093.pdf

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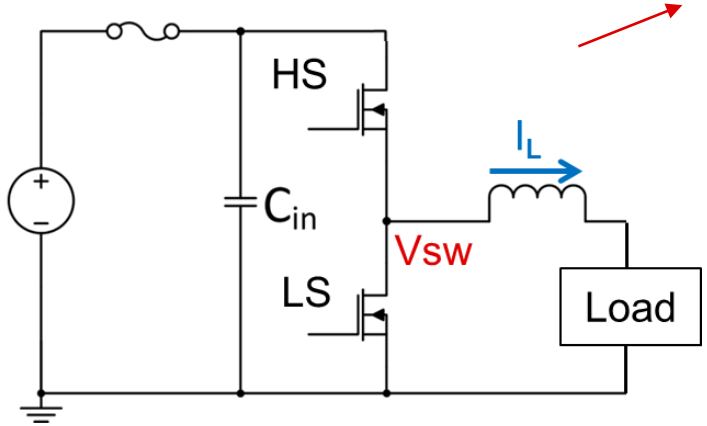
Switching locus : classify switching stress

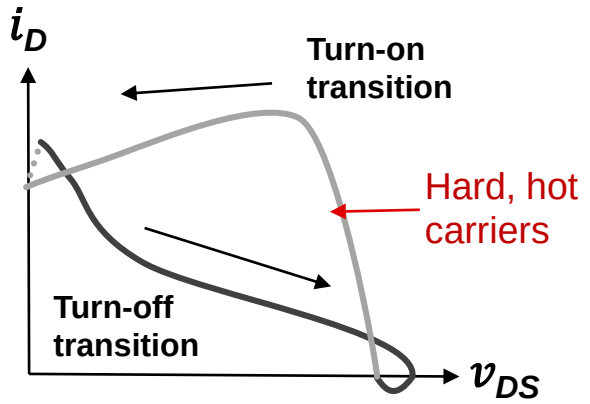
A broad category of circuits have similar loci and subject FETs to similar switching stress. This allows focus on the stress seen by the device, and the selection of a circuit better suited to reliability testing.

Buck converter

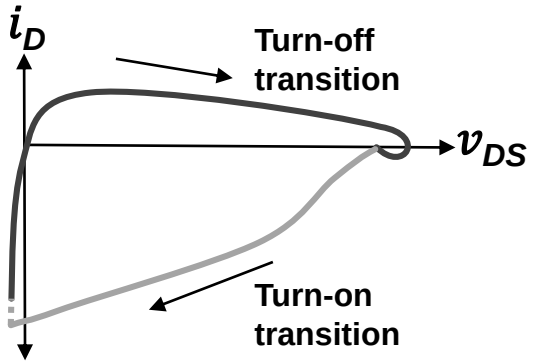


Boost converter: Interchange high and low-side loci

High-side device in a buck converter (hard turn-on). Turn-off is not hard since the channel is off while Vds rises (i_D is from Coss charging).



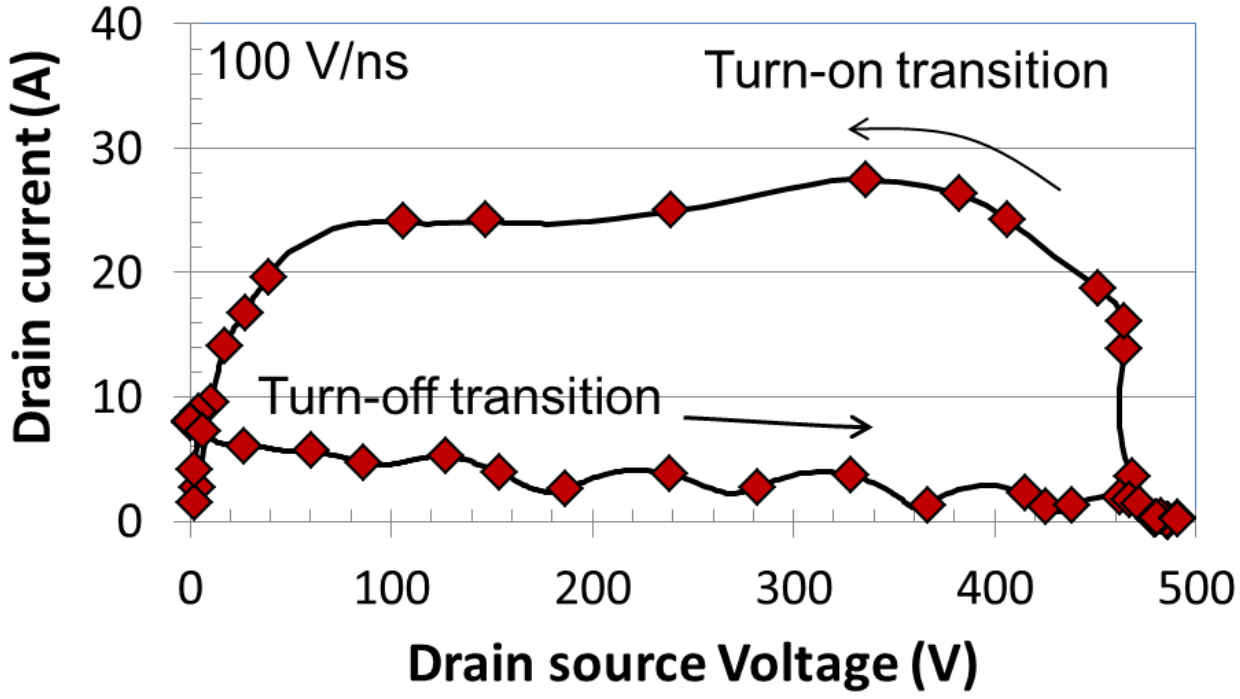
Low-side device in a buck converter (soft turn-on and turn-off)



Switching locus figures source: Fig. 2, JEDEC JEP180

Broad hard-switching coverage

- All hard-switched circuits turn on the switch in the same manner
- This is shown by the identical switching locus curves for the same slew-rate
- Switches under both buck and boost operation get the same switching stress.



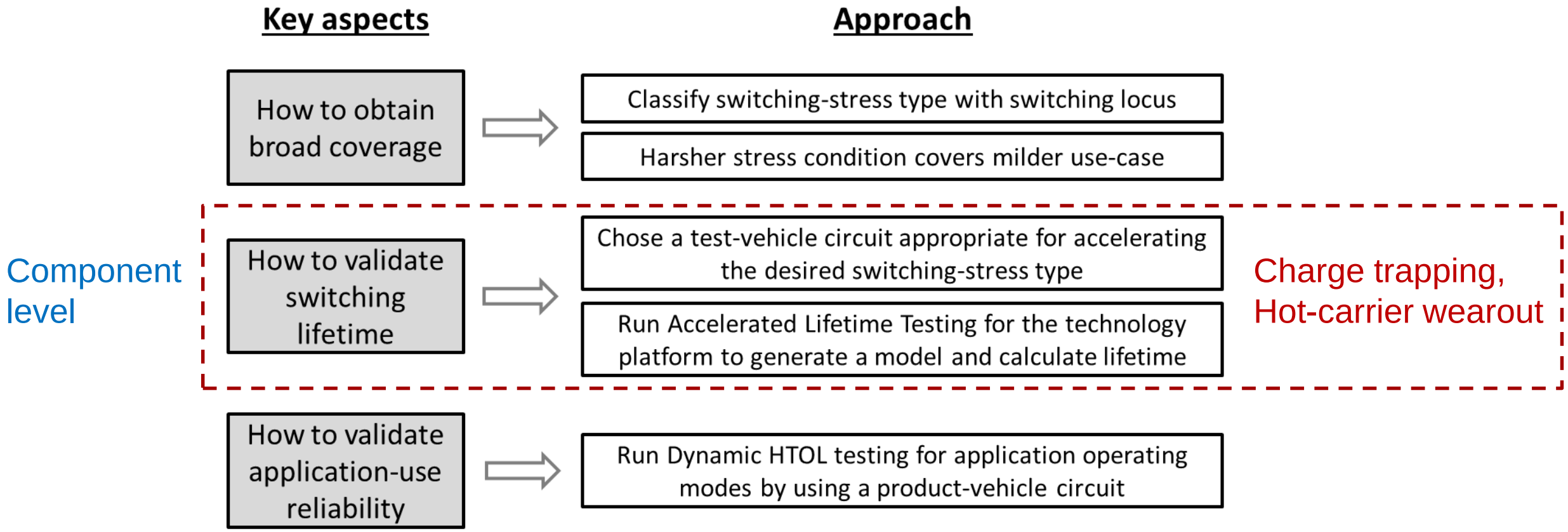
Boost converter

Buck converter

(simulation)

Validating switching reliability: JEP180

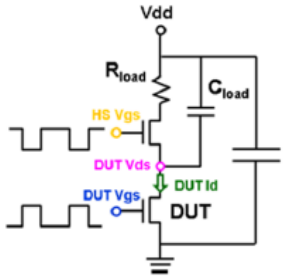
- Traditional qualification does not consider the switching stress of power supplies
- JEP180 assures that GaN parts will operate reliably in the intended application

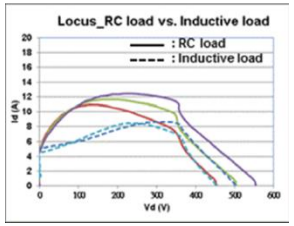


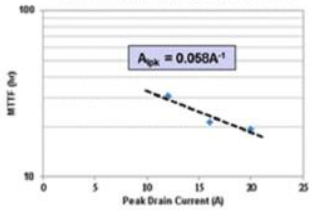
Source: Fig. 1, JEDEC JEP180

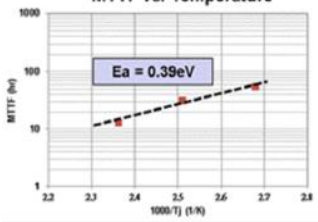
Literature summary on switching lifetime

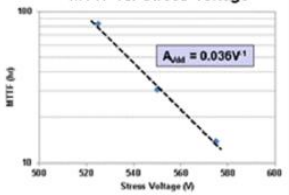
600 V – 650V FETs



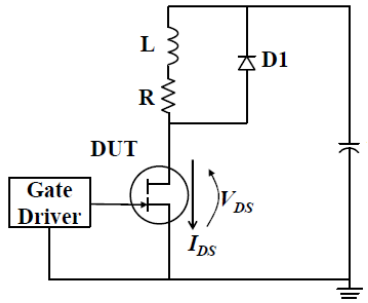


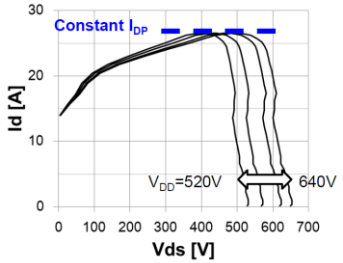


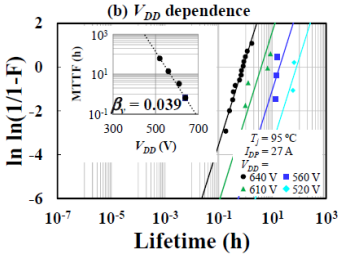


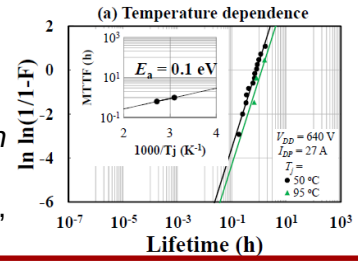


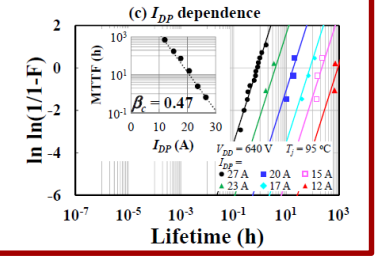
M. Lin et al. (TSMC) "New Circuit Topology for System-Level reliability of GaN", ISPSD 2019, p299





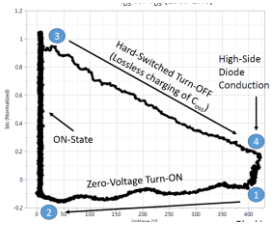


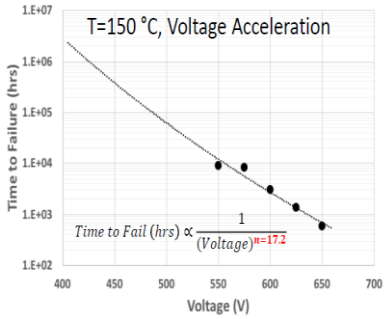


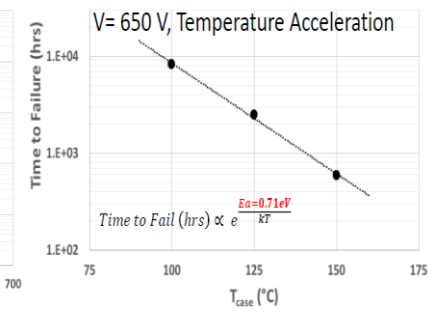


A. Ikoshi et al. (Panasonic), *Lifetime Evaluation for Hybrid-Drain-embedded Gate Injection Transistor (HD-GIT) under Practical Switching Operations*, IRPS 2018, p4E2-1

Switching locus

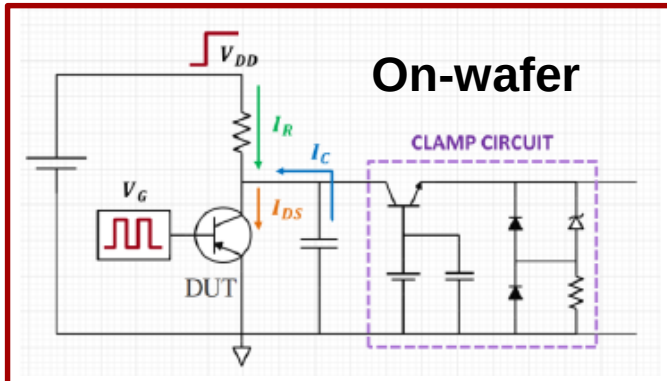


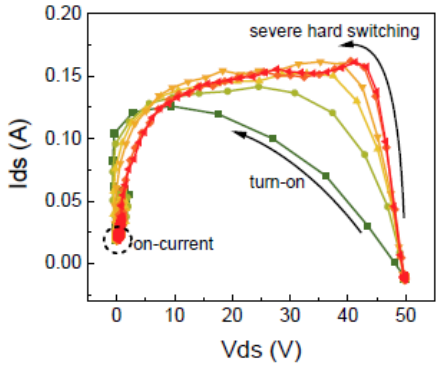




D. Gandhi (Navitas), "Systematic Approach to GaN Power IC Reliability, APEC PSMA Industry session IS11, 2019

TI switching lifetime: following slides





N. Modolo et al. (U. Padova), "*A Generalized Approach to Determine the Switching Reliability of GaN HEMTs on-Wafer Level*", IRPS 2021

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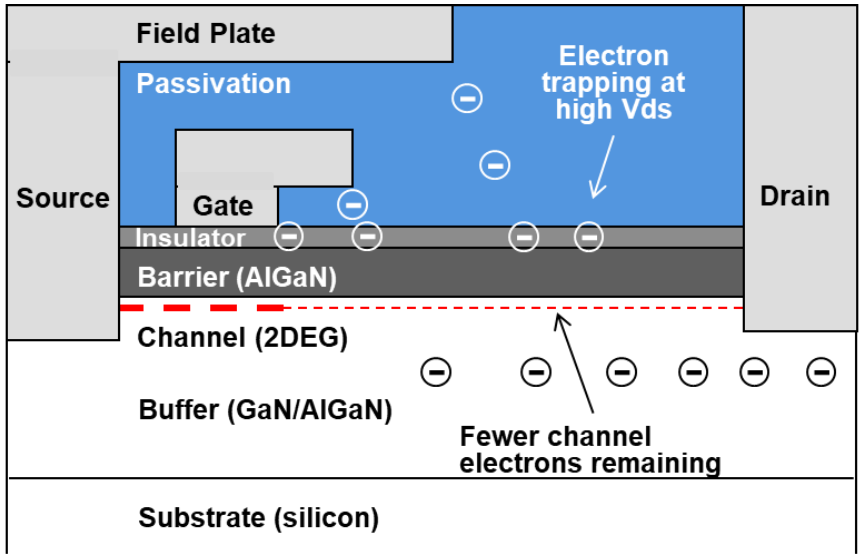
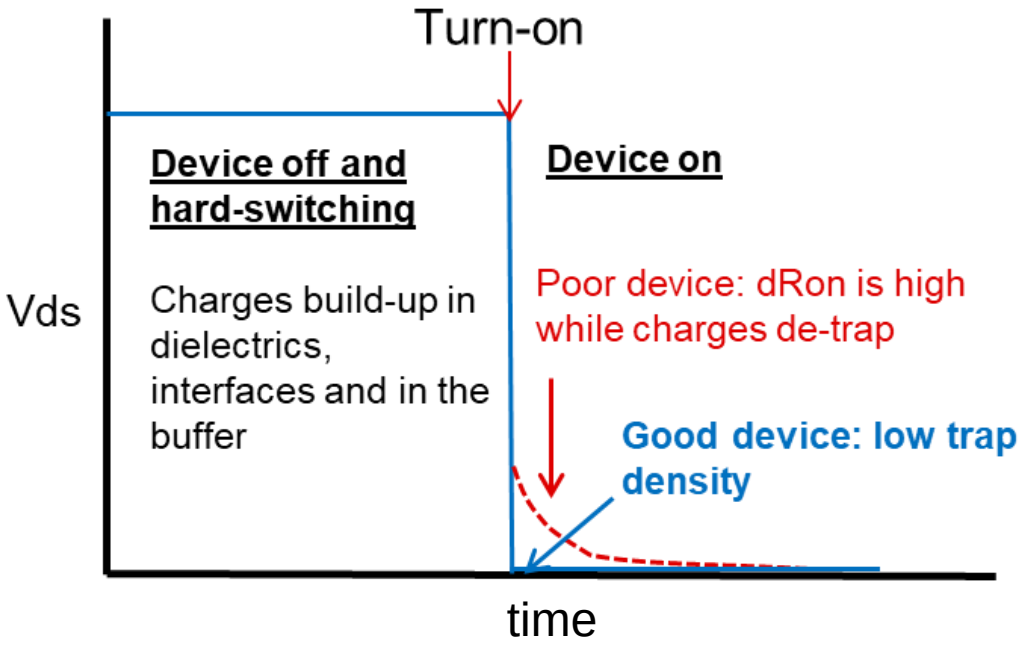
Charge trapping: dynamic Rds-on with aging

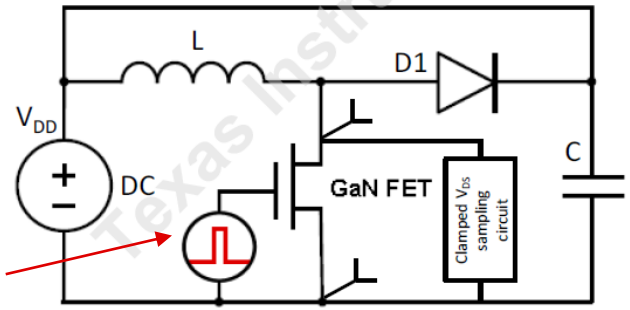




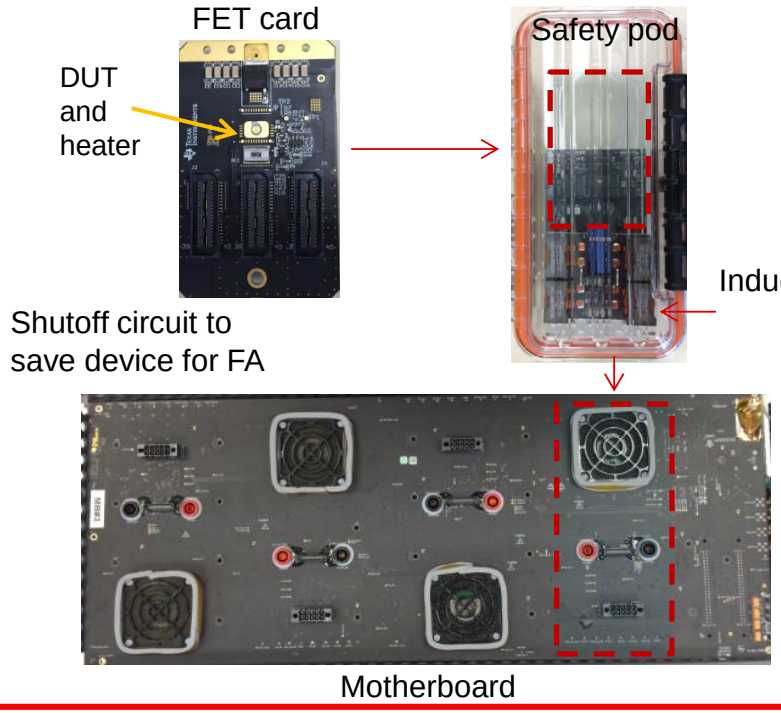
- Charge trapping causes higher dynamic Rds-on, which results in more self-heating and lower efficiency
- Device aging can increase trap density and result in higher dynamic Rds-on
- Need to validate that new traps are not being generated with aging

Validating dynamic Rds-on reliability

Stress circuit per
JEP 182
dRon measured
per JEP 173



Turn on to measure
dRon within 1-usec



Hard-switching test system, for dynamic Rds-on (and hot-carrier wearout) reliability

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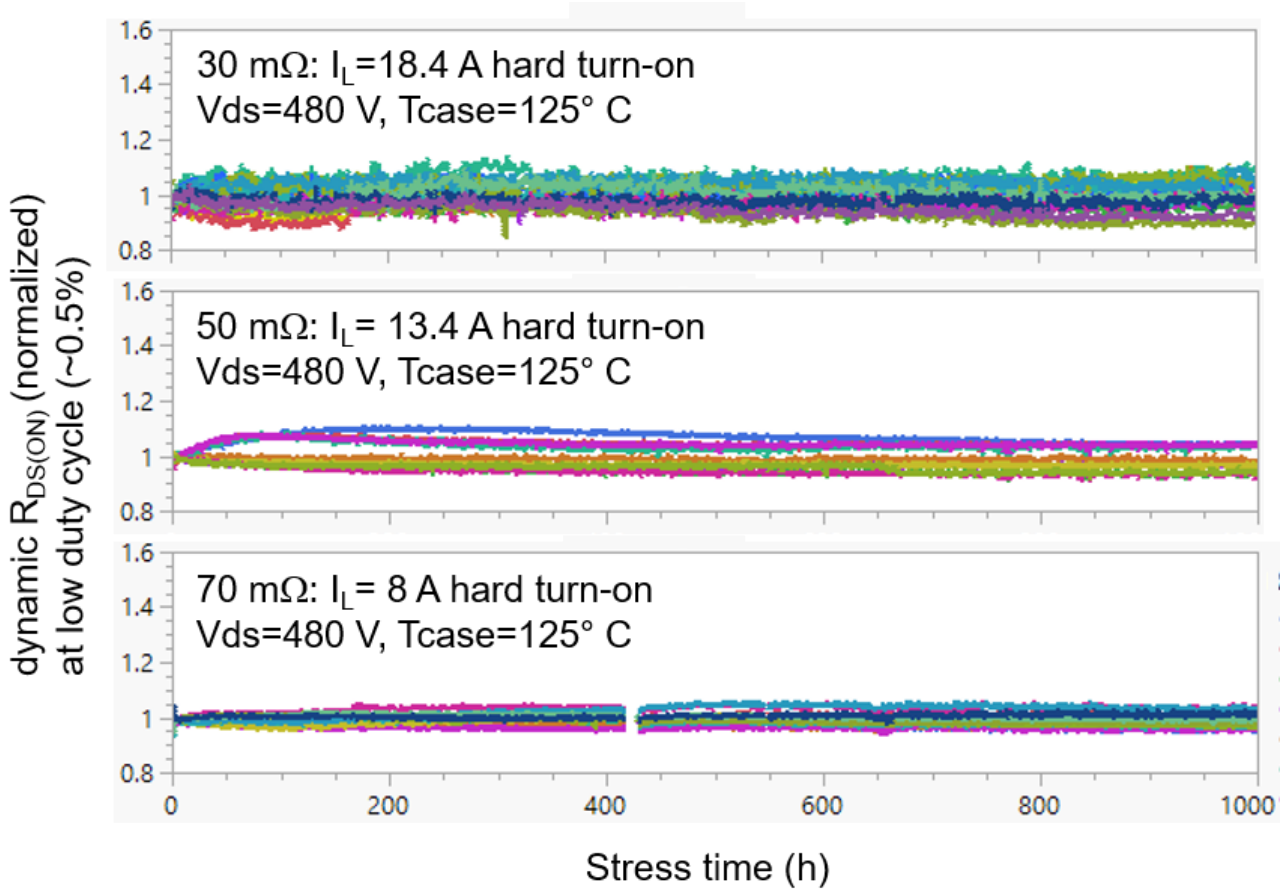
Dynamic Rds-on does not increase with aging

- Low duty-cycle stress provides high trap filling and higher sensitivity to charge trapping (1)
- It provides an early detection method for aging by making dRon sensitive to early-stage traps (less electrically active).
- Stable dRon at low duty cycle demonstrates lack of new trap creation and excellent material quality with aging



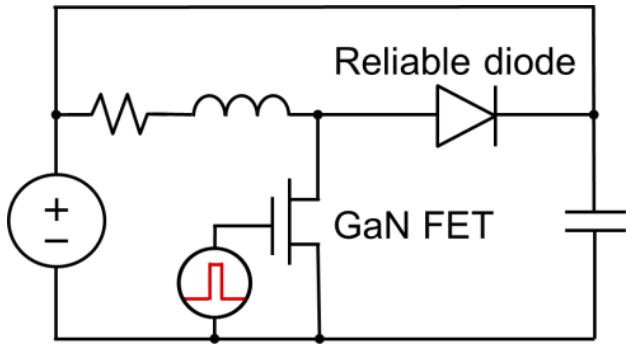
Stable dynamic Rds-on with aging at high-voltage, high-current, high-temperature, hard-switching

(1) J. Bocker et. al, "*Ron Increase in GaN HEMTs – Temperature or Trapping Effects*", IEEE Energy Conversion Congress and Exposition (ECCE), p. 1975, 2017.

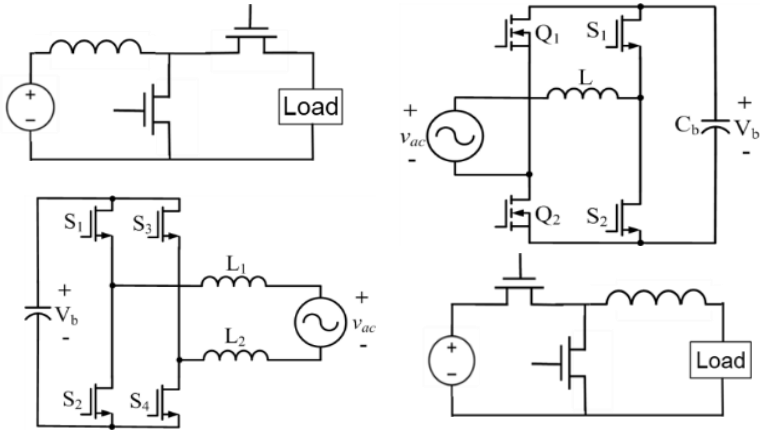
Challenges in determining switching lifetime

- The complexity of the switching transition
- The dependence of the stress rate on the application
- The lack of a broad modeling approach

Stress using a test-vehicle circuit suitable for accelerated stress



Evaluate switching lifetime for broad application use



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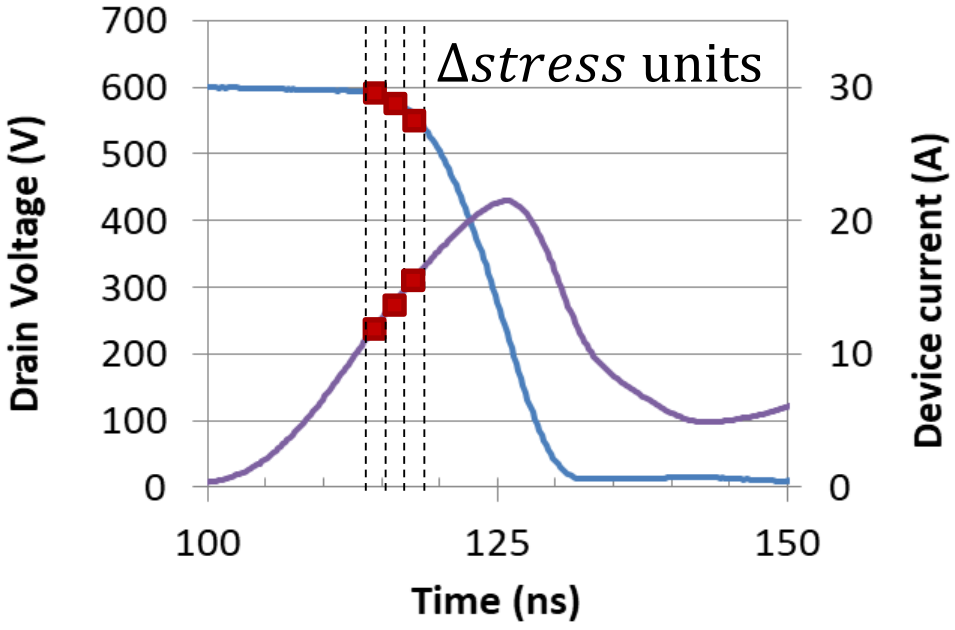
Calculating switching stress

- Prior-art uses fixed parametric values, e.g. V_bus, peak current, etc.
- We integrate the switching waveform with wearout acceleration factors to calculate the switching stress
- Integration captures the complexity of the switching waveform



$$\Delta \boldsymbol{Stress} = \boldsymbol{v_{DS}} \times \boldsymbol{AF^V} \times \boldsymbol{i_{Device}} \times \boldsymbol{AF^I} \times \Delta \boldsymbol{time}$$

(AF=Acceleration Factor)

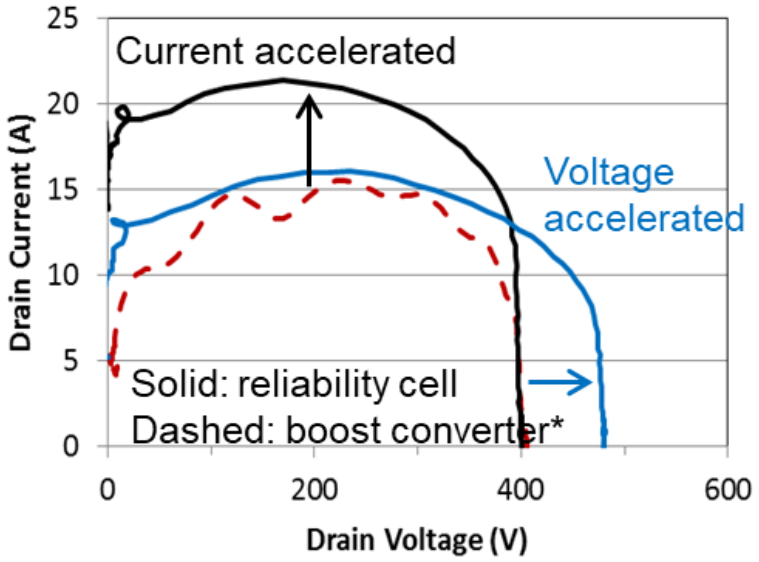
$$Stress[1] = \sum_{t\,(start)}^{t\,(end)} \Delta Stress(t)$$

[1] Builds upon Ikoshi et. al, IRPS 2018, 4E.2-1 that wearout from switching stress is cumulative

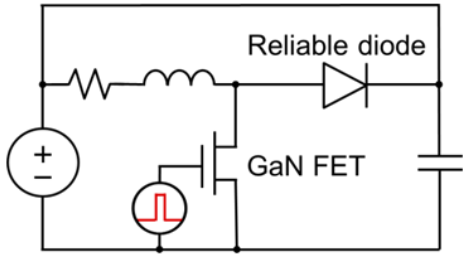
"*A Generalized Approach to Determine the Switching Lifetime of a GaN FET*", IEEE IRPS 2020, available at www.ti.com/lit/ml/slyy196/slyy196.pdf

Hot carrier wearout: switching lifetime model

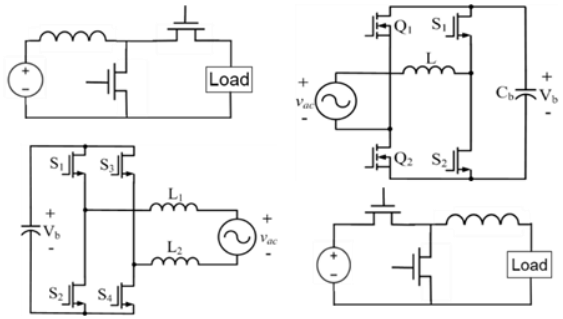
- Hard switching generates hot carriers, which can cause wearout
- TI tests for hot carrier wearout by using accelerated hard-switching



Stress using a test-vehicle circuit suitable for accelerated stress



Evaluate switching lifetime for broad application use



Construct switching stress model

Voltage acceleration

- **Exponential model (TDDB):** $TTF \propto e^{-\beta_V(V_{DS})}$ — β_V=0.109

Current acceleration

- **Exponential model:** $TTF \propto e^{-\beta_C(I_{Ch})}$ — β_C=0.283
- **Power-law model:** $TTF \propto (I_{Ch})^{-n}$ — n=3.1

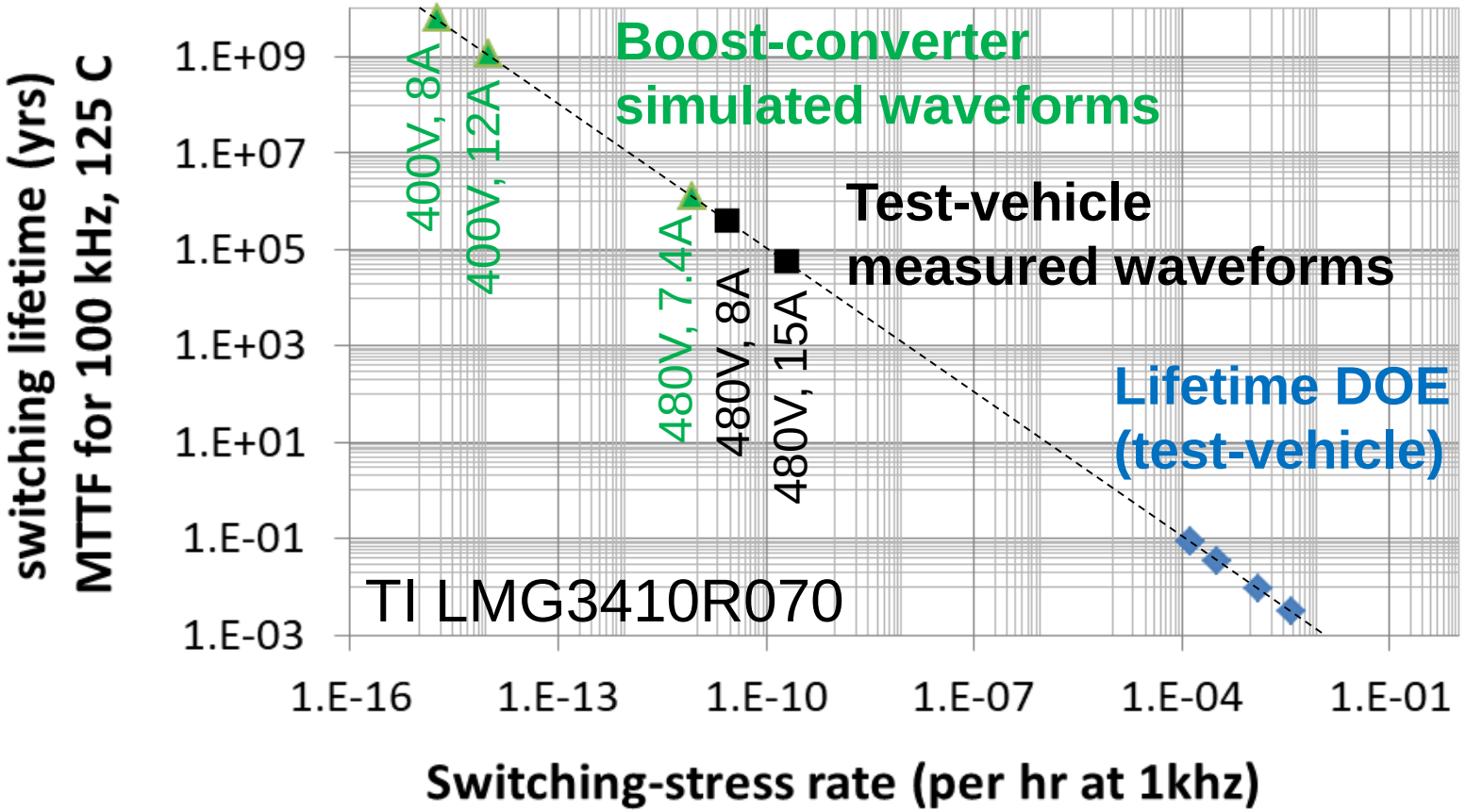
(electromigration, hot-carrier)

Temperature acceleration

- **Arrhenius model:** $TTF \propto e^{\frac{Ea}{k}[\frac{1}{T}-\frac{1}{To}]}$ — E_a=0.7 eV

"*A Generalized Approach to Determine the Switching Lifetime of a GaN FET*", IEEE IRPS 2020, available at www.ti.com/lit/ml/slyy196/slyy196.pdf

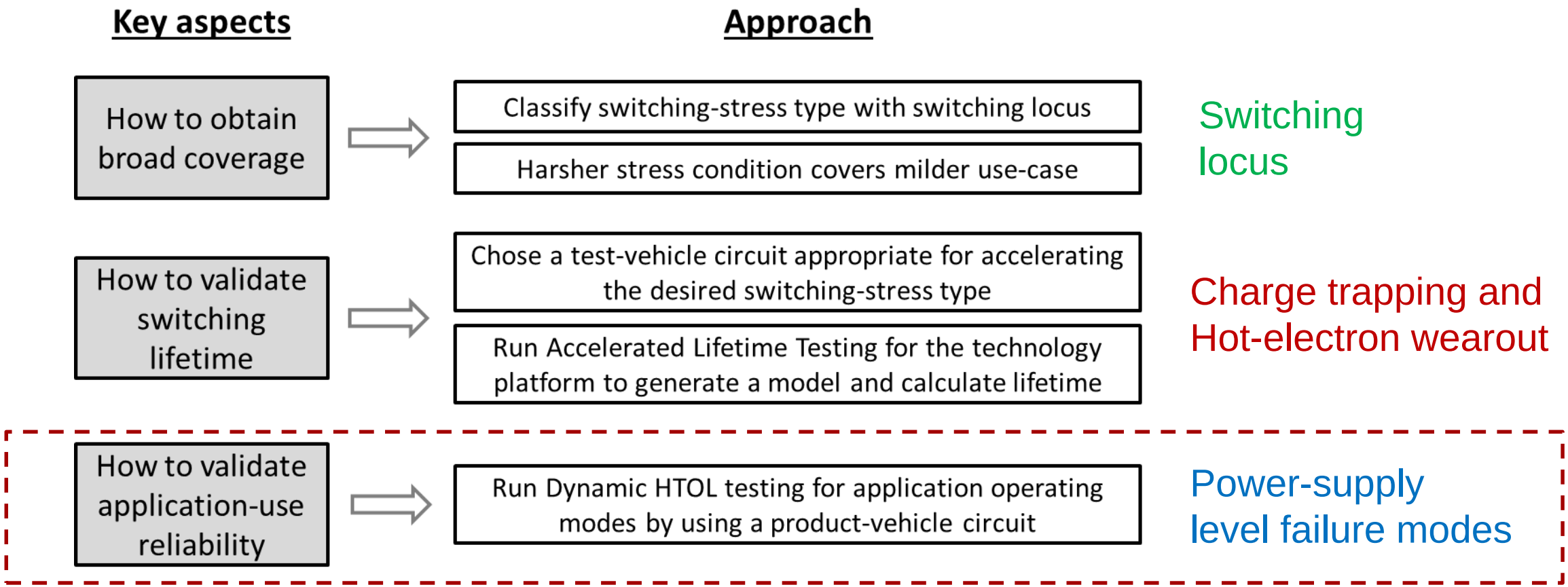
Lifetime extrapolations: hard switching



- Exponential model was used (was more conservative – lower lifetime)
- Over 1 billion years switching lifetime for 400 V, 8 A hard-switching at 100 kHz
- *Hot carrier wearout is not an issue!*

Validating switching reliability: JEP180

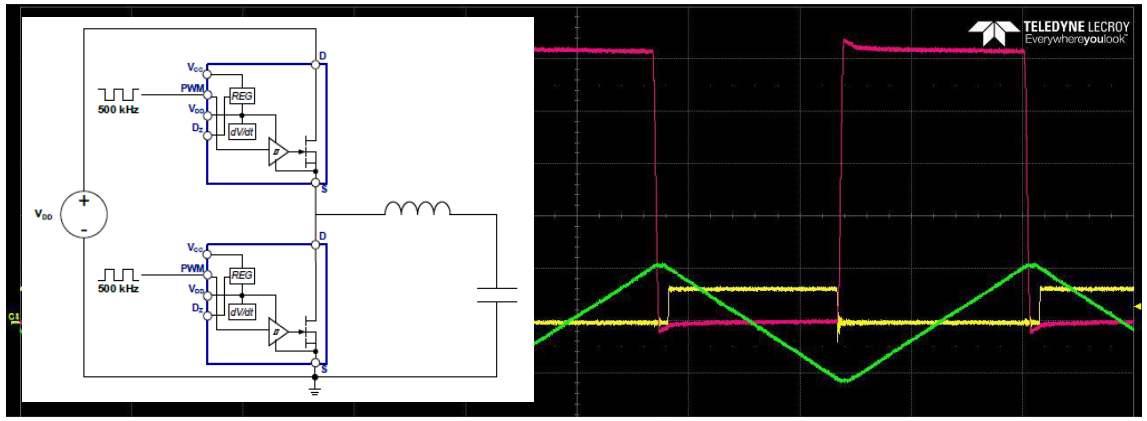
- Traditional qualification does not consider the switching stress of power supplies
- JEP180 assures that GaN parts will operate reliably in the intended application



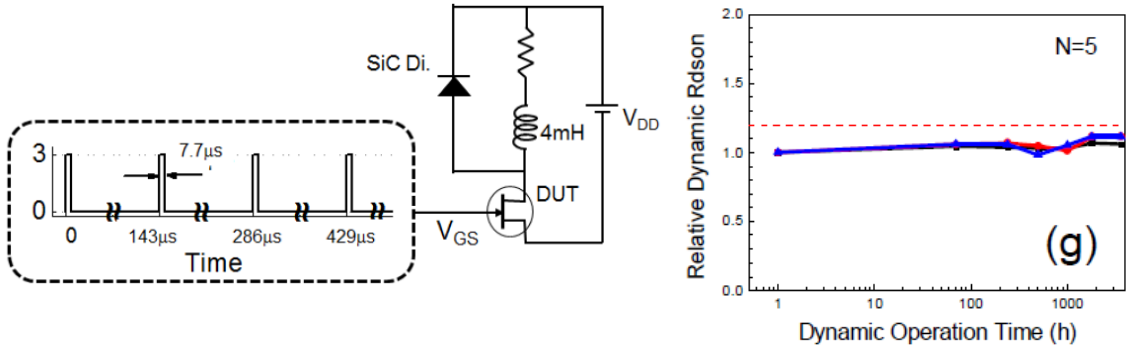
Source: Fig. 1, JEDEC JEP180

Literature summary on DHTOL

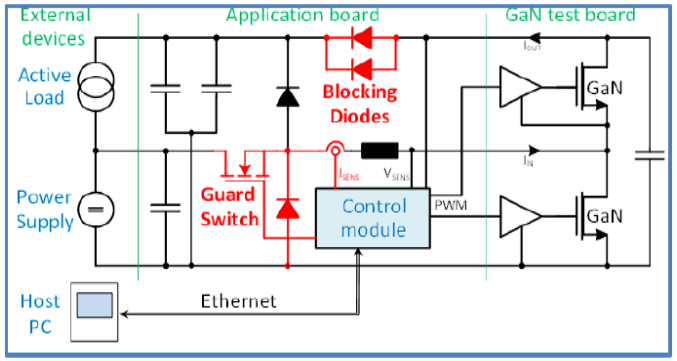
600 V – 650V FETs

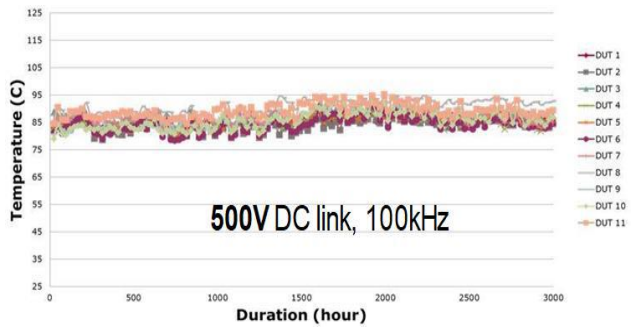


D. Gandhi (Navitas), "*Systematic Approach to GaN Power IC Reliability*", APEC PSMA Industry session IS11, 2019

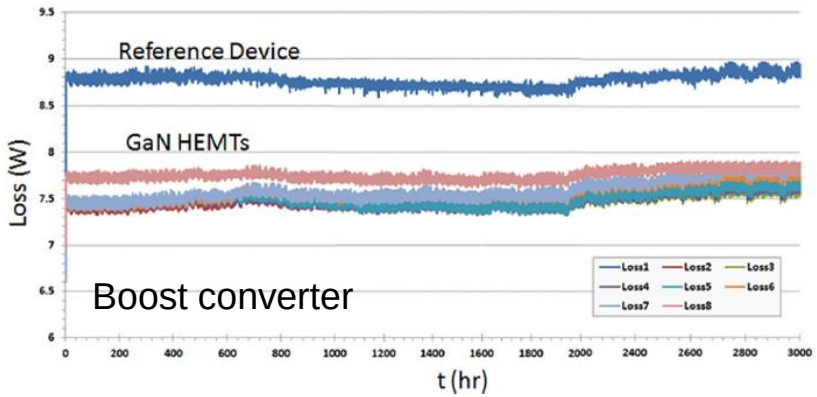


A. Ikoshi et al. (Panasonic), "*DHTOL Life Tests for GaN Hybrid-Drain GITs*", APEC Industry Session IS16-02, 2018





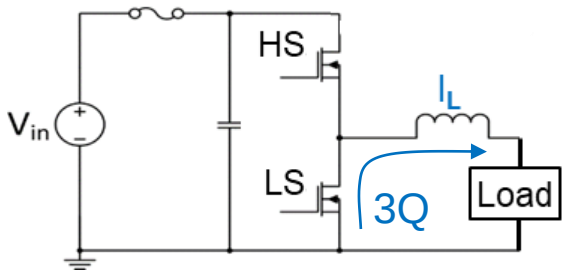
T. McDonald, "*Reliability and qualification of CoolGaN*", Infineon whitepaper



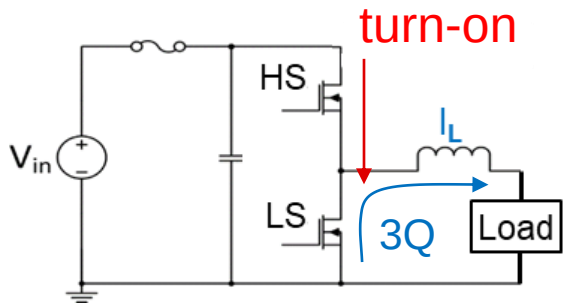
K. Smith, et al., (Transphorm) "*Lifetime tests of 600-V GaN-on-Si power switches and HEMTs*", Microelectronics Reliability, p.197, 2016

TI DHTOL summary: following slides

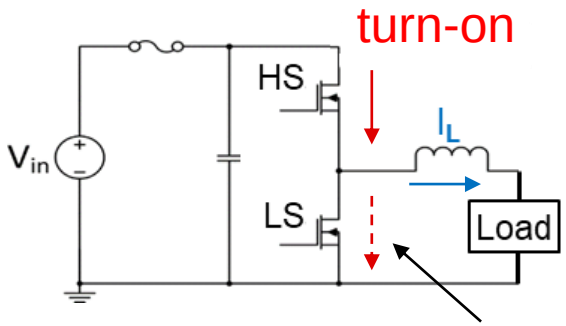
Power-supply level stresses



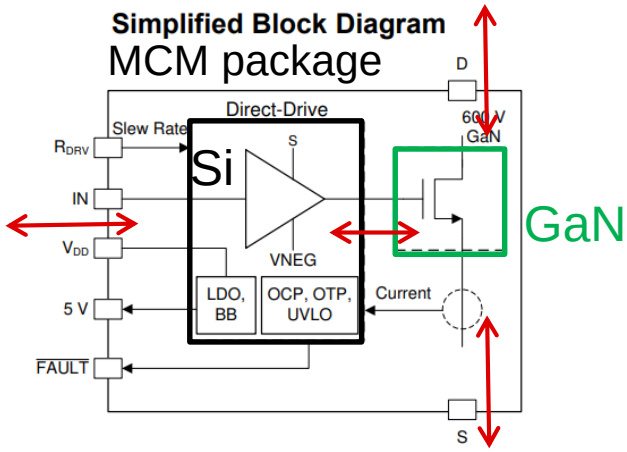
Third quadrant



Hard-commutation (reverse recovery)



Miller turn-on shoot-through



GaN device interaction with driver (and other system components)

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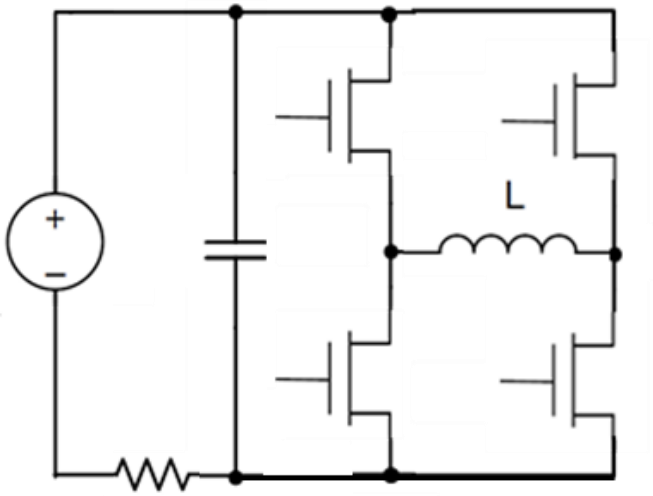
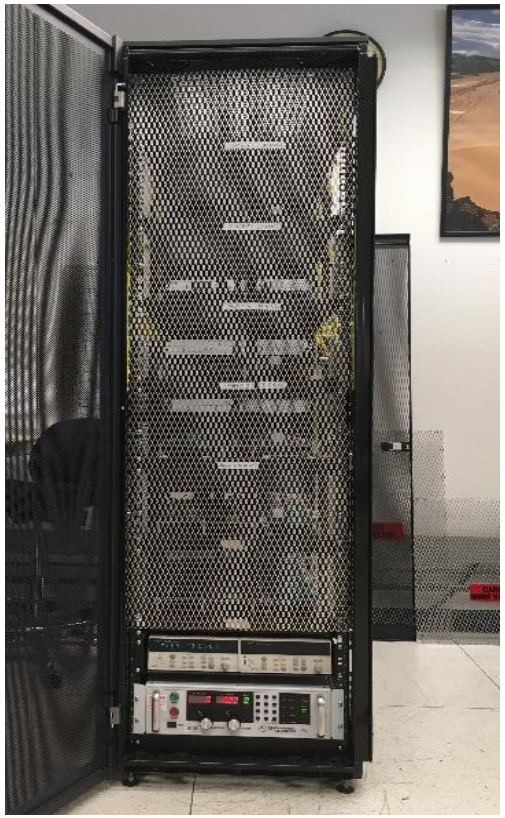
Reliable power-supply operation: DHTOL testing



Loss current sensing

<u>H-bridge circuit</u>

- Recycle power
- Both hard and soft-switching stress at high power
- In-system stress modes



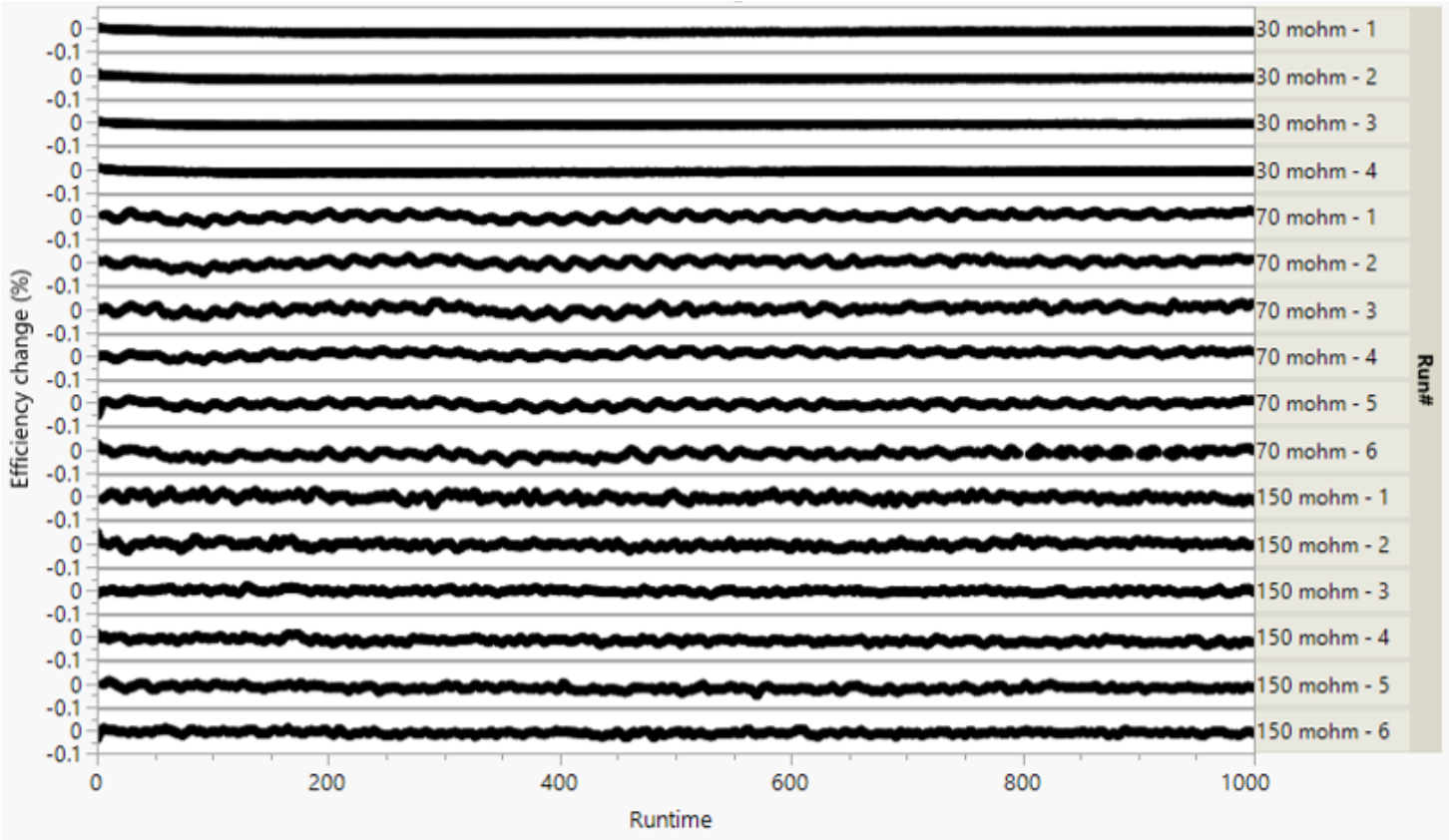
Stress rack

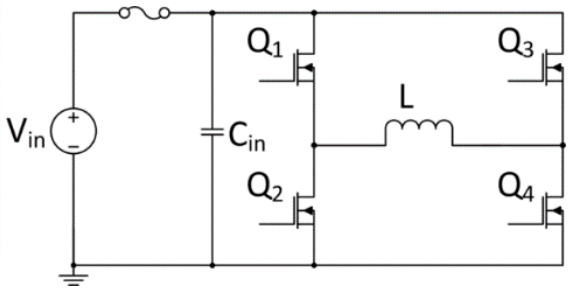
Application half-bridge boards under stress

Texas Instruments

Validating in-system reliability (DHTOL, JEP180)

LMG34xx TI GaN half-bridges run at 480V/125C, 150 kHz, 100 V/ns slew rate and maximum-power hard-switching stress conditions for 1000h.





Rds-on (mohm)	Power (kW)	no. of half-bridges	no. of parts
30	3.8	8	16
50	1.9	12	24
150	1.4	12	24

64 parts ran from multiple lots of the LMG34xx product family

*Reliable in-system operation for **both hard and soft switching**: stable running with efficiency within 0.1%*

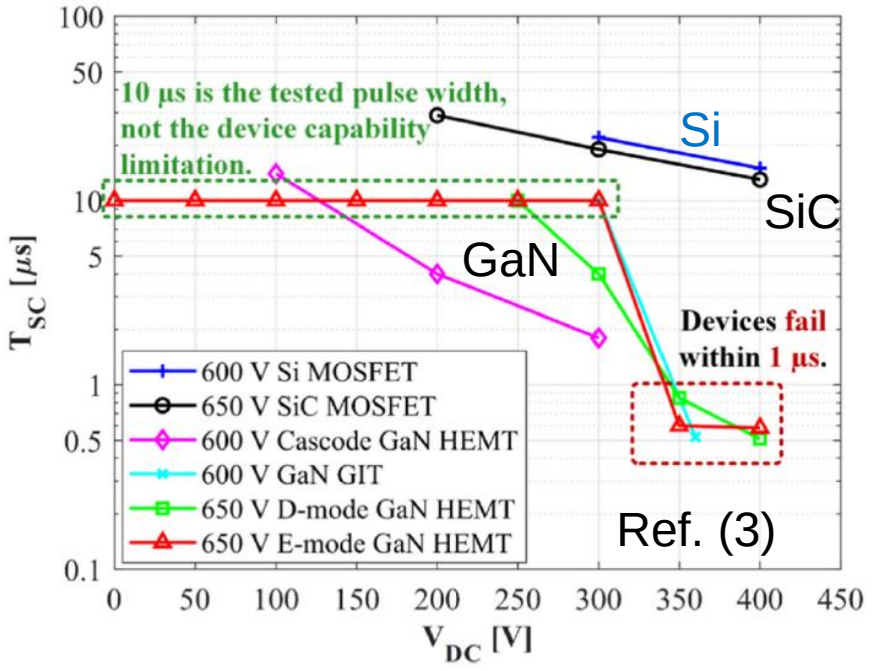
Reliable operation under all conditions

During operation, abnormal or extreme conditions can occur

- The load can short circuit
  - Overcurrent protection would turn the FET off in a latched or cycle-by-cycle manner
- A line surge can occur from an event like a lightning strike
  - The power FET needs to be surge robust
- The supply voltage may dip
  - If the supply voltages go below a threshold, UVLO protection would pause power FET switching until the voltage recovers.
- The die temperature may get too high, such as if there is a cooling issue
  - If the die temperature exceeds the threshold, overtemperature protection turns the power FET off and notifies the system.

Short-circuit robustness

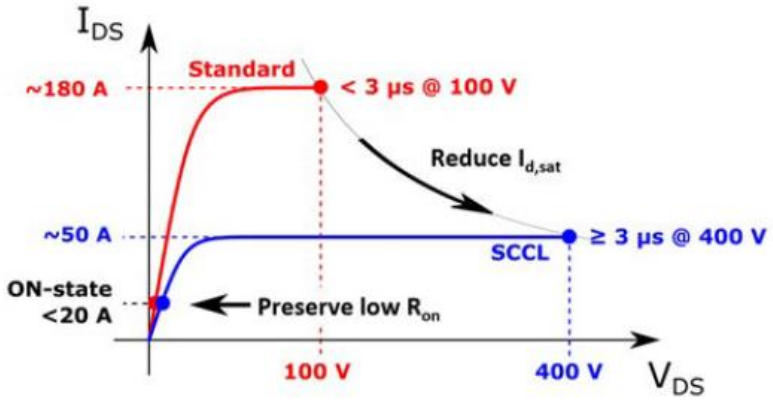
- A 10-μs withstand time was traditionally required for an external hardware protector to sense the short circuit and turn off the power device(1). Driver ICs are faster now, with response times of less than 0.5 μs(2)
- A GaN HEMT has a smaller active volume and higher saturation current than an IGBT, so heats up faster during short circuit. For a 400 V hard short circuit, the fail time could be less than 1 μs(3)
- There are two broad approaches being followed:
  - Reduce Idsat or Id, which increases the short-circuit withstand time
  - Turn off the power FET earlier



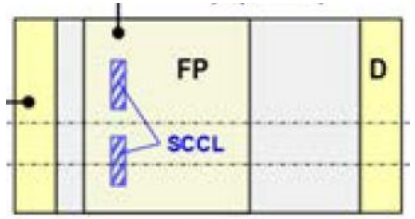
(1) "*Robustness in Short-Circuit Mode: Benchmarking of 600V GaN HEMTs with Power Si and SiC MOSFETs*", Badawi et. al, ECCE 2016
(2) e.g.TI UCC21750 at https://www.ti.com/product/UCC21750
(3) "*A Reliable Ultrafast Short-Circuit Protection Method for E-Mode GaN HEMT*", Lyu et. al, IEEE Trans. Power Elec. 2020

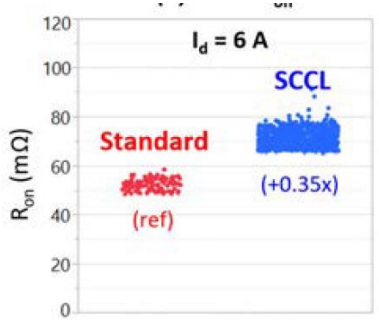
Reduced drain current increases SC withstand time

(a) $I_{D(SAT)}$ reduction by process change



Remove segments of 2DEG near source. (some increase in Rds-on)

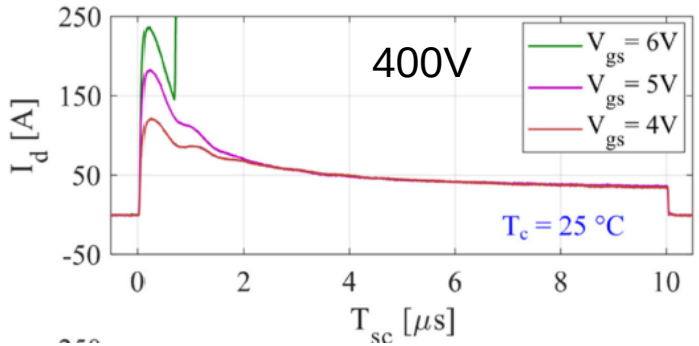


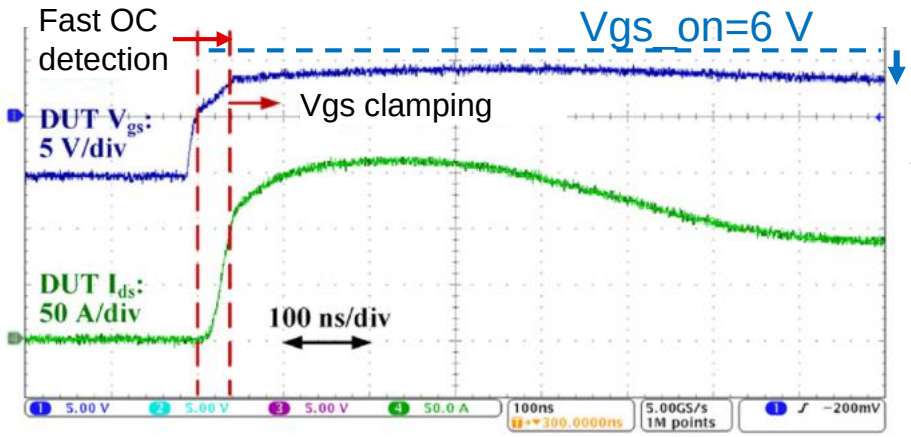


"*Short-Circuit Capability Demonstrated for GaN Power Switches*", D. Bisi et al., APEC 2021

(b) I_D reduction by lowering gate-source voltage

Lower Vgs increases short-circuit (SC) withstand time

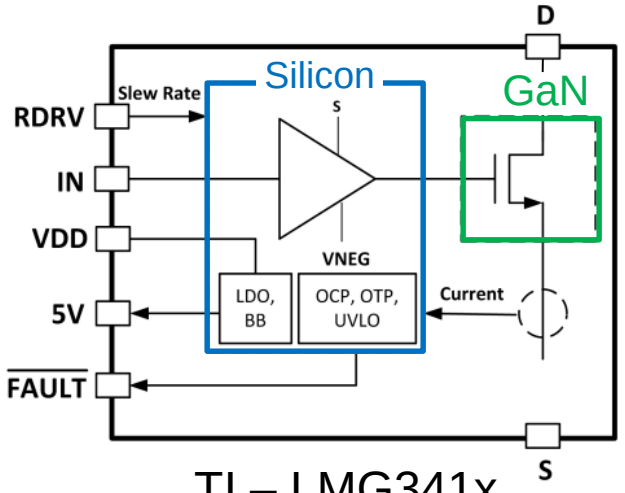




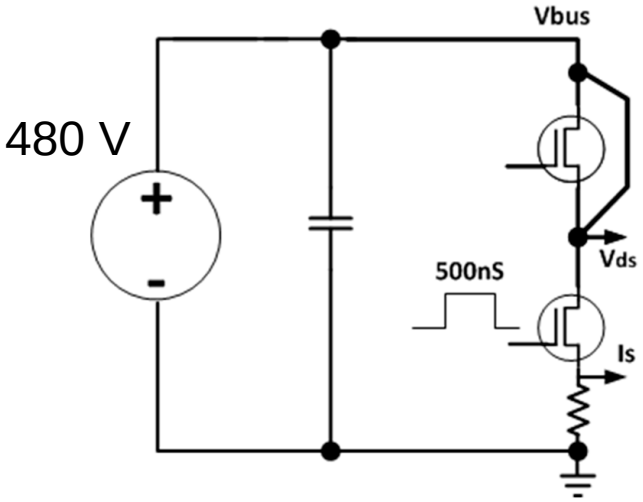
Quickly reduce Vgs and gain more time to allow regular gate-driver turn-off

"*A Reliable Ultrafast Short-Circuit Protection Method for E-Mode GaN HEMT*", Lyu et al, IEEE Trans. Power Elec. 2020

Integration allows to turn off the FET earlier

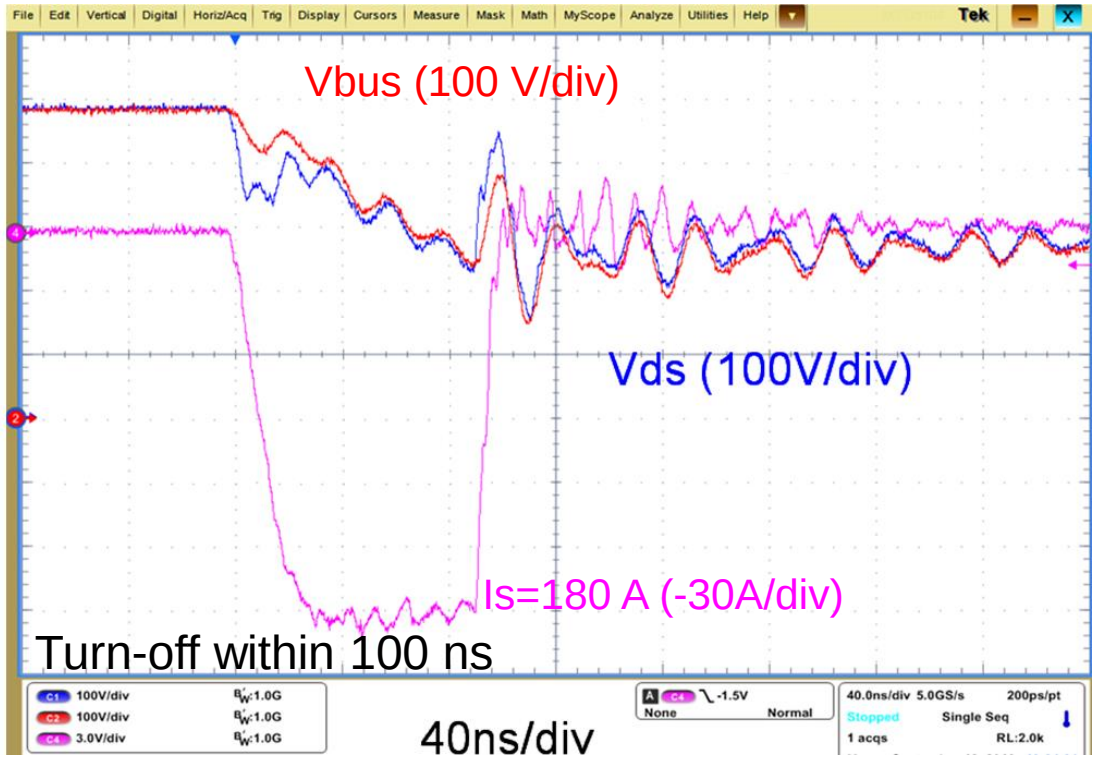


TI – LMG341x



Hard short-circuit test

- Integration of GaN power FET in a low-inductance package with a Si driver and protection allows fast detection and turn-off.
- Built-in protection eliminates delay needed for external components.



(1) "*Overcurrent Protection in High-Density GaN Power Designs*", TI Application Report, www.ti.com/lit/an/snoaa15/snoaa15.pdf

Texas Instruments

Surge robustness: No avalanche? No problem!

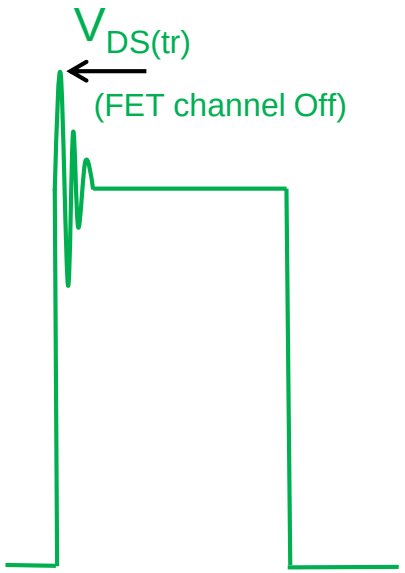
- Power line disturbances can occur due to lightning strikes, malfunction, load and capacitor bank switching, etc.
- Silicon devices use their avalanche rating property to survive these events.
- The use of avalanche is historical. It arises because silicon FETs do not have much voltage headroom above their maximum voltage rating. When a surge strikes, they break down (by impact-ionization).
- Over the years, the silicon industry has improved the ability of power FETs to survive avalanche breakdown. As a result, avalanche ability has become associated with surge protection
- GaN has good transient overvoltage capability. This allows GaN FETs to switch through surge *without avalanche breakdown* and disruption. It also improves system reliability, since MOV degradation can cause failure of Si FETs by subjecting them to higher levels of avalanche.

"*No avalanche? No problem! GaN FETs are surge robust*", available at https://e2e.ti.com/blogs_/b/powerhouse/posts/no-avalanche-no-problem-gan-fets-are-surge-robust

GaN has transient overvoltage capability

- GaN can exceed its rated voltage for short bursts
- In GaN, the voltage rating is not limited by avalanche
- GaN FET manufacturers are including a transient voltage rating in the datasheet for 600-650 V GaN FETs

Part	$V_{DS(tr)}$ Parameter	Value
GS66508B	$V_{DS(transient)}$	750 V
InnoSwitch4	$V_{MAX(NON-REPETITIVE)}$	750 V
NV6117	$V_{DS(TRAN)}$	800 V
TPH3212PS	$V_{DSS(TR)}$	800 V
IGT60R070D1	$V_{DS,pulse}$	800 V
LMG3410R050	$V_{DS(TR)}$	800 V

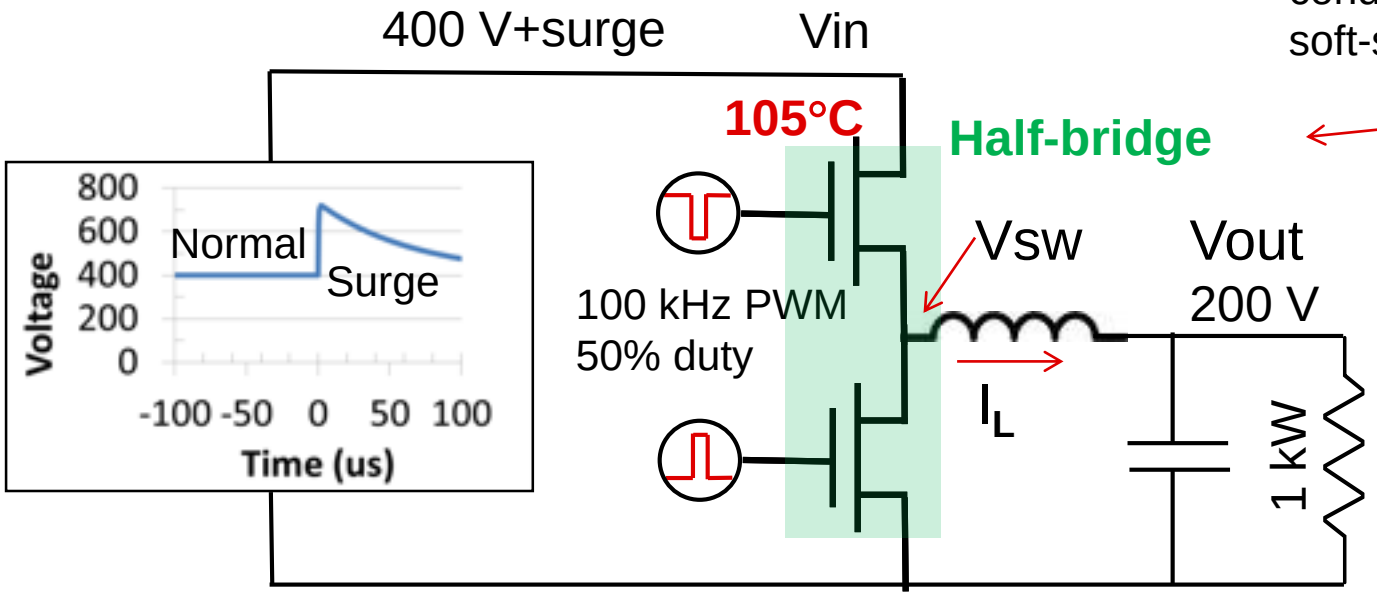


- The $V_{DS(tr)}$ rating is being used for ringing of flyback converters(1).
- Hard-switching circuits need different validation since the channel turns on multiple times during the surge strike and subjects the FET to hot-carrier stress.

(1) "Surge-robust flyback power supplies with GaN", K. Varadarajan et. al., APEC 2020

TI's active-power surge test

- Device: TI LMG3410R070
- Load: 1 kW
- Hard switching at 100kHz
- 105°C device case temperature.
- 720V surge peak at the device terminals



LMG3410 Half-bridge EVM card

High-side (hard-switched)

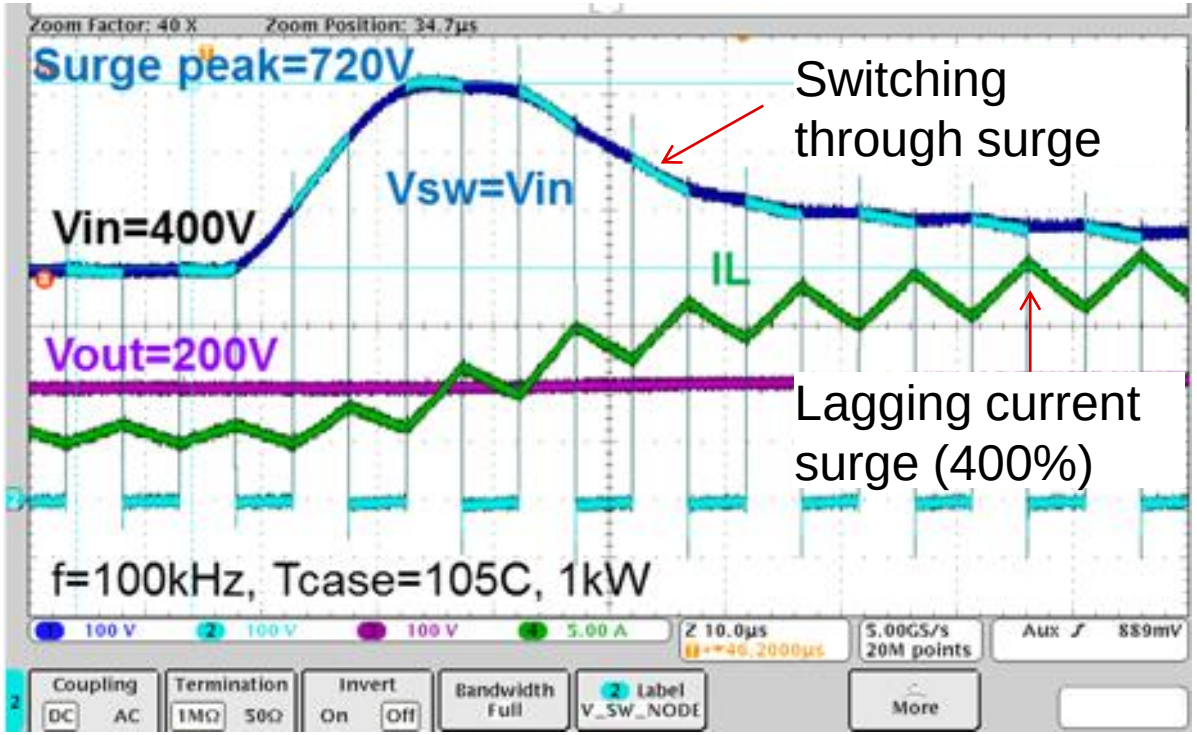
Low-side (reverse conduction and soft-switched)

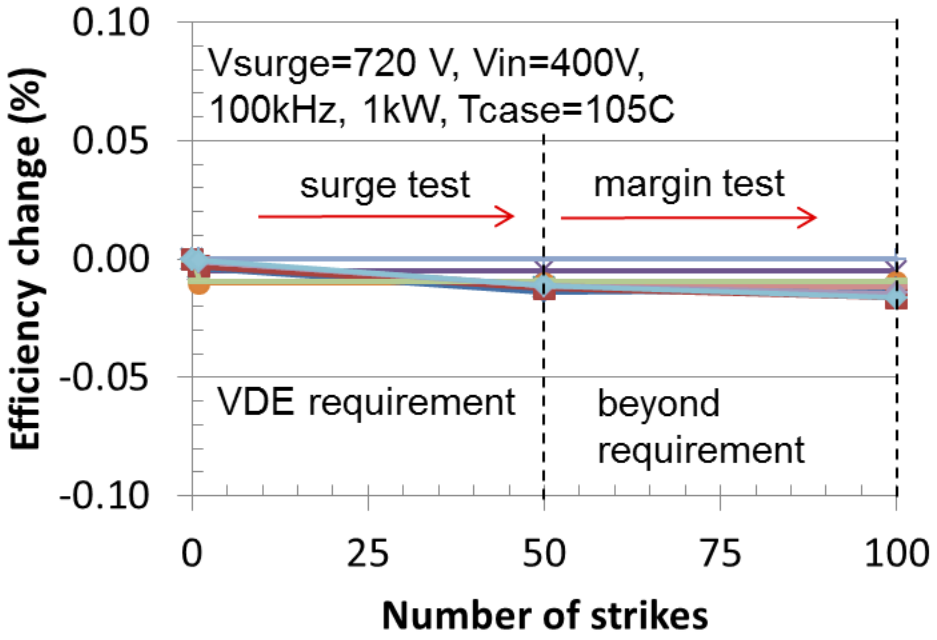
Devices tested under:

- Hard-switching
- Soft-switching
- Third quadrant
- Hard commutation

TI GaN: Robust to surge

- The IEC 61000-4-5 standard specifies the surge waveform
- The VDE 0884-11 standard specifies the application of 50 strikes
- We applied additional 50 strikes to assure margin
- Parts had very stable efficiency and there was no hard failure

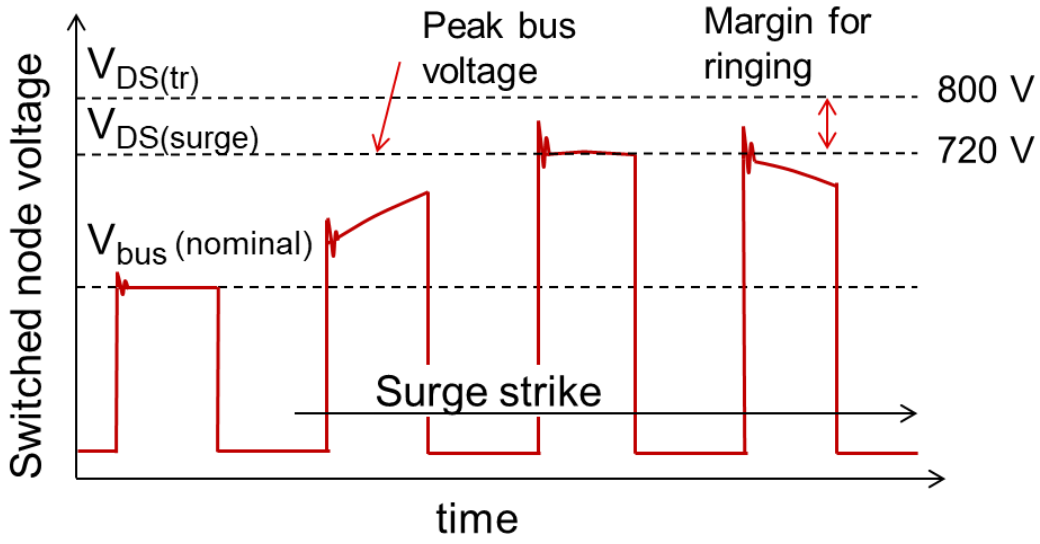




"A New Approach to Validate GaN FET Reliability to Power-line Surges Under Use-conditions",IEEE IRPS 2019, available at www.ti.com/lit/ml/slyy162/slyy162.pdf

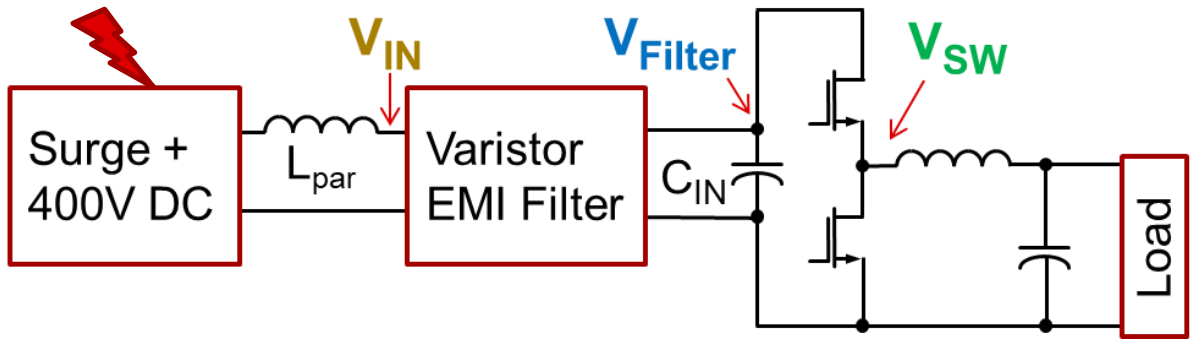
Surge-robust design with GaN

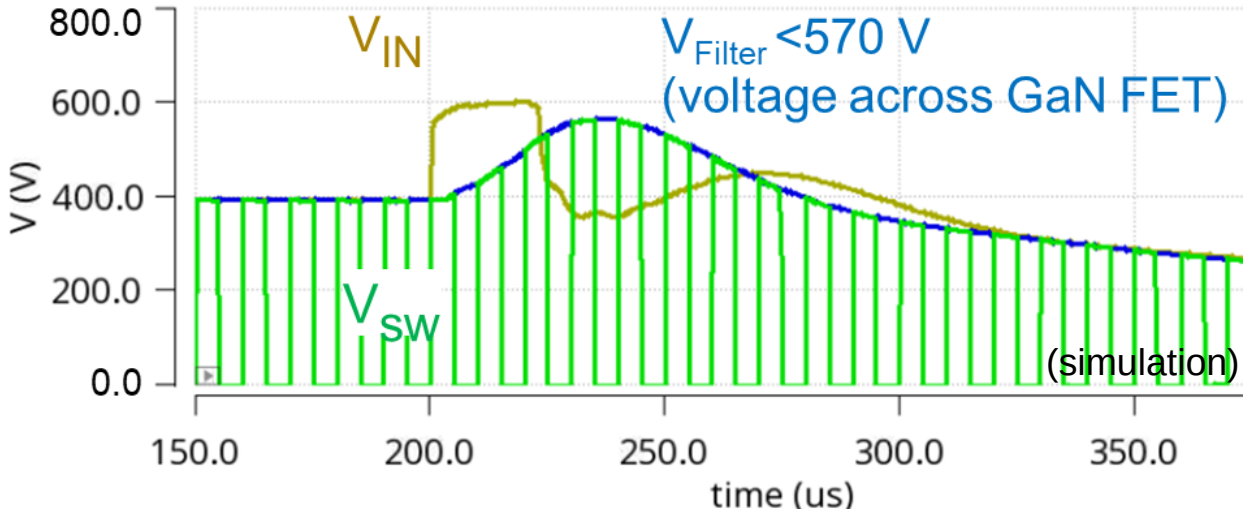
Due to different stresses, there are two transient overvoltage ratings: $V_{DS(tr)}$ for FET off, and $V_{DS(surge)}$ for hard turn-on.



For surge-robust design, select components to keep bus voltage at device below these ratings.

L_{par}=0.5 µH, Cin=47 µF
420 V varistor





- Bus voltage at device < 570 V with 4 kV surge strike
- It is straightforward to limit the voltage, even for severe surge conditions, with margin

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Conclusion

- All devices have failure mechanisms which need to be understood, and be engineered for reliable operation
- For GaN, key mechanisms are TDB, charge trapping and hot-carrier wearout
- Traditional qualification does not consider switching stress of power supplies
- The GaN industry developed the JEDEC JEP 180 guideline to assure that GaN power FETs will operate reliably in the intended application
- JEP180 guides on how to validate reliability for the intended application. TI and other GaN suppliers are now conducting the types of validation recommended and showing that GaN FETs are reliable for application use.
- GaN FETs are also reliable under abnormal or extreme conditions of short circuit and surge.

GaN FETs are reliable and ready to use