The Ohio State University

THE OHIO STATE UNIVERSITY

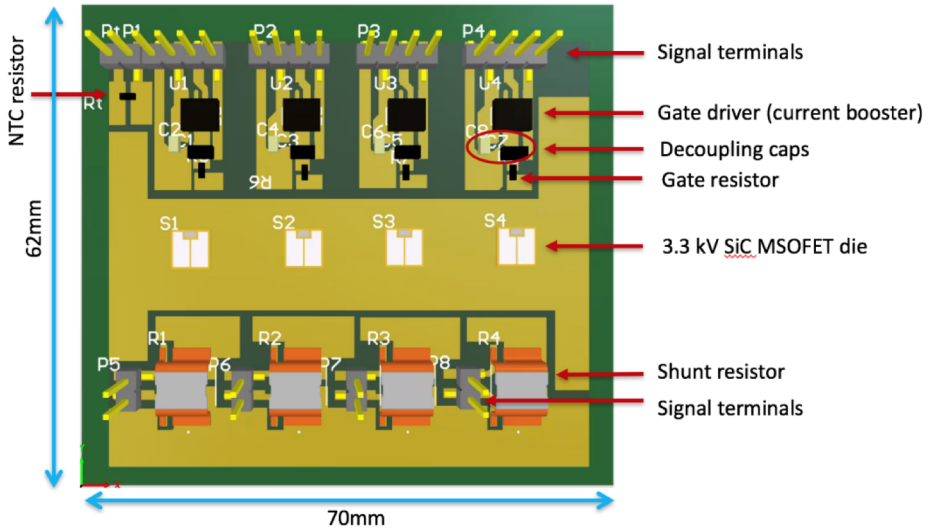
Membership Level: Academic Member

Project Title: Artificial Intelligence-Based Current Sharing for Parallel Operation of 3.3 kV Silicon-carbide MOSFET Chips in Power Module

Objectives: achieve even current sharing of parallel chips on the next generation wide-band gap (WBG) power electronics devices. 3.3-kV SiC bare dies are used to design and build power modules.

Task No. BP5-3.19 (OIF)

PI: Zhang, Email: zhang.564@osu.edu, Phone: 614-619-2889



Power module design to integrate current, temperature sensing to achieve even current sharing for individual chips.

WBG Technology Impact

1. Integrate gate driver and current sensors into power modules to enable even current sharing for parallel chips.
2. Application: if successful, the power modules can be used on EV chargers, motor drives, PV inverters, UPS, Data Center,
3. Will reach out multiple device manufacturers once the power modules are built and tested and discuss the commercialization plan.
4. Current power modules do not have even current sharing between parallel chips. Therefore, parallel chips will experience uneven thermal stress. Overtime, this may reduce the reliability and lifetime of the power module. If successful, this project will help improve power module reliability and lifetime by at least 10%.

Accomplishments/Outcomes

- Chip-level measurement methods
- SiC power modules that integrate gate drivers and current measurement for individual parallel chips
- Active current balance schemes for parallel chips in SiC MOSFET power modules