Final Report

September 2021

DOE Cooperative Agreement DE-EE0006521

North Carolina State University

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Executive Summary

PowerAmerica: The Next Generation Power Electronics Manufacturing Innovation Institute has been established and is making significant progress in furthering the program goals of accelerating the adoption wide bandgap semiconductors into power electronics technologies, to spark early commercialization of compact, robust, energy efficient products, and to nurture the U.S. wide bandgap semiconductor industry by developing a capable workforce though education programs and training. The PowerAmerica consortium, led by NC State University, is accomplishing this through a cooperative agreement with the U.S. Department of Energy (DOE) Office of Energy Efficiency and Renewable Energy's Advanced Manufacturing Office. This private public partnership with EERE includes member companies ranging from startups, small-medium enterprises, to large system integrators, world class universities and community colleges, K-12 educational institutions, trade associations, state and federal government agencies, and economic development organizations. The wide bandgap power electronic ecosystem formed by this diverse set of Institute members is focused on using advanced manufacturing to 1) lower the cost of silicon carbide and gallium nitride devices to be comparable to silicon devices, 2) demonstrate the size, weight and energy efficiency advantages of wide bandgap semiconductor power electronics through world class demonstrations of capability that translate into new products for US industry that create jobs and 3) building an education pipeline for a skilled workforce to meet the future demand for emerging wide bandgap semiconductor power electronic markets to enhance US economic competitiveness globally.

The first year has laid the groundwork for a successful sustainable program that is driven by industry's needs. Infrastructure has been established to ensure industry proprietary information is securely protected, while channels for dialog and communication across the supply chain are enhanced. Formulation of an open source process model for wide bandgap semiconductors, (similar to open source software licensing) is being investigated as a mechanism for industry to mutually invest in wide bandgap semiconductors while maintaining the appropriate control of proprietary information. Strong relationships between university faculty and industry members is leading to technology partnerships that enhance movement up the Technology and Manufacturing Readiness Level scales, that will lead to new product introduction and technology transition.

Under the leadership of Executive Director Nickolas Justice and Deputy Director Dr. John Muth, the PowerAmerica staff and the industry and university partners continue to focus on US competitiveness, guided by the industry voice to shape a wide bandgap power electronic roadmap for the future. In addition to the open source fabrication of wide bandgap semiconductor devices and projects targeted at specific technology achievements, the sustainability initiatives include a new teaching-manufacturing laboratory that cross-cuts Electrical, Mechanical and Industrial Engineering disciplines and has engagement with the College of Management and the School of Design. This new facility represents a significant NC State commitment to the sustainability of the

Institute. The focus on design for manufacture (DFM), design for reliability (DFR) and power electronics assembly will provide a unique capability to engage small-medium enterprises and entrepreneurs in the low and medium volume manufacture of advanced power electronic systems. This serves as a platform to disseminate best design practices and reduce the dependence on contract manufacturing overseas. Similarly, a device "bank" concept is being investigated that will improve the availability and reduce the cost and lead-time of high performance wide bandgap devices. This will allow universities and companies to more easily innovate and build prototypes for demonstration and new product introduction, reducing the time to market and accelerating commercialization.

PowerAmerica is devoted to accelerating the adoption of smaller, lighter, more efficient systems enabled by wide bandgap semiconductors leading to low cost, clean, renewable energy systems, longer-range more efficient transportation, industry and consumer energy savings, smarter electric grids and a better quality of life. As we move into Budget Period 2 and beyond, we look forward to continuing our work with existing members and expanding opportunities with new members to improve US competitiveness in wide bandgap power electronics and building a well-trained, skilled workforce to capitalize on this opportunity.

PowerAmerica Budget Period 1 (2015-2016)
Highlights

Focus Area 1: Operations and Management: In the first year, 22 projects were initiated that extend across the supply chain, building US capability in: the fabrication of wide bandgap powers devices; packaging those devices to maximize their electrical and thermal performance; and incorporating those devices into advanced system demonstrations that have strong commercialization potential. Over the course of the year, four high potential, Open Innovation Fund projects complementing the initial projects were also selected, increasing the diversity and capability of the Institute. In response to the Institute's call for proposals, 93 concept papers were received which resulted in 52 full proposal submissions for budget period two. It is anticipated that after rigorous peer reviews, approximately 30-35 new projects will be awarded that will further advance the Institute's goals.

Focus Area 2: Foundry and Device Development: The nation's first six-inch diameter silicon carbide foundry using an open foundry model was established. Four Institute members committed to develop power electronic devices in this facility. This leverages existing silicon foundry capacity that was underutilized and creates a new business model for US industry to fabricate wide bandgap power electronic devices at lower cost.

Institute member projects also demonstrated and qualified advanced power modules and devices that will impact transportation, aerospace, renewable energy sectors and the power grid, that are of higher performance than silicon. These devices are being evaluated by end-users who desire to build smaller, lighter and more efficient systems than the current generation systems that rely on silicon devices.

Focus Area 3: Power Module Development and Manufacturing: A member company released two new power module products that have lower inductance and capacitance and better thermal properties that allow wide band gap semiconductors power devices to operate closer to their theoretical limits. This company was also acquired by another Institute member.

Focus Area 4: Accelerating Power Electronic Application Commercialization
Power electronic application demonstrations include design and assembly of:

- A 50 KW fast charger for electric vehicles that is 10 times smaller than the state of the art.
- Robust, compact inverters for photovoltaic and electric vehicle applications.
- High frequency, high power density power supplies that have the potential to significantly reduce the power consumption of data centers.

Focus Area 5: Education and Workforce Development: PowerAmerica successfully developed a wide bandgap power electronics concentration and curriculum within NC State University's Professional Science Master Degree program. PowerAmerica has also interacted with hundreds of students and teachers by engaging with community college

instructors, High School teachers, the NSF Advanced Technology Education program, the NIST Manufacturing Extension Partnership, and industry associations such as the Research Triangle Clean Tech Cluster to build a pipeline for a skilled workforce in the area of wide bandgap power electronics.

Operations and Management

Focus Area 1: In its first year of existence, PowerAmerica is fully operational and has made, and is continuing to make significant strides toward meeting the 5 year goals and objectives of the Institute:

1. Form a self-sustaining Institute with an operating budget of $4,000,000 per year in non-federal funds. Partner with industry, academic, and government stakeholders to promote the adoption and manufacturing of WBG semiconductors in power electronics.

2. Reduce the cost and scale-up the production of WBG semiconductor power devices and modules through innovative foundry models and innovations in manufacturing that result in 10,000 WBG wafers per year developed by Members within 5 years.

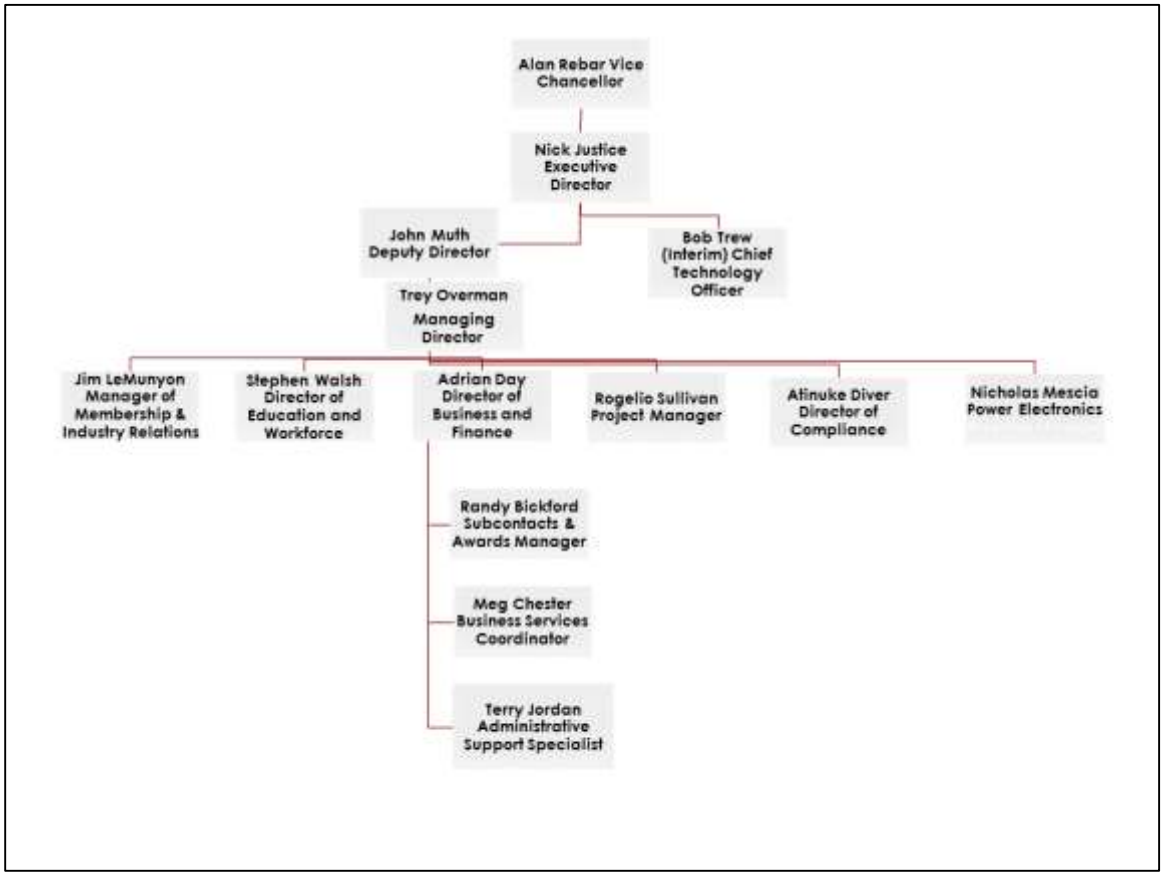
3. Have Members of the Institute perform targeted applied research and focused commercialization projects. Conduct evaluations of WBG device reliability and system level performance advantages that will de-risk industry WBG product development cycles and decrease the time to WBG-enabled products, leading to commercialization of 10 WBG PE technologies within 5 years.

4. Develop an educated workforce that will have the capability to innovate new WBG-enabled products to meet the future demands of WBG manufacturing, including at least 500 workers with certified skills aligned with industrial Member needs within 5 years.

In order to facilitate these goals, PowerAmerica established its headquarters on Centennial Campus at NC State University. Located at 930 Main Campus Drive, Raleigh NC is the 9,000 square foot headquarters facility that serves two distinct purposes: Administrative space occupies approximately 4,000 square feet, which houses all management offices as well as workstations, and collaboration stations, and the remaining 5,000 square feet is primarily utilized for Education and Workforce development activities. PowerAmerica members and the larger NC State community have access to break out rooms, large conference rooms, individual workstations and communal areas to gather, learn and teach. PowerAmerica is also undertaking the establishment of a Teaching Manufacturing Line within the Varsity Research Building, also on Centennial Campus, that will provide an additional 7,000 square feet of space that will not only house the associated equipment, but will also provide a space for contract fee-for-service testing and reliability efforts and research laboratory space with the capability to perform export controlled and ITAR work in a secure environment.

Leadership and Organization: Driving the direction of the Institute, under the leadership of MG Justice and Dr. Muth, are the development and adherence to the Operations Plan, Communications Plan, and Marketing & Branding Plan, all of which have been completed and approved by the Executive Committee. These plans define the methods by which the Institute will recruit new members, plan and conduct the yearly

Call for Projects, manage the activities of the Institute internally, and establish, manage and terminate existing and new projects. Further, these guidelines shape how the Institute engages with its constituencies, including disseminating information to the membership and committees, communicating the vision of the leadership and the Institute to employees and stakeholders, and ensuring how all of the vital roles within the organization will collectively contribute to the success and sustainability of the Institute. Of critical importance to the viability of the Institute, PowerAmerica has developed the necessary processes and procedures for maintaining the integrity of proprietary information, ensuring compliance with all applicable laws and best practices, as well as ensuring export compliance for technology developed under the cooperative agreement.



PowerAmerica Organization

PowerAmerica staffing is virtually complete. Eleven out of twelve key personnel have been appointed, including MG Nickolas Justice as the Executive Director and Dr. John Muth as the Deputy Director. A search for the remaining position of a Chief Technology Office is in process with 20 applicants being considered. The key personnel of PowerAmerica are as follows:

Position	Name	Major Duties
Executive Director	Nick Justice	Provide visionary leadership, strategic direction, set policy and standards, sustainability planning, network with Government and industry peers
Deputy Director	John Muth	Implement Vision, and execute mission. Day to day operations & management, supervise staff, strategic planning, Focus on Sustainability. Liaison with DOE & other Gov., coordinate advisory boards
Chief Technology Officer	TBD	Provide technical expertise in Institute activities, assess technology and market trends and position Institute for success; lead road mapping
Director of Membership and Industry Relations	Jim LeMunyon	Recruit and service industry members, create the value proposition, promote Institute broadly, support Industry Advisory Group
Director of Education and Workforce	Stephen Walsh	Lead and execute education plan, coordinate member education services, liaison with ATE/MEP, recruit students, plan & execute training program
Project Manager	Rogelio Sullivan	Generate planning documents & operating procedures, organize reviews, grant writing, report to DOE, liaison with university organizations
Director of Compliance	Tinu Diver	Provide information security, maintain membership agreement & bylaws, ITAR, EAR, export controls, IP management
Director of Finance and Business	Adrian Day	HR management, business & financial management, financial planning & reporting
Subcontracts and Awards Manager	Randy Bickford	Membership onboarding, tracking invoices and cost share, negotiating and managing subawards
Business Services Coordinator	Margaret Chester	Supports business manager, manage website and information management, documents and external communications
Administrative Support Specialist	Terry Jordan	Equipment and facility management, supplies, support staff, visitors and events
Power Electronics Assembly Manager	Nicholas Mescia	Layout proposed PCB assembly process, equipment needs, and estimate costs

In addition to internal staff at PowerAmerica, the Institute has formed and called upon the Executive Committee and Member Advisory Committee to provide guidance and oversight. Additional expertise within the university has also been called upon to supplement the core team and contribute in key areas.

Budget and Finance: Under the direction of Adrian Day, the Director of Finance and Business, a preliminary resource plan has been completed and submitted. This plan addresses staffing, equipment, facility requirements, current services as well as identifying the needs of research teams within NC State University. Within this resource plan, the PowerAmerica Institute is not only solvent, but also on a well-defined path to sustainability. In addition to the resource planning already undertaken, detailed analysis has been performed to project growth models for the Institute, labor and expense planning, identifying and evaluating new potential revenue streams and infrastructure

As identified in the preliminary resource plan, the internal budget for Budget Period 1 is as follows:

Revenue Sources	
Membership Fees	$ 1,030,000
ORIED support	$ 253,000
New Federal Projects	$ -
New Insustry Projects	$ -
DOE Funds	$ 1,677,567
Cost Share Support	
State of NC	$ 2,200,000
F&A Returns	$ 470,799
NCSU Cost Share Support	$ 2,780,148
Total Revenue	**$ 8,411,514**
Operational Expenses	
Management Staff	$ 1,469,925
Rent	$ 147,582
Marketing	$ 100,000
Travel	$ 210,000
Events	$ 50,000
Summer Activities	$ 10,000
Materials/Supplies	$ 550,000
Equipment	$ 628,765
Varsity Space Expenses	$ 538,000
Project Expenses	
Faculty	$ 795,867
Postdocs	$ 297,500
Students	$ 294,788
Equipment	$ 461,168
Materials/Supplies	$ 330,000
F&A	$ 2,053,738
Total Expenses	**$ 7,937,332**
Net	**$ 474,182**

The overall Institute budget for Budget Period 1, including sub-award projects is as follows:

CATEGORY	Budget Period 1 Costs
Institute Personnel & Travel	$3,107,148
Institute Equipment	$1,141,133
Institute Supplies	$418,427
f. Contractual	
Sub-recipient	$26,012,130
Vendor	$148,878
FFRDC	$350,000
Total Contractual	$26,511,008
g. Construction	$0
h. Other Direct Costs	$949,826
Total Direct Costs	$32,127,543
i. Indirect Charges	$2,505,595
Total Project Costs	$34,633,138

In addition to planning for resources in Budget Period 1 and beyond, the PowerAmerica Institute has made significant accomplishments in establishing the internal mechanisms and protocols for income-generating activities including member fees, contract research, and fee-for-service activities. A variety of collaboration instruments and accounts have also been established to facilitate these activities. Specifically, accounting structures for employees, faculty and sub awardees are functional as are internal accounts to accept membership fees with corresponding subaccounts to establish funds for member-sponsored projects, sustainability planning, marketing and other membership-funded activities. Additionally, standard operating procedures have been established and are guiding instances of in-kind contributions, fee-for-service activities and other revenue generating events.

Membership: Under the leadership of Jim LeMunyon, Manager of Membership & Industry Relations, the Institute is executing the membership recruitment strategies to develop targets for early adopter candidates, sustaining, full, and affiliate membership and engagements with these candidates are underway and will continue. Strategies for engaging with the larger technical community and other potential members, through conferences, trade shows, symposiums and other events are underway and ongoing. Building upon the membership recruiting efforts, Mr. LeMunyon is undertaking the Strategic Planning process for the Institute to drive the long-term success and sustainability of the Institute. A strategic planning kickoff meeting attended by PowerAmerica staff and the Membership Advisory Board was held on December 3rd 2015 to gather inputs and define the strategic vision for the Institute. A series of future meetings will be scheduled to perform SWOT analysis, define the strategies to capitalize on opportunities and identify strategic issues and address potential resource gaps. The plan is being developed and will all culminate in the first report on strategic planning analysis in March 2016.

Membership by level

Road mapping: Dr. Robert Trew, Interim Chief Technology Officer, in cooperation with Dr. Muth, has initiated the Technology Roadmap for the Institute, which will be a key driver for informing the Institute's strategic planning process and identifying market and technology trends that will help shape the success of the Institute. A series of meetings conducted between members of PowerAmerica staff, Dr. Trew and DOE on consensus for the expected product have been conducted and Dr. Trew is currently laying out a detailed plan for producing this roadmap. During the early planning process, two Yole reports were identified for acquisition and are being pursued to guide the development of the PowerAmerica roadmap. At present, Dr. Trew is conducting discussions with various experts and getting different opinions regarding market and technology tradeoffs. Working groups amongst the membership and other subject-matter-experts will be formed in the near future, and these groups will help to develop the detailed Technology Roadmap.

Call for Projects: In October 2015, PowerAmerica initiated its first Call for Projects to award new technical and education & workforce projects for Budget Period 2. This call has received an enthusiastic response from existing and potential new members. In total, 93 concept papers were received within the following focus areas:

- 20 in Foundry Operations (Focus Area 2)
- 17 in Packaging, Power Electronics Foundry, Test & Reliability (Focus Area 3)
- 46 in Accelerating WBG Adoption for Power Electronics Applications (Focus Area 4)

- 10 in Education and Workforce Development (Focus Area 5)

During the initial compliance screening on 26 October, only one concept paper was deemed to be non-compliant and the remaining concept papers were sent to external reviewers, with individual WebEx sessions held, by Focus Area, with the reviewers to generate a formal recommendation, by Focus Area, for encouraging or discouraging the submission of Full Applications. Out of the 92 concept papers that were sent for external review, 57 papers were encouraged for Full Applications, with the respective totals by focus area as follows:

- 12 in Foundry Operations
- 8 in Packaging, Power Electronics Foundry, Test & Reliability
- 29 in Accelerating WBG Adoption for Power Electronics Applications
- 8 in Education and Workforce Development

Milestone summary as of Dec 1, 2015

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
1.1.1	Executive Director Hired	Month 3	Complete
1.1.2	Institute Staffing Plan Submitted to DOE	Month 3	Complete
1.1.3	By-laws agreed to by sub-recipients	Month 3	Complete
1.1.4	Staffing plan hires identified and committed to	Month 6	Complete
1.1.5	Remaining Institute leadership positions hired	Month 12	On-track
1.1.6	Preliminary Resource Plan submitted	Month 3	Complete
1.1.7	Initial headquarters operational	Month 6	Complete
1.1.8	Long-term resource plan reviewed by Executive Committee	Month 12	On-track
1.1.9	Lab and office space is operational	Month 14	On-track
1.1.10	Operations and Communications Plan first draft	Month 3	Submitted
1.1.11	Internal website operational	Month 6	Complete
1.1.12	Internal communication executed according to plan	Month 9	Submitted

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
1.2.1	Membership agreement submitted to DOE	Month 3	Complete
1.2.2	Secure data exchange preliminary method established	Month 3	Complete
1.2.3	Risk mitigation strategies implemented	Month 3	Complete
1.2.4	Membership recruitment strategy submitted to DOE	Month 6	Complete
1.2.5	Membership candidates identified by category	Month 12	On-track
1.2.6	Voice of the customer report on the Institute	Month 12	On-track
1.2.7	Financial targets for sustainability report	Month 14	On-track
1.2.8	Catalog of existing services	Month 5	Submitted
1.2.9	Report on strategy to attract contract research	Month 12	On-track
1.2.10	Report on feasibility of new services for members	Month 14	On-track
1.2.11	Report on feasibility for business opportunity for software package	Month 12	Deletion of this milestone requested in the Recovery Plan
1.2.12	Formal agreement with member investments formalized	Month 14	Deletion of this milestone requested in the Recovery Plan
1.2.13	Marketing and Branding and External Communications Plan	Month 5	Submitted
1.2.14	Knowledge Distribution Strategy Report	Month 12	On-track
1.2.15	Institute Positioning Plan Report	Month 12	On-track
1.3.1	Data repository for strategic planning information	Month 5	Submitted
1.3.2	Training for all members on strategic planning performed	Month 12	On-track
1.3.3	First report on strategic planning analysis	Month 14	On-track

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
1.3.4	Report on second cycle of strategic planning analysis	Month 14	Deletion of this milestone requested in the Recovery Plan
1.3.5	Member Advisory Committee majority recommended list of roadmap items	Month 5	Deletion of this milestone requested in the Recovery Plan
1.3.6	Member Advisory Committee majority recommended Industry Technology Product Draft Roadmap	Month 14	On-track
1.3.7	Report on survey response from at least two thirds of Institute members	Month 14	On-track
1.3.8	Member Advisory Committee majority approved Industry Technology Product Final Roadmap	Month 14	On-track
1.3.9	Private Roadmap refined and Public Roadmap released	Month 14	On-track
1.3.10	Accounting structure in place and demonstrated	Month 3	Complete
1.3.11	Draft accounting instrument set up and demonstrated	Month 5	Complete
1.3.12	Accounts set up and demonstrated	Month 3	Complete
1.3.13	In-kind and industry-sponsored standard operating procedures in place	Month 3	Complete
1.3.14	Fee-for-service activity standard operating procedures in place	Month 3	Complete
1.3.15	Draft of detailed analysis of operating costs	Month 8	Complete
1.3.16	Draft of detailed analysis of potential revenue sources	Month 5	Complete
1.3.17	Draft of detailed infrastructure investment plan	Month 8	Deletion of this milestone requested in the Recovery Plan

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
1.4.1	Operational Plan	Month 5	Submitted
1.4.2	RFP for open competition fund issued	Month 8	Submitted
1.4.3	Selection of at least three projects from open competition fund	Month 11	Submitted
1.4.4	Subcontracts for open competition fund projects completed	Month 14	On-track
1.4.5	RFP for membership-funded projects issued	Month 14	On-track

Education and Workforce Development

Focus Area 5: Formally, the Education and Workforce Development Team (EWDT) has been in existence since October 1, 2015 when Steve Walsh officially became the Director of Education and Workforce Development; however, portions of the team began to be assembled in the late-June to early July 2015 timeframe. Specifically, under the leadership of Dr. Gail Jones, and with the assistance of Dr. Elysa Corin and STEM Education PhD candidate Emily Cayton, they were able to organize and initiate the PowerAmerica Summer Institute. (Note that Dr. Corin has left the team, having accepted a postdoctoral position at Harvard University.)

K12: In addition to having the established relationship with the Friday Institute through Dr. Jones, the EWDT is expanding that relationship to possibly include work that is being done by Dr. Glenn Kleiman's team on MOOCEd technology–relationships have been established and discussions are ongoing. Planning the objectives, curricula, marketing, promotion, logistics, cost estimates, and timeline for the high school teachers' portion of the 2016 Summer Institute is underway.

It should be noted that it is not the intention of the PowerAmerica Institute to create a standalone national K12 STEM education initiative. The intention of the Institute is to work with and through the STEM researchers at the NC State College of Education and the Friday Institute to help ensure that age appropriate pedagogy regarding energy–generation, conservation, and efficiency–provided by WBG semiconductors and the products they enable are developed and distributed–in part–through their local and national networks at the K12 level.

Community College: Contact has been initiated with several of the appropriate NSF Advanced Technology Education Centers. These centers focus exclusively on strengthening technician level skills and education that is critical to our nation. The EWDT continues its conversations with the leadership of these centers while strategizing on different alternatives for moving forward in collaborations that promote PowerAmerica's mission.

Planning the objectives, curricula, marketing, promotion, logistics, cost estimates, and timeline for the community college instructors' portion of the 2016 Summer Institute is underway. But, much more dialogue needs to take place among the EWDT, ATEs and the targeted community colleges in order to develop an effective and efficient program of instruction for the 2016 Summer Institute.

It should be noted that it is not the intention of the PowerAmerica Institute to create a standalone WBG power electronics program for technician-level training at the community college level. Rather, it intends to collaboratively develop with the appropriate stakeholders means and methods to incorporate needed WBG semiconductor knowledge and skills into existing programs.

Undergraduate: The PowerAmerica URS (Undergraduate Research Scholars) program is considered the flagship program of EWD. The students targeted for this program are those with aspirations to pursue graduate degrees (MS and/or PhD) and to become the future leaders in the WBG power electronics industry. The URS program will be modeled after a similar program developed by Dr. Jones at the ASSIST (Advanced Self-Powered Systems of Integrated Sensors and Technologies) Center. Important differences between the two programs will include required interaction with industry partners and both an academic year URS version as well as a summer URS. (Note, both URS versions will have as one of their goals the recruitment and retention of women and minorities; however, extra emphasis will be placed on this during the summer URS.) In addition, collaborations with the NC State DELTA (Distance Education and Learning Technology) organization began, to discuss the possible creation of online educational modules dedicated to the world of WBG power electronics education. Lastly, the team anticipates a special section of the College of Engineering's Engineering Entrepreneurship Program sponsored by PowerAmerica and its members and dedicated to promoting senior design projects that use WBG power electronics components or products.

While discussions with industry are still in their preliminary stages, and the Needs Assessment Survey is ongoing, the trend appears to be pointing toward industry's preference for hiring students from academic institutions whose educational programs provide undergraduates an opportunity to pursue courses in power electronic/systems theory and that incorporate an extensive hands-on portion of the courses to projects.

Dr. Muth and MG Justice address undergraduate engineering students

Graduate: The Professional Science Master (PSM) EPSE (Electric Power Systems Engineering) Program with a concentration in WBG semiconductors has been established, with an online version to hopefully follow soon. The PSM dedicated solely to WBG semiconductors has been placed on hold pending further investigation regarding the needs of industry and the resources required to support its creation and operations. Part of this investigation is that the EWDT is in the process of studying and articulating the new skill sets required to design and build WBG semiconductor products and what level of education these new specialized employees will require. Preliminary investigations point toward the masters' level with concentrations in power electronics and/or power systems both incorporating extensive hands-on training over and above simple projects. Professional skills training (project management, risk assessment, communications) will be a valuable enhancement to the core engineering curriculum. PhDs will be hired for highly specific investigations in large corporations and for both design and specific investigations in SMEs–regardless, their numbers will be a small percentage with respect to the masters' level.

Professional: The EWDT has created and administered the first of several surveys to its members to collect data on the skills their companies need now and into 2020. Preliminary results are being collected at this time. One of our goals is to ensure the team

tracks the training of people to the technology adoption curve of WBG semiconductors. The EWDT does not want to train individuals for jobs that may not exist when they graduate. In collaboration with Phil Mintz of NC State's Industrial Extension Service, the EWDT has established relationships with MEPs from four states. (The MEP [Manufacturing Extension Partnership] is part of NIST.) Lastly, the team continues to reach out to professional organizations such as SMTA, IEEE, ASEE, ASME, etc., to establish working relationships on education and workforce training; however, more planning needs to be completed.

Additional EWD Initiatives:

1. **EWD 5-Year Strategic Plan:** Work has commenced on an EWD 5-Year Strategic Plan (SP). The SP will include an overall 5-year vision for EWD, its tactical mission for Budget Period-2 (BP2), a completed business model canvas (see Alex Osterwalder at www.businessmodelgeneration.com/canvas/bmc), detailed assumptions, required validation points, projected resource requirements, and pro forma financials. Projections will be headcount driven: monthly for BP2, quarterly for BP3, and yearly thereafter.

2. **EWDAB (Education and Workforce Development Advisory Board):** The EWDAB is in the process of being formed. Meetings have been held and professional evaluators have been identified. The EWDAB will be composed of five-persons representing highly connected professionals from STEM education research at the NC State College of Education and the Friday Institute, a dean of engineering/technology from the State of North Carolina Community College System, the current chair of the NC State College of Engineering Course and Curriculum Committee, a workforce development executive from an industry member corporation, and the PowerAmerica director of education and workforce development. The charter for the EWDAB is still under development. Liaisons from all PowerAmerica Institute members will provide input and feedback to the work performed and proposed by the EWDAB.

3. **PowerHouse:** EWDT has begun work on the concept of the PowerAmerica PowerHouse. The PowerHouse will be a multidisciplinary product design, manufacturing, & rapid prototyping facility dedicated to training the next generation of technology innovators, inventors, and educators in the art-and-science of manufacturing and technology commercialization of products enabled by WBG power electronics. At the core of the PowerHouse Concept is the teaching-manufacturing laboratory that will provide the low to medium manufacturing volume outlet for PowerHouse innovation. The PowerHouse is expected to be a transformational game-changer in advanced manufacturing education in the area of energy conservation and efficiency enabled by WBG-based power electronics.

   In the end, DoE recommended that the PowerHouse concept be abandoned. They expressed reservations about its viability, costs, and fit with the mission of the Institute.

4. **PowerUP:** The EWDT is exploring the concept of a PowerAmerica accelerator program. PowerUP would be open to all students, faculty and Institute members. The central concept of PowerUP is to rapidly prove value in the marketplace of WBG-enabled products and move them quickly toward commercialization through external investment instruments. In addition, a central tenet of PowerUP is that it be professionally operated by a former/current entrepreneur/investor with significant operational experience in technology commercialization.

   The PowerUP concept was not implemented due to several factors including the funding needs and the external support required to sustain it.

Milestone Summary as of Dec 1, 2015

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
5.1.1	Develop a needs assessment survey	Month 3	Submitted
5.1.2	Administer the needs assessment survey	Month 6	Submitted
5.1.3	Contact relevant NSF ATE Centers and identified existing skills standards	Month 9	Submitted
5.1.4	Identify six critical skill areas at the technician and engineer levels needed for training	Month 14	On-track
5.1.5	NC MEP Center identified MEP centers in three states to assist with dissemination of program information, materials, marketing, and outreach	Month 3	Submitted
5.1.6	Materials have been developed and strategic outreach plans are in place for four MEP Centers	Month 6	Submitted
5.1.7	Three hundred brochures have been distributed	Month 12	On-track
5.1.8	MEP Centers identified four additional potential partners	Month 14	On-track

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
5.1.9	Established contacts and relationships with more than three appropriate technology related NSF ATE Centers	Month 3	Submitted
5.1.10	Developed marketing materials to be distributed	Month 6	Submitted
5.1.11	Distributed 100 brochures to NSF ATE Centers	Month 12	On-track
5.1.12	Curriculum and resources have been developed into the courses for the training programs	Month 14	On-track
5.2.1	The MS in Electric Power Systems Engineering Wide Bandgap Power Electronics Concentration established and two students commence program.	Month 3	Will be submitted by 12/15/15
5.2.2	The two students work in labs on related Institute projects in WBG Power Electronics.	Month 6	Will be submitted by 12/15/15
5.2.3	Two students complete the WBG PE design project.	Month 12	On-track
5.2.4	Two students complete the WBG concentration program with a MS in Electric Power Systems Engineering.	Month 14	On-track
5.2.5	Development of new courses for the PSM program	Month 3	Deletion of this milestone requested in the Recovery Plan
5.2.6	Recruiting efforts for the PSM program in place	Month 6	Deletion of this milestone requested in the Recovery Plan

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
5.2.7	The new and revised courses and labs are finalized for the PSM program	Month 9	Deletion of this milestone requested in the Recovery Plan
5.2.8	Applicants are reviewed for the PSM program and ten students are admitted to the program for Fall 2015	Month 14	Deletion of this milestone requested in the Recovery Plan
5.3.1	Identified research projects and faculty advisors for the URS program.	Month 12	On-track
5.3.2	Developed marketing materials for the URS program	Month 12	On-track
5.3.3	Distributed 300 brochures and other marketing materials to university partners	Month 12	On-track
5.3.4	Reviewed applicants and selected ten URS candidates to participate in the program	Month 14	On-track
5.4.1	Curriculum and other resources from NSF ATEs and others are identified leverage for the Institute training program	Month 3	Submitted
5.4.2	Marketing materials are developed for the community college and high school train the trainer program.	Month 6	Submitted
5.4.3	One hundred brochures are distributed through NSF ATE Centers, community colleges, and industry	Month 14	On-track

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
5.4.4	Applicants are reviewed and candidates are selected	Month 14	On-track
5.5.1	External evaluator team reviews all programs (Summer Institute, URS, PSM, short course)	Month 12	On-track
5.5.2	Evaluation team develops a set of metrics and surveys for the program	Month 12	On-track
5.5.3	Twenty-five surveys are administered to the program participants	Month 14	On-track
5.5.4	Data is interpreted and first report with recommendations is delivered to the Institute 's Leadership team	Month 14	On-track
5.6.1	Developed storyboards for the videos and develop the WBG Online Portal site	Month 3	Submitted
5.6.2	Created one online module for high school teachers and one module for community college instructors	Month 14	On-track
5.6.3	Scheduled video shoot and WBG Online portal is developed	Month 14	On-track
5.6.4	Video and educational materials are available on the WBG Online portal	Month 14	On-track

Institute Member Accomplishments

Organization: ABB Inc., Corporate Research
Task No./Project Title: Task 2.12 / 3.3 kV SiC MOSFET Device Development
Technical Point of Contact: VR. Ramanan, VR.Ramanan@us.abb.com
Sub-award start date: 02/01/2015

Project Objectives: The purpose of this task is to accelerate the development and manufacture of 3.3 kV SiC MOSFET devices using a 150 mm silicon foundry. According to various estimates, the cost of processing SiC can be up to 50% of the final device cost. Therefore, it is important to understand the major cost components and their cost reduction aspects; this can be achieved effectively by using an existing foundry. Engineering samples of these devices will be provided for wafer level testing and in discrete packages to the Institute. Faculty members at the Institute will aid in the design and process development for these devices. Evaluating the long-term reliability of the gate oxide, as well as surge current capability and other application related performance criteria would not be part of this task.
The measurable outcomes of this task will be:

1. Process developed for 3.3 kV SiC MOSFETs with pathways determined for cost reduction and yield improvements to enable the cost reduction of 3.3 kV SiC MOSFETs in future budget periods.
2. Engineering samples of 3.3 kV SiC MOSFETs delivered to Institute for testing and analysis.
3. Tested 3.3 kV SiC MOSFETs in discrete devices with measured parameters and specifications.

Project's Contribution to the PowerAmerica Mission: The main contribution of this task can be summarized in terms of reducing the cost of WBG devices. By working closely with a world-class US-based facility (XFAB), the ABB project team aims to understand the cost reduction potential of SiC manufacturing. In BP1, the focus is on evaluating the readiness of the foundry in terms of processing 6" SiC wafers with a yield >75%. A mixture of know-how in processing from ABB as well as XFAB is necessary to effectively tackle the issues of SiC processing. Additional improvements in device designs are considered for a possible BP2 extension of the Task, as discussed in more detail in chapter 7.

Through the support from PA, ABB can efficiently collaborate with XFAB, and due to our global corporate presence, generate new opportunities for the US foundry. By running our experimental lots with XFAB, we also contribute to workforce development in US, since the engineers and operators in XFAB have the opportunity to try out new processes on our lots and qualify new tools. This creates much needed US-based expertise and a new generation of foundry specialists able to handle the challenges of processing SiC wafers.

Technical Approach: Work to be accomplished in this task includes:

1. Design of 3.3 kV SiC MOSFET.
2. Assessment of SiC foundry process steps that are non-proprietary.
3. Assessment of SiC foundry process steps that will need to be transferred to the foundry.
4. Transfer of SiC Process to foundry.
5. Design of experiment and iterated three cycles of fabrication, characterization, and testing, to improve process steps to improve manufacturability.
6. Perform wafer level testing.

Issues, Risks and Mitigations: The sub-award has been significantly delayed by lengthy legal discussions, on which the project team had no influence of. Nonetheless, together with PA management, the project team has made significant steps to refocus the task and make sure that the deliverables can still be met (in full or partially) by the official end of BP1. For example, we proposed a concrete action of substituting one MOSFET lot with a JBS diode lot, which will shorten the processing time by about 1 month while still delivering important information about the performance of XFAB in terms of process control, yield, etc.

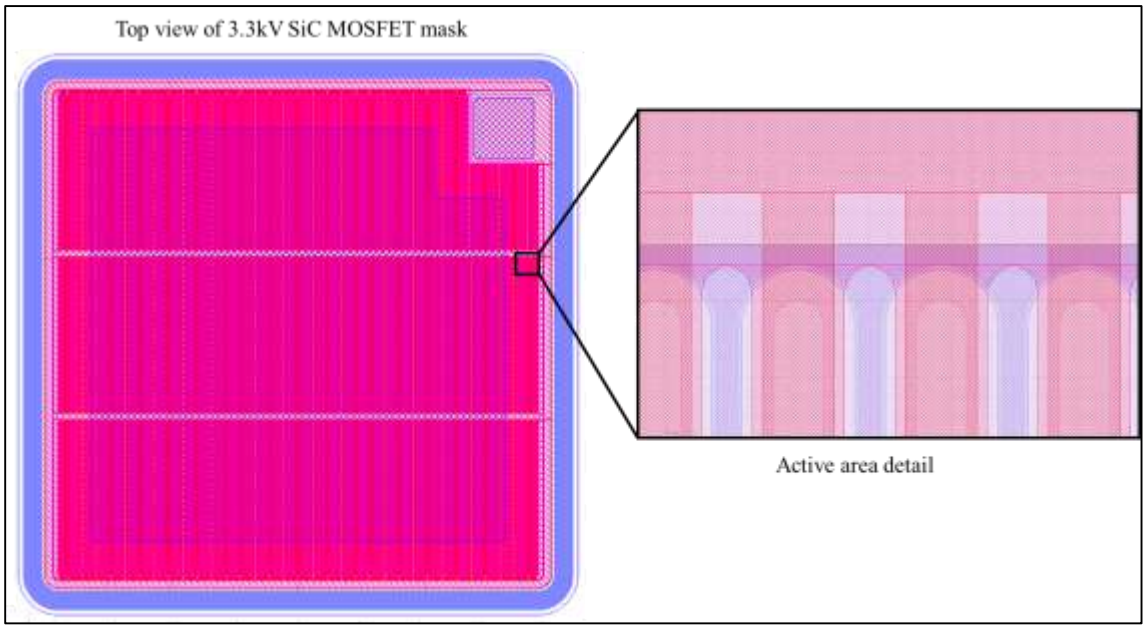
Most of the technical risks were tackled in the project by making sure the processes and designs needed to perform the work have been de-risked previously. Nonetheless, there is always an inherent risk related to the performance of XFAB (or their 3rd party collaborators) in handling our wafers, e.g. wafer breakage can happen, or processes can be performed under the wrong schedule. Therefore, our lots include multiple wafers and the purchase order to XFAB specifies a minimum of 3 good wafers to be delivered to ABB.

Another outstanding technical risk is the specific gate oxidation process required for MOSFETs– as XFAB does not have yet a qualified process in place, ABB has agreed to share with XFAB the use of the MOSFET lots in this project to fine tune this process. Outstanding issues: XFAB still outsources critical process steps to 3rd parties, and this introduces delays and higher costs. Once the dedicated SiC equipment in XFAB will be qualified for production in 2016, we expect a significantly lower processing time.

Significant Accomplishments: Two significant accomplishments are outlined below:

1. Complete design of JBS diode and MOSFET cells, including active and termination regions. In the figure below, the top layout of a MOSFET die is showed. The active area is estimated to allow for close to ideal yields. For the 3.3kV voltage class, the device area translates into a nominal current rating per device of about 25A. This design will not be modified in the next steps, while the variation in device performance due to processing artifacts will be evaluated next year once the lots are completed.

2. Complete process routers for JBS and MOSFETs that match the XFAB internal development status. These routers include now more than 150 detailed processing steps which have been discussed with the foundry during a 2 day site visit in Lubbock TX. The process includes now 10 masks for MOSFET, with a lead manufacturing time of approximately 3 months as communicated by XFAB.



Technology to Market: As mentioned in Chapter 2, the major focus of the task is still understanding the cost reduction potential through the use of the proposed PA foundry model. In BP1 we discussed extensively with XFAB their long-term pricing models were discussed extensively. With the late start of the Sub-Award, it may be more challenging to reach a clear-cut conclusion within the hard end date set for BP1. In addition, XFAB is still in the ramping phase of their line, and outsources critical process steps. This introduces additional costs and longer processing times. This situation is expected to alleviate itself after Q3'2016 when new equipment will be qualified in the foundry.
In order for ABB to successfully complete the assessment of the PA proposed foundry model, we strongly argue for an extension of the activity in Year 2. This will enable our project team to process a statistically significant number of lots (at least 10, each of 6 wafers) and run enough experiments demonstrating the suitability of XFAB as THE SiC foundry of choice. Both ABB and XFAB would have gained by the end of Year 2 a clear & concise picture about the potential for future collaboration in terms of required yields, processing cost per wafer, with expected commercial volumes potentially ramping up in 2018 –pending that all required milestones are passed successfully, and that the business case offers the required ROI.

Plans for Next Budget Period If Funded: Due to the late start date of this sub-award ABB strongly argues that a next budget period is needed to fully exploit the potential of a partnership with XFAB. In addition, XFAB still works on upgrading the production line and fine-tuning their price models accordingly.

If the next budget period is funded, ABB will continue the work on exploring further mechanisms for cost reduction in terms of $/A. The main focus will be identifying novel MOSFET designs and manufacturing processes that lead to reduced cost. For example, developing a design with improved current density can lead to a direct cost reduction potential since the dies can be made smaller. In the Year 1 budget, we are

focusing more on the manufacturing aspects, but an extension into Year 2 will enable more exploratory device designs to be tried out.
A possible schematic SOPO for the next budget period is given below:

Milestone No.	Short Title	Due date	Notes
2.12.2.1	Process established to produce functional 3.3 kV SiC MOSFETs; BV>3.3 kV	Month 4	Based on BP1 and further lot iteration, based on "Standard" design
2.12.2.2	New design 3.3kV SiC MOSFET with improved current density	Month 8	Increased current density translates into smaller dies, thus lower cost per Amp. At least 20% improvement targeted.
2.12.2.3	Samples of 3.3 kV SiC MOSFETs with improved design and processed and wafer tested	Month 12	
2.12.2.4	Around 10 lots of 6 wafers each are processed at XFAB based on "standard MOSFET design". Yield must be >85%	Month 12	In BP1 only few lots could be manufactured at XFAB. This does not provide significant statistical learning and relevance for ABB in order to confirm the validity of the foundry model proposed by Power America.

Project Output: No publications, conference presentations, awards/recognition, IP disclosures, or patent filings were done until now in this Task.

Milestone Summary

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
2.12.1.1	3.3 kV SiC MOSFET mask design and process flow finalized	Month 10	Complete Agreements with foundry in place to run wafers.
2.12.1.2	1st lot processed wafers	Month 13	Incomplete 2 lots (JBS & MOSFET) will be started in parallel in order to account for the late start date of the sub-award.

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
2.12.1.3	Samples of 3.3 kV SiC MOSFETs are wafer tested	Month 14	Incomplete
2.12.1.4	Baseline process established to produce functional 3.3 kV SiC MOSFETs; BV>3.3 kV	Month 14	Incomplete Due to the late Sub-award start date this may be a partial Go/No Go decision, since not enough lots can be processed in the given time frame.

Organization: Arizona State University (Note: Dr. Chowdury is moving UC Davis. UC Davis has been strongly supportive of PowerAmerica and is working closely with PowerAmerica to ensure that cost sharing obligations are met.)
Task No./Project Title: 2.11
Technical Point of Contact: Dr. Srabanti Chowdhury
Sub-award start date: 02/01/2015

Project Objectives: The overarching goal of the project was to design and fabricate 600V D-Mode AlGaN/GaN HEMTs. The project was divided into 2 categories. In first category we developed and characterized the dielectric layers necessary for the device fabrication using MIS capacitors and in the second category we modeled 600V HEMTs and implemented device design based on the model to achieve 600V functional HEMTs.

Project's Contribution to the PowerAmerica Mission: The project developed open foundry process that will enable proliferation of GaN-based power electronic devices, which can be easily manufactured in a Si-based foundry. Our work also resulted in increased "volts-per-micron" leading to significant decrease of the chip area for a given current rating.

Technical Approach:

3.1. Dielectric Engineering

The tasks were designed to solve reliability problems and improve performance of lateral GaN-on-Si (or GaN-on-SiC) MISHEMTs (Metal-Insulator-Semiconductor High Electron Mobility Transistors). The tasks were formulated as process modules that can be readily incorporated into a GaN foundry. Dielectrics and deposition techniques for passivation in GaN devices were studied and down-selected. Device figure of merit (FOM) enhancement through field management and dynamic R_{on} improvements were achieved. Gate stack dielectrics for single chip D-mode devices were investigated and optimized for, reliability, breakdown and channel mobility.

The desired properties of a gate dielectric in a power device include minimal threshold voltage shift after a large positive gate bias, low interface trap density generation under stress while maintaining high channel mobility in the electron channel under the dielectric. High quality passivation dielectrics are also essential for reliable GaN-based devices at the drain side edge of the gate. Therefore, it is critical to develop good quality dielectrics for the gate oxide as well as the passivation dielectrics. Al_2O_3 deposited by different deposition techniques such as Atomic Layer Deposition (ALD) and Plasma Enhanced ALD (PEALD) will be explored to produce reliable dielectrics that can withstand high field and high temperature. Emphasis will be placed on maintaining high quality bulk layers via the use of amorphous dielectrics. Achieving low Dyn R_{on} is necessary for any GaN technology to achieve widespread acceptance. It is therefore included in this task as a simultaneous requirement along with the other metrics.

3.2. Volts-per-micron enhancement

Our approach was to develop higher figure of merit devices (lower R_{on}) by improving the lateral V/micron of breakdown field strength between the gate and the drain. The present electric field for reliable devices is <40V/μm (nearly an order of magnitude smaller than the theoretical breakdown field in GaN) and what has been demonstrated in vertical GaN devices. Lateral field improvement were achieved by improving electric field management. Both lateral electric field modification using implantation and field plate structures were employed to achieve the goals. Field plate design were first developed using Silvaco Atlas software (which is widely used in industry). Devices were

built and the designs were validated. This approach will readily translate into industry as the tools and methodologies will be readily transferable. Volts per micron was determined as the 80% of the breakdown voltage divided by the gate to drain spacing. The breakdown voltage was chosen judiciously to ensure stable operation of the devices and not merely a sweep voltage, which is often reported in various literatures. As a part of this task we will be setting up the criteria for reporting volts per micron.

Issues, Risks and Mitigations: The main issue we have faced during the development of devices in BP1 is lack of vendors to obtain high voltage compatible GaN epi on Si or SiC.

Significant Accomplishments:

In the BP1 our team was able to achieve the following milestones under the program:

- Leakage current $<10^{-2}$mA/cm^2 and average breakdown electric field >3MV/cm were achieved for both ALD Al_2O_3 and PEALD Al_2O_3 gate dielectrics.
- Hysteresis <0.5V was measured; time or voltage dependent stress tests did not cause any remarkable change in C-V characteristics.
- Accurate 2D drift-diffusion model of HEMTs, which were used to optimize field plate designs.
- Field plated HEMT measuring breakdown voltages (V_{br}) up to 900V (equivalent breakdown field 60V/μm), which is significantly higher, compared to what is offered by the state-of-the art designs.

Characterization of Gate Dielectrics

ALD Al_2O_3 was deposited using a commercial ALD system Cambridge Savannah with the following conditions: TMA pulse 15ms/purge 4s, H_2O pulse 1ms/purge 4s, 260°C deposition temperature and no post deposition annealing. The average breakdown electric field of 3.3MV/cm and a record high of 6.7MV/cm were measured. CV hysteresis was 0.59V (Fig.1). Time dependent stress test in which the MIS capacitors were held in 4V for different time durations showed a series of consistent hysteresis of ~0.1V (Fig.2). Voltage dependent stress test in which the MIS capacitors were held in different positive voltages for 10mins showed a series of consistent hysteresis of ~0.15V (Fig.3).

PEALD Al_2O_3 was deposited using self-built PEALD system in Dr. Nemamich's group from the Arizona State University with the following conditions: pretreatment with H_2/N_2 plasma at 680°C, 200°C deposition temperature and post deposition annealing with N_2 at 400°C for 15min. The average breakdown electric field of 3.6MV/cm and a record high of 8.9MV/cm were measured. CV hysteresis was 0.41V (Fig.4). Time dependent stress test showed a series of consistent hysteresis of ~0.04V (Fig.3). Voltage dependent stress test showed a series of consistent hysteresis of ~0.05V (Fig.3).

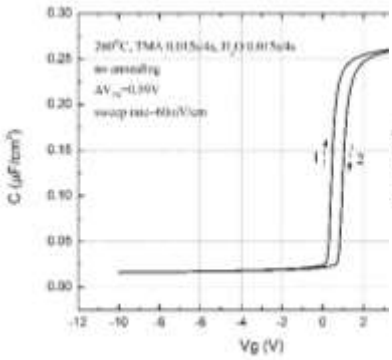


Fig.1 CV characteristic for ALD Al_2O_3

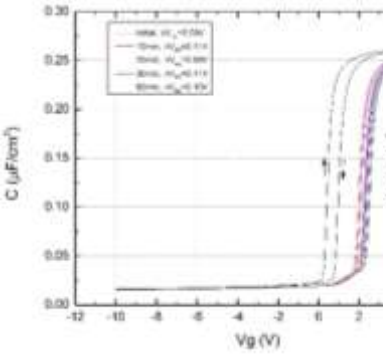


Fig.2 Time dependent stress test for ALD Al_2O_3.

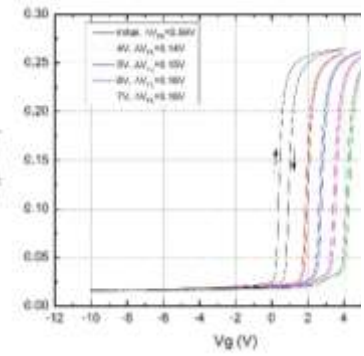


Fig.3 Voltage dependent stress test for ALD Al_2O_3.

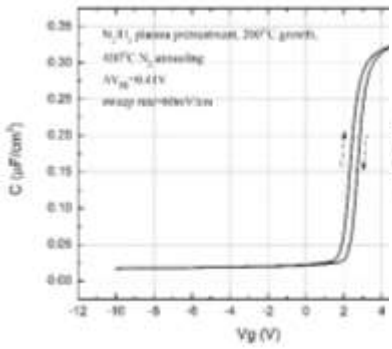


Fig.4 CV characteristic for PEALD Al_2O_3.

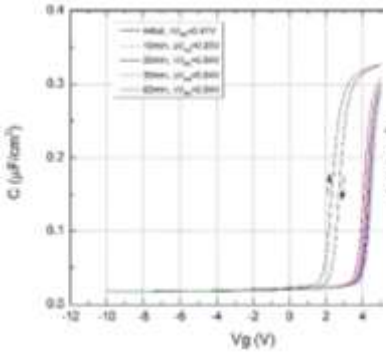


Fig.5 Time dependent stress test for PEALD Al_2O_3.

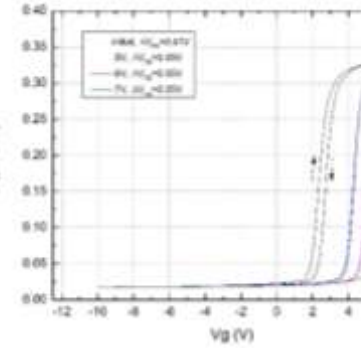
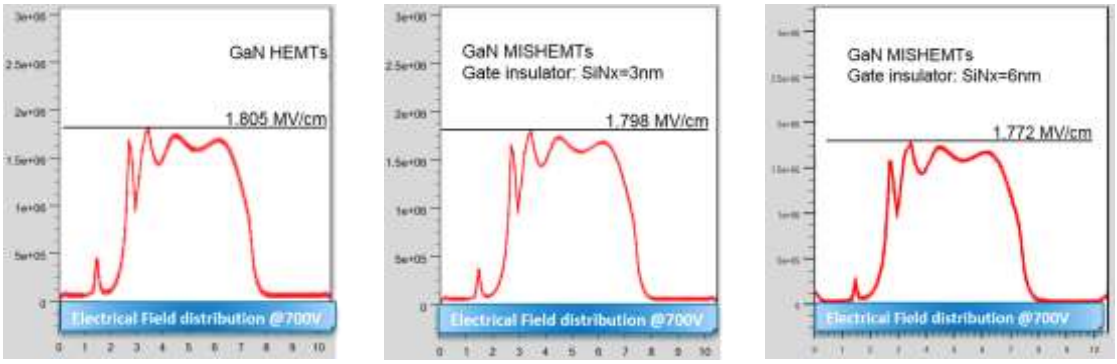


Fig.6 Voltage dependent stress test for PEALD Al_2O_3.

Electrical Field Management using Field-plate (Simulation)

Electrical field profile of field-plated GaN HEMT (or MISHEMT) with L_{SD}=10.5μm and L_{GD}=8μm was simulated in Silvaco. The electric field peak of GaN HEMT was optimized to be 1.805MV/cm at V_{ds}=700V (Fig.7(a)). The electric field peak decreases with increasing the gate dielectric thickness (Fig.7(b) and (c)).



(a) (b) (c)

Fig.7 Electric field profile of field-plated (a) HEMT (b) MISHEMT with 3nm Si_3N_4 (c) MISHEMT with 6nm Si_3N_4.

GaN MISHEMT (Experimental)

GaN MISHEMTs with L_{GD} of 5μm, 10μm, 15μm, 20μm and 25μm and L_g of 2μm were fabricated. R_{on} was in the range of 4-7ohm·mm owing to low R_c=0.43ohm·mm and

R_{sh}=382.5ohm/sq extrapolated from TLM measurement. IV characteristics of the device with L_{GD}=10µm and 25µm are shown in Fig.8 and Fig.11. V_T was around -16V as extrapolated from transfer IV curve (Fig.9 and Fig.12). Low V_{br} measurement was carried out in pinch-off and V_{ds} up to 200V (Fig.10 and Fig.13). I_g was 5.07µA/mm at V_{ds}=-200V and V_{gs}=-20V. The I_{on}/I_{off} ratio was greater than 10^5. Finally, an additional high V_{br} measurement was conducted on the MISHEMT with L_{GD}=15µm. V_{br} of over 900V was achieved using florinert during the measurement.

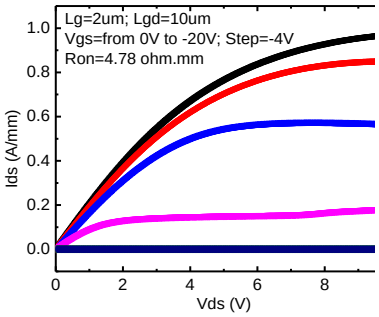


Fig.8 Ids-Vds characteristic for L_G=2µm, L_{GD}=10µm.

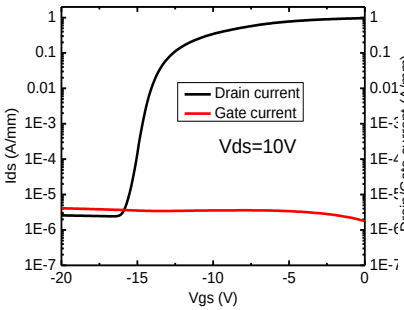


Fig.9 Transfer IV for L_G=2µm, L_{GD}=10µm.

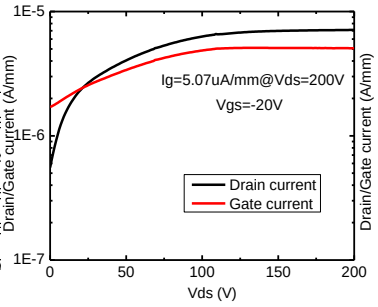


Fig.10 V_{br} measurement up to 200V for L_G=2µm, L_{GD}=10µm.

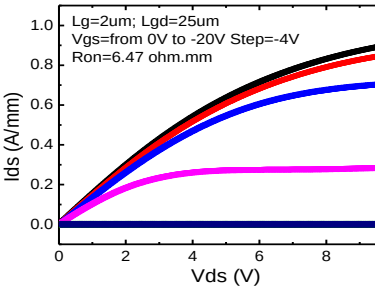


Fig.11 Ids-Vds characteristic for L_G=2µm, L_{GD}=25µm.

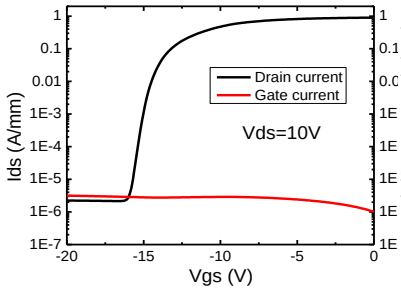


Fig.12 Transfer IV for L_G=2µm, L_{GD}=25µm.

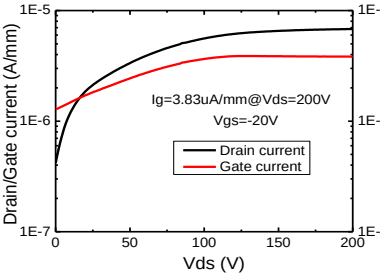


Fig.13 V_{br} measurement up to 200V for L_G=2µm, L_{GD}=25µm.

Technology to Market: The market for the medium power GaN extends from (few hundreds of watts to 10KW) and include 1) Motor Drives 2) Photovoltaic Inverter 3) Power supplies for data centers 4) Adapters and chargers for computers and laptops 5) Servo motors 6) power supplies for surgical tools.

SiC and GaN power devices are expected to claim around 22% of the $15 billion global market for discrete power electronic components by 2020 addressing just four industry segments (buildings and industrial, electronics and IT, renewables and grid storage, and transportation) [1]. For the past two decades, the US has maintained a leadership position in SiC and GaN WBG technology by investing heavily in R&D. Currently these technologies are penetrating the market, resulting in unprecedented amount of energy savings as well as job creation. However the potential impact of the GaN technology in a power converter still remain unleashed due to lack of proliferation of the knowhow pertaining to technology. Or in other words circuit and system design engineers across the country are not able to evaluate the technology due to lack of Si-like foundry. The pathway to manufacturing will be provided in this phase by **first** finding an appropriate Si foundry to run GaN wafers. **Second**, transferring the processes and recipes

developed in university cleanroom to successfully achieve medium power AlGaN/GaN HEMTs (600V-1.1kV) to the foundry. **Third,** scaling the devices in the foundry to current levels ranging between 10A and 40A. **Fourth,** collaborating with power converter architects and designers from both academia and industry to design new and existing architectures using GaN devices. GaN technology is becoming a global technology; the only way we can maintain the US competitiveness of GaN in global market is through high volume of research geared towards manufacturing the parts in the US and implementing them into the circuit and system, thereby enabling the end user to evaluate the impact of the technology. An awareness need to be created nationwide about the impact of the technology on energy savings, which is seeded in our effort to transfer GaN HEMT to an open GaN foundry.

We have made an attempt to talk to industry partners we will be able to disclose in the next budget period due to restriction imposed by on-going NDA.

[1] Lux Research's, "Beyond Silicon: Plotting GaN and SiC's Path within the $15 Billion Power Electronics Market," 2012. [Online].
Available:," https://portal.luxresearchinc.com/research/report_excerpt/10212

Plans for Next Budget Period If Funded: We propose to develop AlGaN/GaN HEMTs with breakdown voltages ranging between 600V and 1.1kV using optimized field plate structures and improved dielectric layers. The processes developed under this program will be transferred to an open GaN foundry identified by the PowerAmerica team during the course of the program.

We will take some innovative approaches to drastically reduce chip area for a rated current by rendering slant field structures. We will continue to develop reliable dielectric processes to ensure stable and reliable HEMT operation. We will develop a complete GaN modeling software to aid testing device designs starting from their layout to generating their performance matrix.

Milestone Summary

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
2.11.1.1	Develop and implement ALD and PEALD gate dielectrics using MIS capacitors, while maintaining a channel conductivity of <350ohms/sq , V_{TH} hysteresis of <500mV, and low gate leakage of 10μA /mm (10mA /cm²) measured at pinch-off and 100V V_{ds}. (Month 3)	Month 3	Complete

2.11.1.2	maintaining a channel conductivity of <300ohms/sq , V_{TH} hysteresis of <500mV, and low gate leakage of 1µA /mm (1 mA /cm^2) measured at pinch-off and 100V V_{ds}. (Month 9)	Month 9	complete
2.11.2.1	Drift-diffusion model for field plate optimization and implementation of the same to achieve D-mode HEMT with breakdown field ~50V/µm, R_{on} (static) < 12 ohm-mm (=6milliohm-cm^2) demonstrated. (Month 6)	Month 6	complete

Go/NO-GO Decision Point: D-mode HEMT with dynamic Ron <25% (measured within 200ns of turning off the high voltage pulse with a duty cycle of 10%) and breakdown field ~60V/µm, R_{on} (static) < 11ohm-mm (=6milliohm.cm^2) and gate leakage < **1µA /mm (1 mA /cm^2)** demonstrated. (Month 12)

Organization: Arizona State University
Task No./Project Title: 4.15 Development of SiC/GaN Based High Performance PV String Inverters and Micro Inverters
Technical Point of Contact: Raja Ayyanar
Sub-award start date: 02/01/2015

Project Objectives: The objective of this R&D project is to design and demonstrate in hardware the performance and efficiency entitlements of power conversion using SiC and GaN devices for solar PV applications. Transformer-less string inverters, and both transformer-less and isolated microinverters are developed with the following specific goals.

Subtask 4.15.1: High performance transformer-less micro inverters with high gain DC-DC stage: Development of GaN/SiC based microinverter without transformer isolation, which requires developing a topology that is capable of achieving relatively high voltage conversion ratio from the single PV module voltage of about 25-35 V DC to 200 V. The target CEC efficiency at high switching frequencies is >95% while achieving 5X improvement in the power density from 1.8 W/in^3 to 10 W/in^3. The goal also includes elimination of electrolytic capacitors and high frequency PV ground current issues inherent in transformer-less inverters.

Subtask 4.15.2: Doubly grounded, transformer-less, dynamic DC-link string inverter: SiC based, high frequency, transformer-less, doubly-grounded (eliminating ground currents), and electrolytic-capacitor-less PV **string** inverter (3 kW) with grid support features with targeted CEC efficiency of 96% and power density improvement from 1 W/in^3 of current commercial string inverters to about 10 W/in^3.

Subtask 4.15.3: High performance microinverter with high frequency transformer isolation: Development of GaN based high frequency transformer isolated, electrolytic-capacitor-less microinverter with grid support features, with >95% CEC efficiency and with a 4X improvement in power density from less than 2W/ in^3 of commercial inverters to more than 8W/ in^3.

Project's Contribution to the PowerAmerica Mission:

- Demonstrates efficiency and significant power density improvements in PV inverters made possible through use of WBG devices and new topologies that exploit WBG device characteristics
- Demonstrates reliable operation of commercial SiC and GaN devices in practical applications while operating near maximum voltage rating
- Enables use of high voltage film capacitors (1200V) for 120 Hz power decoupling; develops high frequency magnetics and gate drive solutions
- Directly supports 1 post doc and 3 PhD students who will potentially be leaders in WBG applications; through Education task, develops several publicly available educational videos on power electronics

Technical Approach: In single-phase PV inverters a key challenge for achieving high power density and high reliability is the power pulsation at twice the line frequency (120 Hz in the US) that is typically supported by large electrolytic capacitors. For transformer-less PV inverter configurations, another key issue is the capacitive coupled, high frequency ground currents. Hence, a key R&D effort in Year I is the development and demonstration of a novel inverter topology for single phase applications (PV string

inverter and micro inverters) utilizing the concept of dynamically variable DC link voltage, which efficiently solves the two key issues in single phase transformer-less PV topologies as below:

- The topology allows double grounding, i.e., the PV array can be connected to the neutral thus completely eliminating high frequency, capacitor-coupled ground currents.
- The dynamic DC link concepts allows the use of very low values of capacitance while supporting the 120 Hz power pulsations in single phase inverters, thus completely eliminating the need for electrolytic capacitors which is a major reliability issue in several string/micro inverter designs at present. It may be noted that the capacitance needed for supporting the 120 Hz power pulsation does not depend on the switching frequency, hence, it is important to reduce this value through topological innovation in high frequency converters as envisioned here. In order to achieve high energy density in the DC link film capacitors it is advantageous to operate at higher voltages (>1kV) which makes it attractive to use 1200 V SiC MOSFETs which feature very low $R_{DS\ ON}$.

A topological variation to dynamic dc link voltage circuit shown in Fig. 1 is utilized for the 3 kW transformer-less string inverter. The input voltage is directly controlled by a high bandwidth controller to minimize the 120 Hz ripple, allowing the dynamic dc link to support the power pulsation using only film capacitors. The topology is capable of supporting a range of leading and lagging power factors. All the switches are realized with 1200 V SiC devices (C2M0080120D) from CREE.

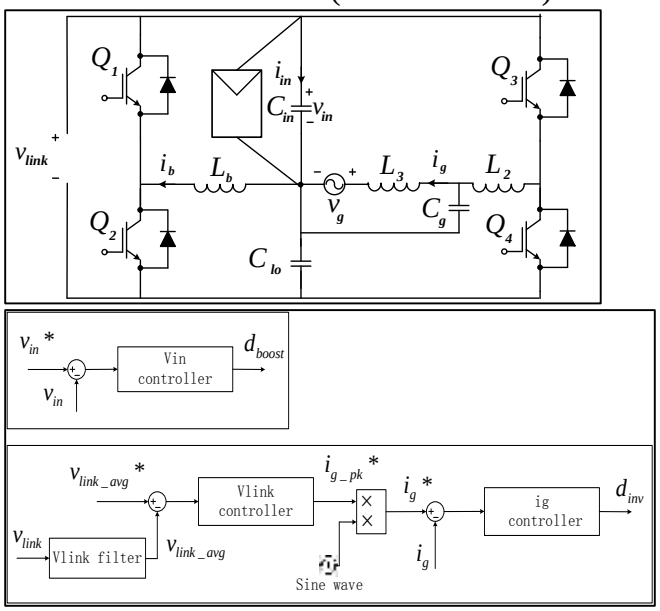


Fig. 1 Dynamically variable dc-link, all-film capacitor, transformer-less PV inverter topology (patent pending) and the corresponding control block diagram

For the microinverter a similar approach as above is used for the dc-ac conversion and 120 Hz power decoupling. In addition, the microinverters use a high-gain non-isolated dc-dc stage for the transformer-less version and a high step-up ratio isolated topology for the transformer-based version. The technical approach involves a thorough simulation-

based analysis of several potential topologies for the high gain and isolated dc-dc stages for the microinverter and select the optimal topology for hardware validation. The low voltage switches (< 200 V rating) are realized with EPC GaN EPC2010 and EPC2021, and all the high voltage switches (~ 600 V) rating) are realized with GaN Systems devices (GS66508P). The control is implemented using TI TMS320F28335.

Issues, Risks and Mitigations: Printed circuit board layout related issues are critical challenges in achieving reliable operation of WBG based inverters and in achieving the targeted efficiency and power density. For the 3 kW string inverters, which use SiC in standard packages, we have gone through several iterations of the PCB, and driver and protection circuits to achieve the target efficiency and exceed the power density goals. The GaN devices in microinverters, due to their special packages are more challenging and an added potential risk is that per the intended design, we operate the devices close to their maximum voltage ratings to achieve high efficiency and small capacitor size. We are currently going through different iterations of layout, gate drive, protection and power supplies, and as possible mitigation measures we will try reducing the operating voltages if needed, and slowing the switching transition speeds through suitable gate drive design (both of which may have small impact on the efficiency) and choose the optimal switching frequency considering these impacts

Significant Accomplishments:

High performance transformer-less and isolated micro inverters:

- Several potential topologies including switched capacitor circuits and several extended-duty-ratio circuits have been compared through detailed design and simulation for the transformer-less, high gain stage
- The three-stage extended-duty-ratio converter shown in Fig.2a is finally chosen as the most suitable to achieve the required power density and efficiency targets; it has been fully validated in simulation with detailed loss models.
- Several potential topologies including dual-active-bridge (DAB), semi-DAB, active-clamp and Weinberg converters, and asymmetric half bridge have been compared through detailed design and simulation for the isolated microinverter
- The asymmetric-controlled, half-bridge shown in Fig. 2b has been chosen for final implementation due to its low magnetics volume and low switch count; this topology has been fully validated in simulation with detailed loss models.

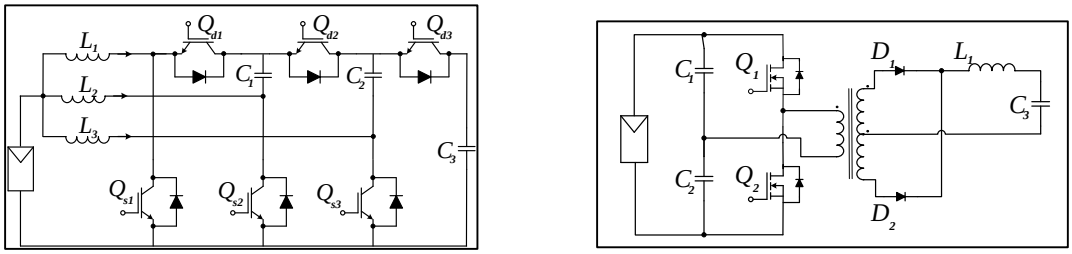


Fig. 2 DC-DC stages of the two microinverters (a) Extended-duty-ratio, high-gain converter for transformer-less inverter and (b) asymmetric-controlled half-bridge for transformer-based inverter

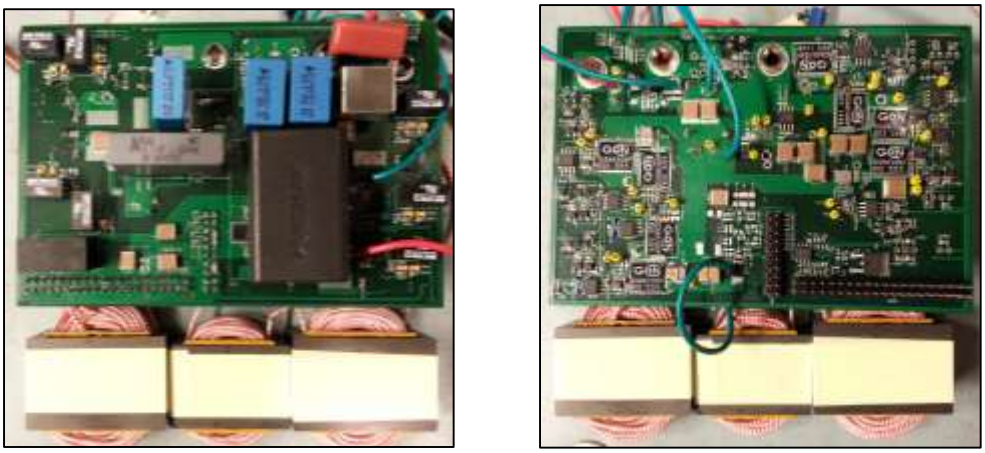


Fig. 3 Transformer-less microinverter prototype: top side (a), bottom side (b) (Size: 5.39 X 5.09 X 0.85 = 23.32 in^3)

- The hardware prototype for the transformer-less microinverter has been fabricated and is currently being tested. The target is to improve the power density by 5X from the present commercially available microinverter; i.e., from a value of 1.8 W/ in^3 to 10W/ in^3. The top and bottom views of the prototype are shown in Fig. 3. The estimated power density of this prototype is 12.8 W/ in^3 (volume: 5.39 X 5.09 X 0.85 = 23.32 in^3) without considering the heat sink, DSP-controller, and EMI filters.
- For the transformer-isolated microinverter, the dc-ac stage will be the same as that shown in Fig. 1 with the DC-DC stage added separately. The design and PCB layout of the DC-DC stage has been completed and the PCB has been ordered and the testing will commence by the end of Quarter 3 (Nov 2015).

High performance transformer-less string inverter:

- A new dynamic dc link topology (combination of boost/buck-boost/half-bridge inverter) developed and an invention disclosure has been filed with AzTE
- Two generations of hardware prototypes completed, tested (with passive loads) and evaluated for functionalities and performance; Figure 4 shows the string inverter hardware prototype
- Performance at different power factors verified; Figure 6 shows the salient waveforms under unity power factor mode and at a power factor of 0.7 leading (which is the worst case condition)
- Power density achieved is > 30W/in^3 (without EMI filters, relays) which is well above the target of 10 W/in^3
- CEC efficiency target of 96% is achieved at 75 kHz; Figure 5 shows the measured efficiency plots (which do not include 6 W control/drive power)

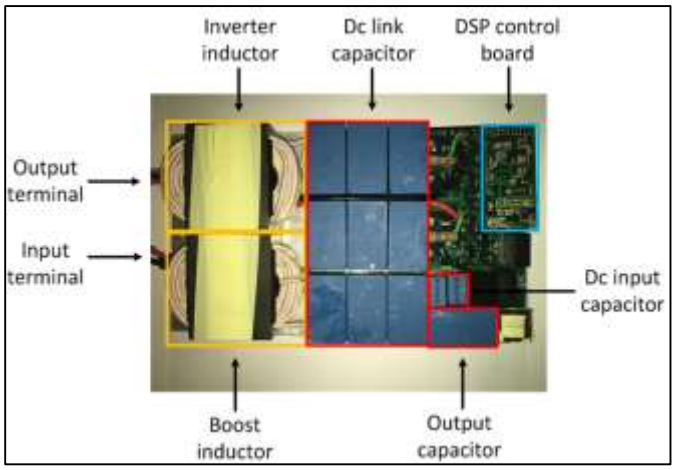
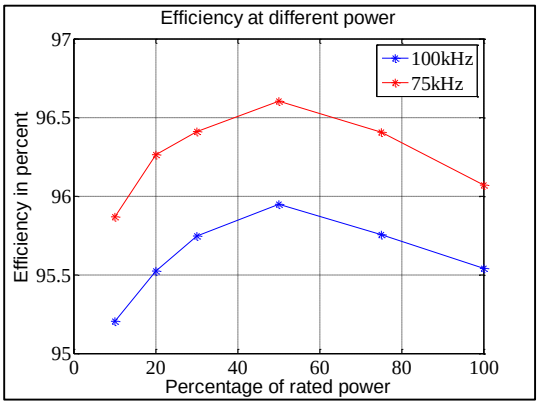


Fig. 4 3 kW string inverter prototype

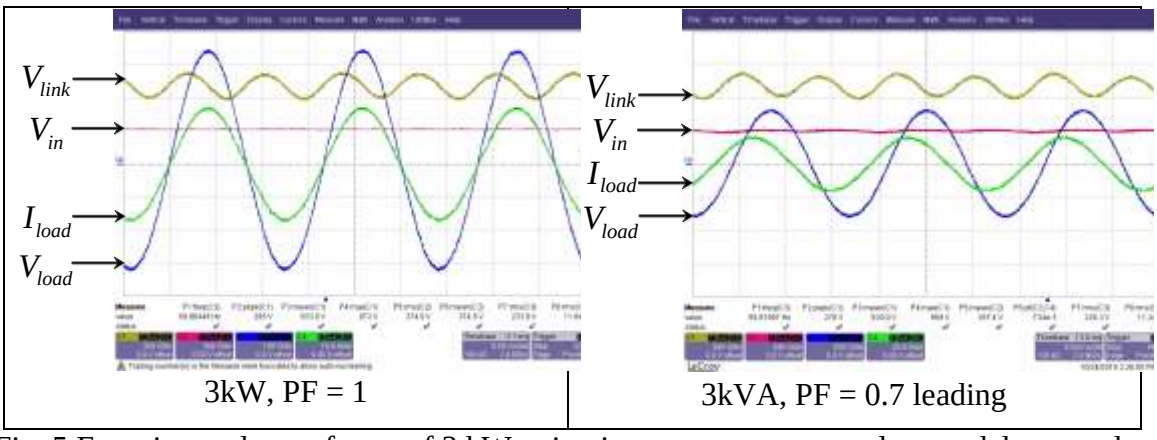


CEC 96.4%

CEC 95.8%

Control/drive power not included

Fig. 5 Measured efficiency



3kW, PF = 1

3kVA, PF = 0.7 leading

Fig. 5 Experimental waveforms of 3 kW string inverter prototype under standalone mode

- Low 120 Hz ripple in the input voltage achieved per target (< 3% of nominal input voltage)
- Negligible common mode ground current due to the connection of the negative terminals of PV and neutral

- The prototype uses only film capacitors; the capacitor used for 120 Hz power decoupling is 15 uF/kW (at 1100 V rating) which is significantly better than the target of <35 uF/kW (there is additional 5 uF/500V at the input to filter switching frequency component)

Educational videos, animations and simulations for WBG based power electronic conversion

Presentation material for the videos on the module on power converters for solar PV with WBG devices and the module on WBG device basics for power electronics designers have been put together and a story board highlighting some of the contents were submitted. The videos for these two modules will be recorded in November and December. The videos will be prepared by screencast tools such as Adobe Captivate by Dr. Ayyanar and from videos taken by the research students and post-doctoral scholar while running the hardware prototypes and device characterization. About 10 PLECS-based simulations corresponding to above material have been developed for use in web-based interactive simulations.

Technology to Market: The plan is to prove the merits of the topologies, control methods and merits of WBG devices in several hardware prototypes and approach inverter manufacturers for further development and licensing.

Plans for Next Budget Period If Funded: Two main challenges in the dynamic link topology are that the devices are subjected to more than twice the voltage stress compared to conventional H-bridge, which leads to higher switching losses even for SiC devices, and higher ac filter requirement due to two-level, bipolar PWM. To simultaneously address these two issues, the main inverter leg is proposed to be made three-level by the addition of two switches which significantly reduce the switching losses. More importantly, the three-level variation also reduces the size of grid side filter significantly compared to BP1 solution. The second topological innovation proposed for both string and microinverter is the use of two half-bridge inverters in a split-phase configuration, with the two inductors of the ***two phases optimally coupled***. This results in three main advantages – (1) half the voltage stress allowing 600 V GaN devices instead of having to use 1200 V SiC only, (2) optimal coupling mimics the performance of three-level or unipolar PWM which along with the cancellation of 60 Hz flux component in the common core results in a large reduction in the inductor size, and therefore, inductor losses, (3) the current through the buck-boost dc-dc stage is significantly reduced and allows for easier implementation of zero voltage transition circuits. With these improvements CEC efficiency of 98% for string inverters and 96% for microinverters are targeted while further improving power density and switching frequency.

Another new project proposed for BP2 is the design and demonstration of a fully modular power conditioning system block (PCSB) for microgrid applications. It aims to develop a fully-modular power conversion architecture where high performance dc-ac building block converter modules made of WBG devices can be connected in many configurations of series and parallel connections at the input and output ensuring dynamic sharing of appropriate voltages and currents. The building-block converter module is

tentatively planned to be 25 kW, 1kV AC, 380 VDC with 98% efficiency. Three such modules will be used to demonstrate a larger, modular power system.

Project Output:

1. R. Ayyanar, Y. Xia, J. Roy, "Transformer-less, reduced volume PV inverter topology," Invention disclosure filed with AzTE, 11/20/2015

2. String inverter prototype present by Y. Xia at "IEEE ECCE 2015 Student Project Demonstration on Emerging Technology" in Montreal, Sept 2015

3. Y. Xia, R. Ayyanar, "High Performance ZVT with Bus Clamping Modulation Technique for Single Phase Full Bridge Inverters," accepted and to be presented at IEEE Applied Power Electronics Conference (APEC) March 2016, Long Beach, CA.

Milestone Summary

Milestone No.	Short Title	Due date	Status (complete /incomplete, notes)
4.15.1.1	Optimum circuit configuration for the transformer-less microinverter developed conceptually	Month 3	100% complete
4.15.1.2	Performance of the chosen architecture for the different stages validated in detailed simulations	Month 6	100% complete
4.15.1.3	Fabrication of a 300 W transformer-less microinverter completed using commercial GaN/SiC devices	Month 9	100% complete
4.15.1.4	A fully functional 300 W transformer-less microinverter with only film capacitors demonstrated with CEC efficiency above 95% at a switching frequency above 100 kHz and with 5X improvement in the power density compared to current commercial microinverters	Month 14	Task on target
4.15.2.1	Validation of dynamic dc link topology in simulation to meet the performance metrics	Month 3	100% complete
4.15.2.2	Fabrication of a 3 kW transformer-less PV inverter	Month 6	100% complete
4.15.2.3	A fully-functional 3 kW, transformer-less PV inverter with power density above 10W/ in^3, 97% CEC efficiency	Month 9	100% complete; Achieved 96.4% CEC efficiency at 75 kHz and well above 10W/in^3
4.15.2.1	Demonstration of grid support features, power factor control on transformer-less string inverter	Month 14	Task on target

Milestone No.	Short Title	Due date	Status (complete /incomplete, notes)
4.15.3.1	Optimum circuit configuration and converter topology for the DC-DC isolated stage and the DC-AC stage identified	Month 3	100% completed
4.15.3.2	Capability of the topology and design to achieve >95% CEC efficiency at high switching frequency demonstrated in simulation	Month 6	100% completed
4.15.3.3	Fabrication of a microinverter with high frequency transformer isolation and rated at 300 W completed	Month 9	90% completed
4.15.3.4	A fully-functional, 300 W PV micro inverter, using only film capacitors demonstrated in grid connected mode with >95% CEC efficiency and power density >8W/cubic inch, and reactive power capability	Month 14	Task on target

Fayetteville

Organization: Cree Fayetteville, Inc. (Note: Arkansas Power Electronics International (APEI) was purchased by CREE. CREE has now spun out Wolfspeed. For the purposes of this report we are treating the business unit of Wolfspeed in Fayetteville separately from CREE Wolfspeed since it has a distinct statement of work)	
Task No./Project Title: Task 3.1: Power Module Development and Manufacturing	
Technical Point of Contact: Dr. Jared Hornberger	Business Point of Contact: Dr. Ty McNutt
Sub-award start date: 02/01/2015	

Project Objectives: Task 3.1 seeks to establish a igh volume, wide bandgap (WBG) power module-packaging foundry through the utilization of Cree Fayetteville's existing WBG power module and power discrete facility. This facility, located in Northwest Arkansas, is an AS9100- and ISO9001- certified manufacturing facility for production of aerospace, industrial, and commercial power electronic products. The goal of the WBG packaging foundry model is to provide Institute partners with packaging services for a wide range of device technologies, throughout the life of the Institute .

Additional objectives of the packaging foundry are to increase production capabilities, throughput, and to expand the range of packaging options available for WBG technologies. Target improvements to the foundry during this budget period include the implementation of x-ray inspection for low-voiding die and substrate attach, as well as the implementation of automated electrical testing. Product offering targeted in this budget period include a full-bridge 1200V, 50A module and a 1700 V, high current half-bridge module. New module development targeted medium voltage applications with the design of a 3.3 kV half-bridge module and associated gate driver.

Project's Contribution to the PowerAmerica Mission: The goals of Cree Fayetteville align perfectly with the mission of PowerAmerica; Cree Fayetteville continually advances the state-of-the-art in packaging capabilities for WBG technology, while continuing to offer a wide range of products to meet the needs of a vast number of end user applications. Cree Fayetteville products span market needs across automotive, energy, aerospace, defense, and industrial applications. By continually ramping up advanced manufacturing in the US, Cree Fayetteville is not only meeting the market demand for WBG modules and device, but is also spurring domestic economic growth.

Technical Approach: Task 3.1.1 is to increase the packaging foundry throughput and capabilities by improving in-line testing capabilities and process automation. In this task, the power module foundry facility focused on improving several additional in-line module inspection steps, such as X-ray, automated optical inspection (AOI), and automated electrical test. High priority was given to making improvements to the X-ray in-line testing of both the die and substrate attach, where measurements are performed to catch voiding in the attachments.

Task 3.1.2 focused on power module packaging commercialization by increasing the availability of packaging options through the release of new product offerings. Specific modules and companion gate drivers released as products include: an ultra-compact, high temperature power module with a four-switch position 1200V/50A H-bridge topology and a high temperature-capable two-switch position half-bridge topology power module at 1700 V and 200A per switch position.

Task 3.1.3 was targeted at the packaging needs for commercial medium voltage modules and gate drivers; this task capitalized on new in-development devices for 3.3 kV voltage levels. A medium voltage (3.3 kV), half-bridge power module was designed and fabricated with high temperature capability of 175+ °C, which is optimized for low

inductance, low thermal resistance, and high reliability over a wide range of temperature extremes. The module is also capable of high current capability, initially targeting >200 A. The module has a companion gate driver board, with integrated power supplies, optimized to support the voltage range and form factor of the module. Companion datasheets for both products were developed to enable end-user implementation and begin the end-system integration process. Full, industry standard characterization of the power module includes: static and dynamic characteristics over temperature, minimum and maximum operating conditions, and transient thermal graphs.

Issues, Risks and Mitigations: The issues to date have been 1) negotiating the membership agreement and 2) obtaining a license for the 3.3 kV module housing. On the contract risk mitigation, working with the NCSU team, permission to start an initial amount of work was granted prior to the contact being signed, targeting production improvements and module releases at the designated trade show events. A bulk of the remaining tasks were delayed until the contract was signed on August 20th.

As for the worldwide royalty-free license on the 3.3 kV module housing, Infineon was contacted to obtain an XHP module license. Risk mitigation for this issue has been to work with the publically known footprint dimensions of the module to adapt novel layout techniques to map out die placement and maximum current ratings. Once the license agreement is completed, the final location of the gate/source kelvin contacts will be known and the module housing tooling obtained.

Significant Accomplishments:

HT-4000 Module

Cree Fayetteville has released two new power modules this year, the first was the HT-4000 module and companion gate driver released at The Applied Power Electronics Conference (APEC) in March 2015. The HT-4000 is a low profile, full H-Bridge power module which allows users a high degree of configurability. This module is particularly well suited for increasing system efficiency in a variety of new applications such as motor drives, Plug-in HEV chargers, and solar inverters. With a maximum package temperature of 225 °C, voltage of 1700 V and current of 90 A, the HT-4000 can be used across a variety of different industries from aerospace to commercial vehicles. The HT-4000, shown in Figure 1, brings all of the benefits of SiC power devices to users in an optimized, accessible package.

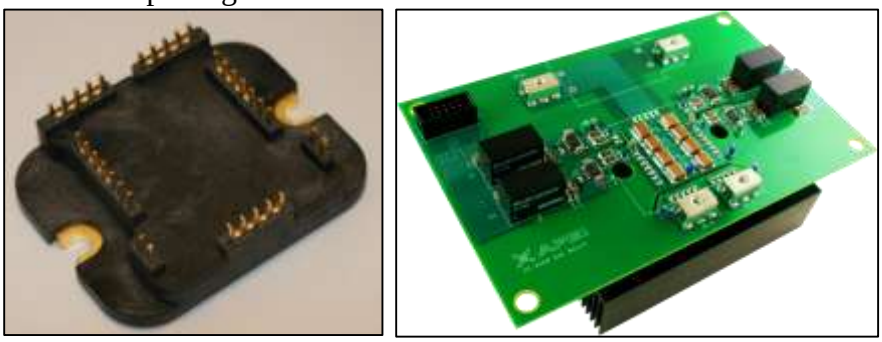


Figure 1. Image of a fabricated HT-4000 WBG power module (left) and image of the companion four channel gate driver and development board for the HT-4000 (right).

1700 V HT-3000 module

The second new module released this year was at the Power Conversion and Intelligent Motion (PCIM) conference and trade show in May 2015. This module was the HT-3231 SiC power module., which utilizes 1700 V SiC power devices in parallel to produce a half-bridge module with 9 mΩ per switch position. The HT-3231 targets applications such as high-efficiency converters / inverters, industrial & automotive traction drives, motor drives, and smart grid / grid-tie distributed generation among many others. An image of a fabricated HT-3000 module is shown in Figure 2 along with its companion ITGD2-3001 gate driver.

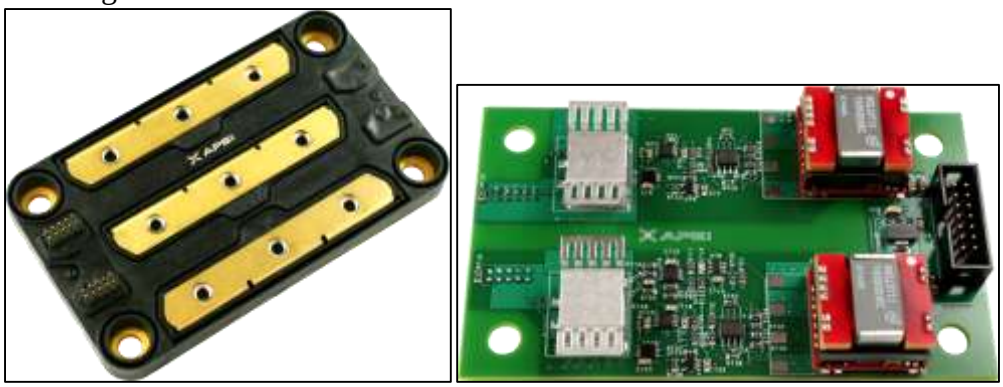


Figure 2. HT-3231 1700 V 9 mΩ SiC half-bridge power module (left) and ITGD2-3001 companion gate driver for the HT-3000 series modules.

Medium voltage power module

Cree Fayetteville has designed a medium voltage power module based on the Infineon XHP open standard module platform of 100 x 140 mm footprint, expected to be an industry standard in the near future. This is a single module platform designed to support multiple voltages from 1700 V to 6.5 kV in a single-phase leg topology. Some of the features of the Cree Fayetteville design of this module include light weight, high thermal conductivity AlSiC baseplate, high thermal conductivity power substrate, very low inductance internal design, ultrasonically-welded power terminals, 175 °C operation, and a modular, easily paralleled housing for increasing the current output.

The design process began by adapting the XHP housing to the desired module performance for SiC power devices. The power device layout was optimized for the highest power density, while maintaining sufficient thermal dissipation capability. High temperature materials are used to support a maximum junction temperature of at least 175 °C. In addition, significant effort was put into designing this module with minimal internal inductance in the power loop to enable ultra-fast switching with minimal voltage overshoot. The XHP modules (pictured in Figure 3) will feature medium voltage power semiconductors at 3.3 kV initially, pushing to 6.5 kV in the future. The inherent faster switching speeds of SiC, enabled by low inductance module design, allow the magnetics to be reduced in volume by as much as 70x, reducing the overall system cost, weight, and size. The thermal resistance of the module is 0.03 K/W in the current configuration with the ability to dissipate up to 1700 W of losses assuming a conservative cold plate performance. Based on Cree 3.3 kV device technology, the current capability will be ~ 540 A per switch position for the module design. The baseplate has been engineered to

result in a concave up-bow for minimum thermal resistance to the cold plate once bolted in place.

The next phase in the module development is procurement of the bill of materials, assembly, and initial testing scheduled for the latter portion of calendar 2015 extending into early 2016. Early prototypes will be built, followed by pre-production modules later in 2016.

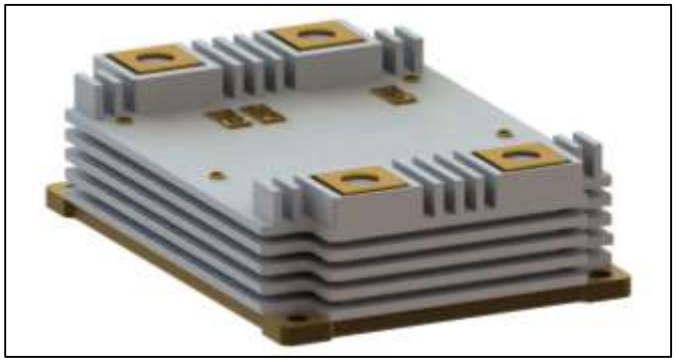


Figure 3. CAD design of Cree Fayetteville's XHP medium voltage power module.

Technology to Market: When ranking the top SiC Power device makers in 2014, Yole Development named Cree as one of the top-two market players and the only U.S. manufacturer listed within the top 97% of the market. As such, the established world-side sales chain of Cree and Cree Fayetteville will be used to transport these modules and gate drivers to market. This includes in-house sales and marketing teams and a number of worldwide distributors and sales representatives trained to understand the SiC technology.

In addition to the WBG-based modules, the gate driver and power supplies developed are being used to spur the adoption of the released power modules. Likewise, circuit simulator models of the HT-3000 module have been developed on other efforts for use in circuit simulation tools. These circuit simulator models for commonly used platforms (e.g., SPICE, LTSpice) will not only start educating today's IGBT user community about SiC, but also the next generation of WBG engineers involved with university level research. Additionally, publications at a variety of conferences have shown reference system designs and WBG design philosophies, while additional documentation (datasheets, app notes, user manuals, etc.) will be made available for ease of use and understanding of the technology.

Plans for Next Budget Period If Funded: The next budget period will consist of the following tasks:

Task 1: Improve Packaging Foundry In-Line Testing and Process Automation (Duration 12 months)

In budget period 2, the power module foundry will focus on process improvements to increase throughput and capability, in addition to setting up the line to manufacture industry standard power module footprints. In addition to the need for fully optimized, high-performance products, there is also a need to fill the gap between standard Si IGBT power module packages and new high performance WBG module packages currently produced on this line to capture more of the potential power module integration market. To fill this gap, the power module foundry will be adding processing capability to

package WBG devices in standard module footprints.

Task 2: Commercialization of a 3.3 kV SiC Power Module (Duration 12 months)

This task will enable the availability of commercial 3.3 kV voltage modules through the initial qualification of a SiC power module *designed and prototyped in PowerAmerica's budget period 1 (BP1)*: a SiC half-bridge power module capable of 3.3 kV and 540 A. This module is currently being prototyped in BP1 and sample orders have been received. The 3.3 kV SiC-based modules will be built and run through Cree Fayetteville's existing qualification facility. In addition, the *gate driver and power supply developed during BP1* will be iterated in this task; the iteration will target a UL listing for commercial release along with the power module. Likewise, circuit simulator models of the module will be developed for use in circuit simulation tools (e.g., SPICE, LTSpice).

Task 3: A 10 kV Half-Bridge SiC Power Module for Medium Voltage Applications (Duration 12 Months)

There exists a need in industry to make available medium-voltage WBG modules using SiC. As such, this tasks will introduce a SiC half-bridge power module capable of 10 kV and > 200 A and a developmental gate driver and gate driver power supply for the 10 kV half-bridge power module. Cree Fayetteville will perform initial qualification on the module and *iterate an already developed 10 kV gate driver and power supply* to accompany the module release.

Task 4: A Neutral Point Clamped SiC-Based Module for Industrial Drive Applications (Duration 12 months)

The purpose of this subtask is to meet the packaging needs for commercial modules and gate drivers for new devices currently in development for the 900 V-1700 V voltage ranges. A 900-1700 V neutral-point clamped T-type SiC power module will be designed and optimized for low inductance, low thermal resistance, and reliability over temperature extremes. The module will also be capable of high current capability, initially targeting >300A, with the prototyped and demonstrated module based on a 900 V SiC MOSFET device.

Project Output: During BP1, there were hundreds of press announcements around the world on the APEI acquisition by Cree. For example:

Cree Acquires Power Module Company APEI, *Compound Semiconductor (UVM: 29,787)*

"The companies' shared mission to deliver the industry's most innovative SiC power products has already led to successful collaboration on multiple government contracts."

Many publications have been done on the base module technology of the modules described in this report, with one falling in BP1, as listed below.

B. McPherson, et al, "A High Current, Low Inductance Wide Bandgap Power Module for High Performance Motor Drive Applications", Applied Power Electronics Conference, Charlotte, NC, March 2015.

IP:

Upcoming on the 3.3 kV power module once implemented and put into practice this quarter.

Milestone Summary

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
3.1.1.1	Install X-ray	M3	Complete
3.1.1.2	Process improvement	M6	Complete
3.1.1.3	Automate electrical test, room temperature	M12	Incomplete
3.1.1.4	Automate electrical test, high temperature	M12	Incomplete
3.1.2.1	New WBG module release: HT-4000 (H-bridge), HT-3000 (1700V)	M6	Complete
3.1.3.1	3.3 kV half-bridge module design	M12	Incomplete
3.1.3.2	3.3 kV gate driver	M14	Incomplete

Wolfspeed

Organization: Cree Wolfspeed, Inc.
Task No./Project Title : Task 2.3 Gen3 HTRB Qualification of 3.3kV SiC MOSFETs, 10kV SiC MOSFETs, 10kV SiC JBS Diodes and Gen3 3.3kV SiC MOSFET Half H-Bridge Prototype Development
Technical Point of Contact: David Grider
Sub-award start date: 02/01/2015

Project Objectives: The overall objectives for this Task 2.3 are to establish manufacturable fabrication processes for Gen3 3.3kV/40mOhm SiC MOSFETs, Gen3 10kV/350mOhm SiC MOSFETs, and 10kV/20A SiC JBS Diodes, and to carryout High Temperature Reverse Bias (HTRB) qualification of each product family per JEDEC guidelines. In addition, under Task 2.3, the objective is to develop a 3.3kV/10mOhm SiC MOSFET Half H-Bridge Module prototype using Gen3 3.3kV/40mOhm SiC MOSFETs.
The objectives for Subtask 2.3.1 for BP1 are to carry out the design and development of Gen3 3.3kV/40mOhm SiC MOSFET die on 100mm 4HN-SiC wafers, develop a preliminary datasheet for Gen3 3.3kV/40mOhm SiC MOSFET die, and carry out the high temperature reverse-bias (HTRB) testing per JEDEC guidelines for Gen3 3.3kV/40mOhm SiC MOSFET die fabricated on 100 mm 4HN-SiC wafers. The Gen3 3.3 kV/40mOhm SiC MOSFETs will be used to stimulate markets for a number of applications including rail transport and medium voltage motor drives.
The objectives for Subtask 2.3.2 are to develop a preliminary datasheet for Gen3 10kV/350mOhm SiC MOSFET die and carry out the high temperature reverse-bias (HTRB) testing per JEDEC guidelines for Gen3 10kV/350mOhm
SiC MOSFET die fabricated on 100mm 4HN-SiC wafers. The Gen3 10kV/350mOhm SiC MOSFETs will be used to stimulate markets for numerous applications including rail transport, medium voltage motor drives, and power distribution in factories and data-centers.

The objectives for Subtask 2.3.3 are to develop a preliminary datasheet for 10kV/20A SiC JBS Diode die and carry out the high temperature reverse bias (HTRB) testing per JEDEC guidelines for 10kV/20A SiC JBS Diode die fabricated on 100mm 4HN-SiC wafers. The 10kV/20A SiC JBS Diodes will be used as antiparallel diodes for the Gen3 10kV/350mOhm SiC DMOSFETs in 10kV all-SiC modules which will be used to stimulate markets for numerous applications including rail transport, medium voltage motor drives, and power distribution in factories and data-centers.
The objective for Subtask 2.3.4 is to develop a 3.3kV/10mOhm SiC MOSFET Half H-Bridge Module prototype using Gen3 3.3kV/40mOhm SiC MOSFETs developed under Subtask 2.3.1.

Project Contribution to Power America Mission: Under Task 2.3, this project will establish manufacturable fabrication processes for Gen3 3.3kV/40mOhm SiC MOSFETs, Gen3 10kV/350mOhm SiC MOSFETs, and 10kV/20A SiC JBS Diodes. In addition, the project will carry out High Temperature Reverse Bias (HTRB) qualification of these Gen3 3.3kV/40mOhm SiC MOSFETs, Gen3 10kV/350mOhm SiC MOSFETs, and 10kV/20A SiC JBS Diodes per JEDEC guidelines. This project represents a critical initial phase of the transition from development to qualification for commercial production of these Gen3 3.3kV/40mOhm SiC MOSFETs, Gen3 10kV/350mOhm SiC MOSFETs, and 10kV/15A SiC JBS Diodes at Cree's SiC power technology fabrication, test, and packaging facilities.

Technical Approach: Under Subtask 2.3.1 of this project, an optimized Gen3 3.3kV/40mOhm SiC MOSFET device design will be completed which includes efficient edge termination, reliable cell structure, and area optimization. Using this device design, Gen3 3.3kV/40mOhm SiC MOSFET fabrication lots will be carried out on 100mm 4HN-

SiC wafers, and characterization of these devices will be carried out in order to establish a stable updated Gen3 3.3kV/40mOhm SiC MOSFETs manufacturing process. Utilizing Gen3 3.3kV/40mOhm SiC MOSFET characterization data from these fabrication lots, a preliminary device data sheet will be developed for Gen3 3.3kV/40mOhm SiC MOSFET die fabricated on 100mm 4HN-SiC wafers. These fabrication lots will also be used to provide Gen3 3.3kV/40mOhm SiC MOSFET die for high temperature reverse-bias (HTRB) testing per JEDEC guidelines (i.e., 77 devices from multiple fabrication lots for 1000 hours at T_a=150°C, V_{gs} = 0V and V_{ds} = 2640V, which is 80% of the rated blocking voltage), as well as provide three-hundred and fifty (350) engineering samples of Gen3 3.3kV/40mOhm SiC MOSFET die as device deliverables. Additional Gen3 3.3kV/40mOhm SiC MOSFET die from these fabrication will also be utilized for the development of a prototype 3.3kV/10mOhm SiC MOSFET Half H-Bridge Module in Subtask 2.3.4.

Under Subtask 2.3.2 of this project, an optimized Gen3 10kV/350mOhm SiC MOSFET device design will be completed which includes efficient edge termination, reliable cell structure, and area optimization. Using this device design, Gen3 10kV/350mOhm SiC MOSFET fabrication lots will be carried out on 100mm 4HN-SiC wafers, and characterization of these devices will be carried out in order to establish a stable updated Gen3 10kV/350mOhm SiC MOSFETs manufacturing process. Utilizing Gen3 10kV/350mOhm SiC MOSFET characterization data from these fabrication lots, a preliminary device data sheet will be developed for Gen3 10kV/350mOhm SiC MOSFET die fabricated on 100mm 4HN-SiC wafers. These fabrication lots will also be used to provide Gen3 10kV/350mOhm SiC MOSFET die for high temperature reverse-bias (HTRB) testing per JEDEC guidelines (i.e., 77 devices from multiple fabrication lots for 1000 hours at T_a=150°C, V_{gs} = 0V and V_{ds} = 8000V, which is 80% of the rated blocking voltage), as well as provide two-hundred (200) engineering samples of Gen3 10kV/350mOhm SiC MOSFET die as device deliverables.

Under Subtask 2.3.3 of this project, an optimized 10kV/20A SiC JBS Diode device design will be completed which includes efficient edge termination and area optimization. Using this device design, 10kV/20A SiC JBS Diode fabrication lots will be carried out on 100mm 4HN-SiC wafers, and characterization of these devices will be carried out in order to establish a stable updated 10kV/20A SiC JBS Diode manufacturing process. Utilizing 10kV/20A SiC JBS Diode characterization data from these fabrication lots, a preliminary device data sheet will be developed for 10kV/20A SiC JBS Diode die fabricated on 100mm 4HN-SiC wafers. These fabrication lots will also be used to provide 10kV/20A SiC JBS Diode die for high temperature reverse-bias (HTRB) testing per JEDEC guidelines (i.e., 77 devices from multiple fabrication lots for 1000 hours at T_a=150°C, V_{gs} = 0V and V_{ds} = 8000V, which is 80% of the rated blocking voltage), as well as provide two-hundred (200) engineering samples of 10kV/20A SiC JBS Diode die as device deliverables.

Under Subtask 2.3.4 of this project, a prototype 3.3kV/10mOhm SiC MOSFET Half H-Bridge Module will be designed utilizing Gen3 3.3kV/40mOhm SiC MOSFETs from Subtask 2.3.1. Using this design, fifteen (15) prototype 3.3kV/10mOhm SiC MOSFET Half H-Bridge Modules will be assembled and characterized utilizing Gen3 3.3kV/40mOhm SiC MOSFETs from Subtask 2.3.1. Based upon this characterization data, a preliminary device data sheet will be developed for this prototype

3.3kV/10mOhm SiC MOSFET Half H-Bridge Module. Ten (10) of these prototype 3.3kV/10mOhm SiC MOSFET Half H-Bridge Module will be provided as deliverables.

Issues, Risks and Mitigations: Following completion of the 10kV/20A SiC JBS Diode Fabrication Lot #1, Lot #2, and Lot #3, and subsequent device characterization under Subtask 2.3.3, it was found that the 10kV/20A SiC JBS diode device from all three fabrication lots exhibited elevated reverse leakage currents (i.e., > 10 µA) at the designed 10 kV blocking voltage compared with the typical measured values for devices from other recent 10kV/20A SiC JBS diode fabrication lots. Analysis is currently underway to determine the cause of this observed elevated leakage current (i.e.,> 10 µA) at 10 kV blocking voltage for the 10kV/20A SiC JBS diodes from these first three fabrication lot under Subtask 2.3.3. Based upon this analysis, an improved manufacturable 10kV/20A SiC JBS diode fabrication process is being developed for better control of this 10 kV reverse leakage current for future 10kV/20A SiC JBS diode fabrication lots which will be completed under Subtask 2.3.3.

Although the devices from 10kV/20A SiC JBS Diode Fabrication Lot #1 exhibited elevated values for the 10kV reverse leakage current, these Lot #1 10kV/20A SiC JBS Diode devices were usable for an initial examination of the 10kV/20A SiC JBS diode device robustness under High Temperature Reverse Bias (HTRB) testing as well as validation of high voltage package robustness and the HTRB test system at Cree. As a result of initial HTRB testing of these Lot #1 10kV/20A SiC JBS diodes in high voltage packages, a limitation in the robustness of the silicone passivation gel in the high voltage package has been identified. Failure analysis of the 10kV/20A SiC JBS Diodes in high voltage packages following initial HTRB testing showed that this silicone passivation gel delaminates from the surface of the 10kV/20A SiC JBS Diode device die in the high voltage package. As a result of this delamination of the silicone gel from the device die, high voltage discharge occurs across the surface of the device termination during the HTRB testing.

In this initial HTRB testing of 10kV/20A SiC JBS Diodes in high voltage packages from Fabrication Lot#1, we divided eighty (80) device die into four (4) separate high voltage packaging assembly runs, each consisting of twenty (20) 10kV/20A SiC JBS Diode die in high voltage packages. During the initial HTRB testing of these Lot #1 10kV/20A SiC JBS Diode packaged devices, one (1) of the four (4) high voltage packaging assembly runs exhibited the eight (8) out of twenty (20) packaged device failures. However the other three high voltage packaging assembly runs exhibited at most only one (1) of twenty (20) packaged device failures during the initial HTRB testing of these Lot #1 10kV/20A SiC JBS Diode packaged devices.

Because all of the 10kV/20A SiC JBS diodes were fabricated in the same Fabrication Lot #1, this disparity in the failure rate for different high voltage packaging assembly runs strongly suggests that these HTRB failures are most likely associated the high voltage packaging process and probably not be indicative of HTRB failures of the 10kV/20A SiC JBS diode devices themselves. Furthermore, subsequent examination and analysis of the high voltage packaged 10kV/20A SiC JBS diode devices that failed under initial HTRB testing demonstrated that the failures did indeed result from a high voltage discharge across the surface of the device termination which could arise due to delamination of the silicone passivation gel. This indicates that there is a weakness with

the silicone gel passivation potting process that was used during the assembly of the 10kV/20A SiC JBS diode high voltage packages. In order to address this silicone gel passivation delamination issue, we are currently examining the quality of a more manufacturable and reliable silicone gel passivation process utilized by team members at the Cree-Fayetteville facility for use in future high voltage packaging assembly of all of the 3.3kV and 10kV SiC devices being developed and undergoing HTRB testing on this program under Task 2.3.

Significant Accomplishments:

Subtask 2.3.1 – Gen3 3.3kV/40mOhm SiC MOSFET and HTRB Qualification: A new optimized Gen3 3.3 kV/40mOhm SiC MOSFET device design has been completed which has resulted in an 8.5% reduction in die size and 13% reduction in the 25°C on-state resistance ($R_{DS,ON}$) compared to the legacy 3.3kV/47mOhm SiC MOSFET device design. Utilizing this new optimized device design, Gen 3.3kV/40mOhm SiC MOSFET Fabrication Lot#1 and Lot #2 have been completed along with device characterization. In addition, Gen3 3.3kV/40mOhm SiC MOSFET Fabrication Lot#3 is currently in process. The two successfully completed Gen3 3.3kV/40mOhm SiC MOSFET fabrication lots (i.e., Lot#1 and Lot #2) have validated the new optimized device design. A comparison of the Gen3 3.3kV/40mOhm SiC MOSFET device die layouts and the on-state resistance distributions for the legacy design and the new optimized design for the Gen3 3.3kV/40mOhm SiC MOSFET are shown in Figure 1. This shows the 8.5% reduction in die size and 13% reduction in the 25°C on-state resistance ($R_{DS,ON}$) of the new optimized Gen3 3.3 kV/40mOhm SiC MOSFET device compared to that of the legacy Gen3 3.3kV/47mOhm SiC MOSFET.

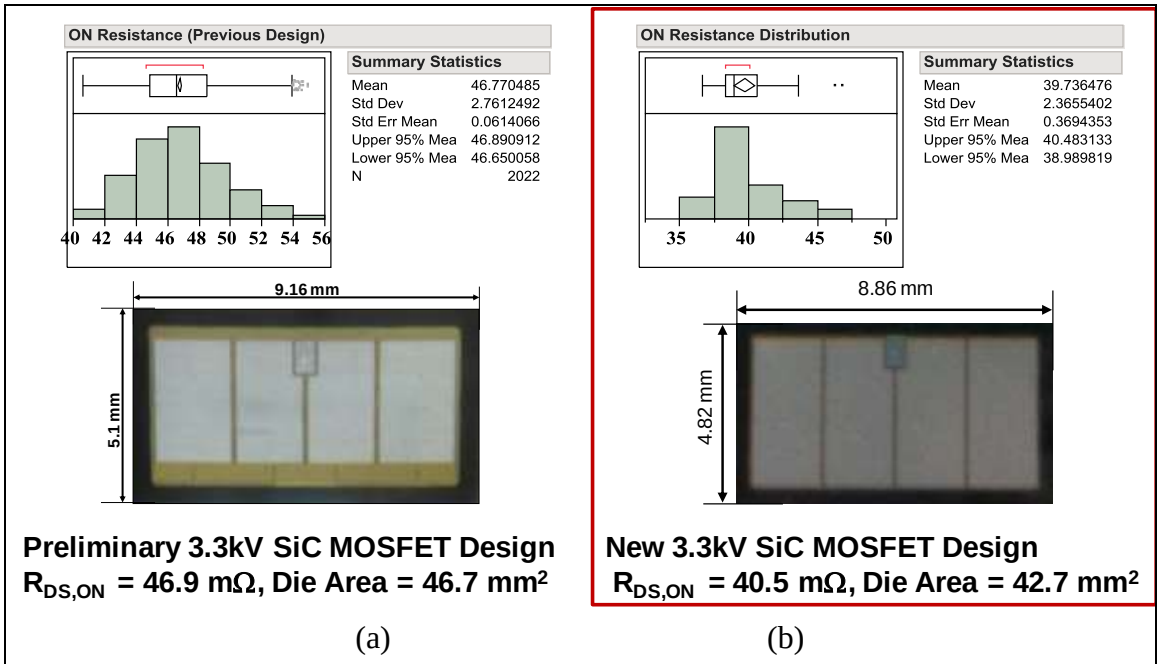


Figure 1. (a) Legacy design and (b) new optimized design (red boundary) of 3.3 kV/40mOhm SiC MOSFET device die layout reduced by 8.5% and 25C on-state resistance ($R_{DS,ON}$) reduced by 13% for the new optimized 3.3kV/40mOhm SiC MOSFET device design compared with the legacy 3.3kV/47mOhm SiC MOSFET device design.

The new optimized design Gen3 3.3kV/40mOhm SiC MOSFETs from Fabrication Lot #1 and Lot #2 are currently being prepared for high voltage packaging in preparation for HTRB testing in the HTRB test system at Cree. As described in the earlier section on high voltage packaging of 10kV/20A SiC JBS diodes, the best known silicone gel passivation practice currently being investigated using the facilities at Cree-Fayetteville will be implemented in the high voltage packaging of these Gen3 3.3kV/40mOhm SiC MOSFETs from Fabrication Lot #1 and Lot #2 for HTRB testing.

Subtask 2.3.2 – Gen3 10kV/350mOhm SiC MOSFET and HTRB Qualification: A new optimized Gen3 10 kV/350mOhm SiC MOSFET device design has been completed which has a long-MOS-channel design for improved circuit performance and robustness. This long-MOS-channel design for this new Gen3 10kV/350mOhm SiC MOSFET has been implemented with no degradation in the on-state performance of the device. This new long-MOS-channel Gen3 10kV/350mOhm SiC MOSFET design does result in a device with a threshold voltage of ~ 4V, which is 1.5V higher than the legacy Gen3 10kV/350mOhm SiC MOSFET with the standard-MOS-channel length design.

Utilizing this new optimized long-MOS-channel device design, Gen3 10kV/350mOhm SiC MOSFET Fabrication Lot#1 has been completed along with device characterization. In addition, Gen3 10kV/350mOhm SiC MOSFET Fabrication Lot#1 is currently underway using this new long-MOS-Channel design. Figure 2 shows the distributions in on-state resistance ($R_{DS,ON}$) and threshold voltage (V_T) for the functional Gen3 10kV/350mOhm SiC MOSFETs from Fabrication Lot #1. As shown in Figure 2, the mean on-state resistance ($R_{DS,ON}$) is 364mOhm and the mean threshold voltage (V_T) is 4.1 V for the Gen3 10kV/350mOhm SiC MOSFET from Fabrication Lot#1.

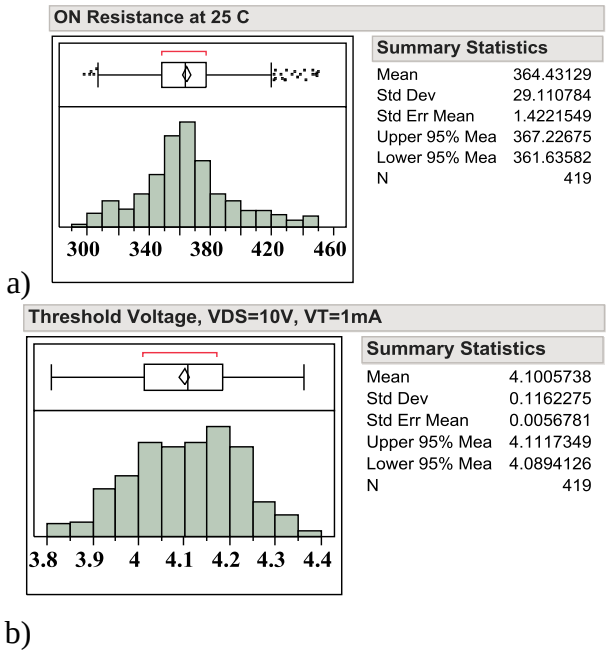


Figure 2. Distribution of the (a) on-state resistance ($R_{DS,ON}$) and (b) threshold voltage (V_T) values for the Gen3 10kV/350mOhm SiC MOSFETs from Fabrication Lot#1 showing a mean on-state resistance ($R_{DS,ON}$) of 364mOhm and the mean threshold voltage (V_T) of 4.1 V.

Subtask 2.3.3 - 10kV/20A SiC JBS Diode and HTRB Qualification: Design of the 10 kV/20A SiC MOSFET device has been completed. Utilizing this device design, 10kV/20A SiC JBS Diode Fabrication Lot #1, Lot #2, and Lot #3 have been completed along with device characterization. As discussed previously, it was found that the 10kV/20A SiC JBS diode device from all three fabrication lots exhibited elevated reverse leakage currents (i.e., > 10 µA) at the designed 10 kV blocking voltage compared with the typical measured values for devices from other recent 10kV/20A SiC JBS diode fabrication lots.

Figure 3 shows a comparison of a typical 10kV/20A SiC JBS diode blocking I-V curve from these three fabrication lots on this Power America program with that from a typical legacy device from another recent 10kV/20A SiC JBS diode fabrication lot. Although the breakdown voltage is in excess of 10kV for both devices, the 10kV/20A SiC JBS diode fabricated in Lot #1, Lot #2, and Lot#3 have reverse leakage currents that are approximately three orders of magnitude higher than those from other recently fabricated 10kV/20A SiC JBS diodes.

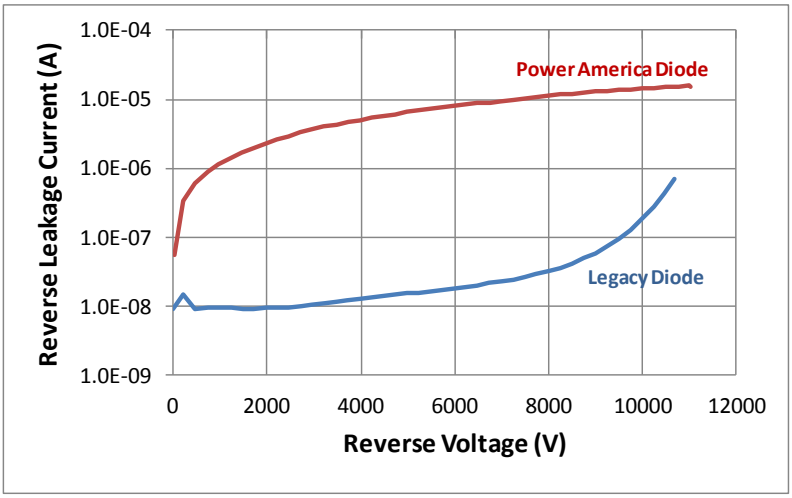


Figure 3. Typical 10kV/20A SiC JBS diode blocking I-V curve from first three Power America fabrication lots compared with that from a typical legacy device from another recent 10kV/20A SiC JBS diode fabrication lot

Analysis is currently underway to determine the cause of this observed elevated leakage current (i.e.,> 10 µA) at 10 kV blocking voltage for the 10kV/20A SiC JBS diodes from these first three fabrication lot under Subtask 2.3.3. Based upon this analysis, an improved manufacturable 10kV/20A SiC JBS diode fabrication process is being developed for better control of this 10 kV reverse leakage current for future 10kV/20A SiC JBS diode fabrication lots which will be completed under Subtask 2.3.3.

Although the devices from 10kV/20A SiC JBS Diode Fabrication Lot #1 exhibited elevated values for the 10kV reverse leakage current, these Lot #1 10kV/20A SiC JBS Diode devices were usable for an initial examination of the 10kV/20A SiC JBS diode device robustness under High Temperature Reverse Bias (HTRB) testing as well as validation of high voltage package robustness and the HTRB test system at Cree. As a result of initial HTRB testing of these Lot #1 10kV/20A SiC JBS diodes in high voltage

packages, a limitation in the robustness of the silicone passivation gel in the high voltage package has been identified. Failure analysis of the 10kV/20A SiC JBS Diodes in high voltage packages following initial HTRB testing showed that this silicone passivation gel delaminates from the surface of the 10kV/20A SiC JBS Diode device die in the high voltage package which high voltage discharge occurs across the surface of the device termination during the HTRB testing. In order to address this silicone gel passivation delamination issue, we are currently examining the quality of a more manufacturable and reliable silicone gel passivation process utilized by team members at the Cree-Fayetteville facility for use in future high voltage packaging assembly of all of the 3.3kV and 10kV SiC devices being developed and undergoing HTRB testing on this program under Task 2.3.

Subtask 2.3.4 - 10kV/20A SiC JBS Diode and HTRB Qualification: A preliminary design of the prototype Gen3 3.3kV/10mOhm SiC MOSFET Half H-Bridge Module has been completed based upon an existing 62 mm x 106 mm x 30 mm module platform. An alternative approach is being investigated using a Cree-Fayetteville design for the prototype Gen3 3.3kV/10mOhm SiC MOSFET Half H-Bridge Module.

Technology to Market: Cree is currently a world leader in the development of medium voltage (i.e., 3.3kV to 10kV) SiC power technology. Cree has been actively developing a variety of medium voltage SiC power device technologies for several years including 3.3kV SiC MOSFETs, 6.5kV SiC MOSFETs, 10kV SiC MOSFETs and 10kV SiC JBS diodes. In addition, Cree and Cree-Fayetteville are currently developing both 3.3kV SiC MOSFET modules and 10kV SiC MOSFET modules.

Cree has had numerous discussions and is continuing to work closely with multiple major companies regarding applications that will utilize medium voltage (i.e., 3.3kV to 10kV) SiC power technology. There is rapidly growing interest in 3.3kV SiC power devices and modules for a number of 3.3kV medium voltage power applications for rail traction, medium voltage motor drives, solar inverters, and UPS systems. There is also a substantial interest in 10kV SiC power devices and modules for several 10kV medium voltage power applications including medium voltage motor drives, grid-tied solar converters, solid-state transformers, HVDC systems, and power distribution in factories and data-centers.

Cree has an established SiC power device and power module production capability for SiC power technology that will enable the expeditious development of manufacturable 3.3kV and 10kV SiC power technologies for qualification leading to early commercial release of 3.3kV and 10kV SiC power devices. The HTRB qualification of 3.3kV SiC MOSFETs, 10kV SiC MOSFETs, and 10kV SiC JBS diodes per JEDEC guidelines under Task 2.3 of this program is a critical first stage in the qualification of these 3.3kV and 10kV SiC power device technologies leading to their release as commercial products.

Cree is a world leader in commercial production and distribution of SiC power device and module products. As a result, Cree has established distribution channels that will be utilized for 3.3kV and 10kV SiC power devices and modules. Cree will interface and sell 3.3kV SiC MOSFETs, 10kV SiC MOSFETs, and 10kV SiC JBS diodes directly to medium voltage module manufacturers and through commercial die distributors. Cree will also work with team members at Cree-Fayetteville to produce commercially released 3.3kV and 10kV SiC MOSFET power modules.

Plans for Next Budget Period If Funded: During the next budget period, Cree is planning to continue development of manufacturable and reliable Gen3 3.3kV/40mOhm SiC MOSFET and Gen3 10kV/350mOhm SiC MOSFET device technologies, ultimately leading to commercially released Gen3 3.3kV/40mOhm SiC MOSFET and Gen3 10kV/350mOhm SiC MOSFET device products. Cree will carry out further reliability qualification per JEDEC guidelines for these Gen3 3.3kV/40mOhm SiC MOSFET devices and Gen3 10kV/350mOhm SiC MOSFET devices fabricated by Cree including:

1) High Temperature Gate Bias (HTGB) testing of Gen3 3.3kV/40mOhm SiC MOSFETs and Gen3 10kV/350mOhm SiC MOSFETs to evaluate the device gate oxide reliability and threshold voltage stability under the maximum recommended gate oxide electric field and device operating temperature;
2) Thermal Shock (TS) testing of Gen3 3.3kV/40mOhm SiC MOSFETs and Gen3 10kV/350mOhm SiC MOSFETs to evaluate the device and die attach fatigue reliability under temperature cycling conditions ranging from the minimum to the maximum recommended case temperature;
3) Constant voltage Time Dependent Dielectric Breakdown (TDDB) testing of Gen3 3.3kV/40mOhm SiC MOSFETs and Gen3 10kV/350mOhm SiC MOSFETs to assess gate oxide wear-out reliability of these devices;
4) Electrostatic Discharge (ESD) testing of Gen3 3.3kV/40mOhm SiC MOSFETs and Gen3 10kV/350mOhm SiC MOSFETs for the human body model (HBM) and charged device model (CDM) testing modes; and
5) Gen3 3.3kV/40mOhm SiC MOSFET and Gen3 10kV/350mOhm SiC MOSFET device Body Diode High Temperature Operating Lifetime (BD-HTOL) testing to evaluate the reliability of the Body Diode during third-quadrant operation of these devices.

As part of this project for the next year to develop manufacturable and reliable Gen3 3.3kV/40mOhm SiC MOSFETs and Gen3 10kV/350mOhm SiC MOSFETs, Cree will fabricate and characterize the devices needed for the HTGB, TS, TDDB, and BD-HTOL reliability qualification testing described previously. In addition, Cree will provide two-hundred (200) Gen3 3.3kV/40mOhm SiC MOSFETs and one-hundred (100) Gen3 10kV/350mOhm SiC MOSFETs as a combination of device die and packaged devices for the Power America device bank. Cree will also establish 1000-unit budgetary pricing for these Gen3 3.3kV/40mOhm SiC MOSFETs and Gen3 10kV/350mOhm SiC MOSFETs for select customers including Institute partners. Cree will also develop a prototype datasheet for these Gen3 3.3kV/40mOhm SiC MOSFETs and Gen3 10kV/350mOhm SiC MOSFETs.

Project Output: Thus far during the course of this program, there have been no publications, conference presentations, IP disclosures, or Patent filings have yet been completed regarding the development and HTRB qualification of 3.3kV SiC MOSFETs, 10kV SiC MOSFETs, 10kV SiC JBS diodes or 3.3kV SiC Modules under this program.

Milestone Summary

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
2.3.1.1	3.3kV/40mOhm SiC MOSFET Design Completed	5/31/2015	Completed - 3.3kV/40mOhm SiC MOSFET Mask and Epi Design
2.3.1.2	3.3kV/40mOhm SiC MOSFET Fab Lot #1 Completed	8/31/2015	Completed - 3.3kV/40mOhm SiC MOSFET Fab Lot #1 and Lot #2
2.3.1.3	3.3kV/40mOhm SiC MOSFET Concept Datasheet Completed	11/30/2015	Incomplete - Concept Datasheet To Be Completed by 12/10/15.
2.3.1.4	3.3kV/40mOhm SiC MOSFET Preliminary Datasheet Completed & 1000 Unit Price $330/Die	4/30/2016	Incomplete – Preliminary Datasheet Development and Pricing Analysis Underway
2.3.1.5	HTRB Testing Completed for 3.3kV/40mOhm SiC MOSFET	4/30/2016	Incomplete – Packaging 3.3kV/40mOhm SiC MOSFET for HTRB Testing
Go/No-Go 2.3.1	HTRB Testing and Announce Availability Engineering Sample 3.3kV/40mOhm SiC MOSFET	4/30/2016	Incomplete – Packaging 3.3kV/40mOhm SiC MOSFET for HTRB Testing
2.3.2.1	10kV/350mOhm SiC MOSFET Design Completed	5/31/2015	Completed - 10kV/350mOhm SiC MOSFET Mask and Epi Design
2.3.2.2	10kV/350mOhm SiC MOSFET Fab Lot #1 Completed	8/31/2015	Completed - 10kV/350mOhm SiC MOSFET Fab Lot #1
2.3.2.3	10kV/350mOhm SiC MOSFET Concept Datasheet Completed	11/30/2015	Incomplete - Concept Datasheet To Be Completed by 12/10/15

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
2.3.2.4	10kV/350mOhm SiC MOSFET Preliminary Datasheet Completed & 1000 Unit Price $750/Die	4/30/2016	Incomplete – Preliminary Datasheet Development and Pricing Analysis Underway
2.3.2.5	HTRB Testing Completed for 10kV/350mOhm SiC MOSFET	4/30/2016	Incomplete – Packaging 10kV/350mOhm SiC MOSFET for HTRB Testing
Go/No-Go 2.3.2	HTRB Testing and Announce Availability Engineering Sample 10kV/350mOhm SiC MOSFET	4/30/2016	Incomplete – Packaging 10kV/350mOhm SiC MOSFET for HTRB Testing
2.3.3.1	10kV/20A SiC JBS Diode Design Completed	5/31/2015	Completed - 10kV/20A SiC JBS Diode Mask and Epi Design
2.3.3.2	10kV/20A SiC JBS Diode Fab Lot #1 Completed	8/31/2015	Completed - 10kV/20A SiC JBS Diode Fab Lot #1, Lot #2, and Lot#3. Addressing Issue of Elevated Reverse Leakage Current at 10kV for Future Lots.
2.3.3.3	10kV/20A SiC JBS Diode Concept Datasheet Completed	11/30/2015	Incomplete - Concept Datasheet To Be Completed by 12/10/15.
2.3.3.4	10kV/20A SiC JBS Diode Preliminary Datasheet Completed & 1000 Unit Price $300/Die	4/30/2016	Incomplete – Preliminary Datasheet Development and Pricing Analysis Underway
2.3.3.5	HTRB Testing Completed for 10kV/20A SiC JBS Diode	4/30/2016	Incomplete – Initial HTRB Testing of 10kV/20A SiC JBS Diode From Lot #1 Showed Packaging Issue. Developing Improved High Voltage

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
			Packaging for HTRB Testing of 3.3kV & 10kV SiC MOSFETs and JBS Diodes.
Go/No-Go 2.3.3	HTRB Testing and Announce Availability Engineering Sample 10kV/20A SiC JBS Diode	4/30/2016	Incomplete – Initial HTRB Testing of 10kV/20A SiC JBS Diode From Lot #1 Showed Packaging Issue. Developing Improved High Voltage Packaging for HTRB Testing of 3.3kV & 10kV SiC MOSFETs and JBS Diodes.
2.3.4.1	Preliminary Design of 3.3kV/10mOhm SiC MOSFET Half H-Bridge Module Completed	5/31/2015	Completed - Preliminary Design of 3.3kV/10mOhm SiC MOSFET Half H-Bridge Module Using Existing 62mm x 106 mm x 30 mm Module.
2.3.4.2	Assembly & Characterization of Initial Prototype 3.3kV/10mOhm SiC MOSFET Half H-Bridge Module Completed	8/31/2015	Incomplete - Assessing Alternative Approach Using Cree-Fayetteville Design to Assemble 3.3kV/10mOhm SiC MOSFET Half H-Bridge Module
2.3.4.3	Assembly & Characterization of 7 Prototype 3.3kV/10mOhm SiC MOSFET Half H-Bridge Module Completed	11/30/2015	Incomplete - Assessing Alternative Approach Using Cree-Fayetteville Design to Assemble 3.3kV/10mOhm SiC MOSFET Half H-Bridge Module
2.3.4.4	Assembly & Characterization of 7 Prototype 3.3kV/10mOhm SiC	4/30/2016	Incomplete - Assessing Alternative Approach Using Cree-Fayetteville Design to Assemble

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
	MOSFET Half H-Bridge Module Completed		3.3kV/10mOhm SiC MOSFET Half H-Bridge Module
2.3.4.5	Preliminary Datasheet of Prototype 3.3kV/10mOhm SiC MOSFET Half H-Bridge Module Completed	4/30/2016	Incomplete - Assessing Alternative Approach Using Cree-Fayetteville Design to Assemble 3.3kV/10mOhm SiC MOSFET Half H-Bridge Module
Go/No-Go 2.3.5	Announce Availability of Prototype 3.3kV/100mOhm SiC MOSFET Half H-Bridge Module & Budget Pricing of $5,500/Module	4/30/2016	Incomplete - Assessing Alternative Approach Using Cree-Fayetteville Design to Assemble 3.3kV/10mOhm SiC MOSFET Half H-Bridge Module

Organization: Delphi Automotive, LLC
Task No./Project Title: Task 4.5 WBG Power Semiconductor Device Packaging and Characterization
Technical Point of Contact: Monty B. Hayes
Sub-award start date: 02/01/15

Project Objectives: The purpose of this development is to apply the Delphi Development Process to develop a boosted and/or non-boosted Traction Drive Inverter for Light-Duty and/or Heavy-Duty Electric Drive Vehicle (EDV) platforms applying advanced wide bandgap (WBG) power semiconductor devices to improve the electrified powertrain's system efficiency, while reducing its cost and size (overall space-claim/volume and weight) compared with current state-of-the-art inverters. The learning from this development will also be applicable to adjacent products and markets such as other transportation platforms (e.g., aerospace) and other power conversion applications (e.g., industrial AC motor drives). Delphi will work with OEM(s) to develop a system-level specification for development of the subsystem and its components for production. This development will target Model Year 2020 for market introduction, with an assumed start date of January 1, 2015 for the development process. The activity will support the development of an inverter utilizing a WBG switch and diode, as well as comparison to inverters with best-in-class Silicon IGBTs and a WBG diode as a baseline for evaluating the benefits of the all-WBG inverter. While the exact specification for the all-WBG inverter system will be finalized after further discussion with OEMs, for the boosted system, the initial input voltage for the inverter will be 200V – 430V with a boosted output target of 360V – 650V, depending on vehicle platforms targeted. The inverter design is targeted to be a liquid-cooled inverter with 75°C coolant; however, during the specification and design phase, 105°C coolant and air-cooled thermal solutions will also be considered. The development will target 55 – 120 kW electrified systems. The effort in Budget Period 1 will focus on developing the specification with the OEM customer, selection of the WBG device to best meet the requirements of the OEM customer platforms, concepts for the component packaging for the application, and design of the packaging and characterization of the chosen concept. The subtasks shown below outline the various tasks that will be undertaken to develop the packaged WBG device for the Traction Drive WBG Inverter.

Summary: The objectives of the subtasks of Task 4.5 in Budget Period 1 will be to develop the inverter specification based on working with OEM customers, selection of the appropriate WBG device, conception, design and down-selection of appropriate packaging for the chosen WBG power device, and build, test and characterization of the packaged devices.

Project's Contribution to PowerAmerica Mission: This project supports the PowerAmerica mission for technology advancement in the area of power semiconductor devices for the transportation sector including US job growth, supply chain development and US job growth. The technologies developed in the activity will support product development for traction drive inverter products manufactured in Kokomo, Indiana. The project will also contribute to the following:

- Reduction of energy losses over vehicle drive cycle
- Reduction of system cost and size/weight, compared to state-of-the-art Si IGBT devices
- Commercialization of WBG devices for automobiles and light-duty trucks, and potentially other applications
- Helping to drive demand for WBG devices by lowering system cost compared to

Si devices
- Creating additional US jobs by growth of electrification products manufactured in the U.S.
- US job growth via development of skilled US work force and supply chain for power electronics
- Providing opportunities for internships and workforce development related to the manufacturing of power electronics products in the US for vehicle electrification globally

Technical Approach:
Subtask 4.5.1.1: *Analyze/Develop System Level OEM Specifications*
Work with vehicle OEM(s) to analyze vehicle specifications for the targeted application. This study will result in the targeted design specifications for the component product for the targeted application. This may include analysis and simulation. It is anticipated that the design will focus on volume and mass benefits, including power level, steady-state operating current and specification for worst case current based on vehicle and motor parameters such as stall, etc. The developed specifications will also be in line with DOE 2020 inverter targets. The system will target 55-120 kW power.

Subtask 4.5.1.2: *Investigate Topology with Power Semiconductor Device Supplier*
Working with the power semiconductor device supplier and OEM as applicable, investigate and identify the best topology/approach for the targeted vehicle application, including the targeted WBG power semiconductor device technology.

Subtask 4.5.1.3: *Power Semiconductor Device Selection and Design*
Choose power semiconductor devices. While the goal of the activity is not to develop new semiconductor technologies, the die layout may need to be changed for the chosen packaging technologies/design. Target equivalent RDSon is <10-17 mΩ for a single device and 2-3 mΩ for a paralleled solution.

Subtask 4.5.1.4: *Power Semiconductor Device Packaging and Characterization*
Develop the design/concept for the WBG packaging, fabricate the developed package, characterize statically and dynamically the packaged device, including loop inductance performance. The targeted device for characterization will be a Half-H Bridge implementation with a top and bottom switch.

Issue, Risks and Mitigations: There are no known major risks to the development of the WBG packaging and inverter component, but overall in the marketplace there is risk associated with the development of low cost WBG devices capable of carrying large currents and being competitive with silicon based devices. For automotive products in particular, low enough cost to be competitive will require WBG devices that can be manufactured in larger volumes and are proven reliable in the automotive environment.

Significant Accomplishments
Subtask 4.5.1.1: *Analyze/Develop System Level OEM Specifications*

Delphi has held discussions with various OEMs and has developed initial performance specifications for traction drive inverter systems. We need to further compare the chosen specification with inverter systems from other OEMs to be sure that the chosen specifications can meet the needs of multiple customers. For the targeted system, Delphi has developed an initial volume claim for a traction drive inverter system. Based on the continued design effort, Delphi will further define the inverter design targets.

Subtask 4.5.1.2: *Investigate Topology with Power Semiconductor Device Supplier*
Delphi has discussed with OEM and semiconductor vendors topology and approach for boosted and non-boosted systems.

Subtask 4.5.1.3: *Power Semiconductor Device Selection and Design*
Delphi has discussed next generation devices with vendors. Delphi received agreement from DOE's Steven Boyd, Cree and other team members of Ford and APEI for Delphi to receive parts from another DOE program, to evaluate and package for this one.
Delphi received the 900V devices from Cree and is in the process of building these bare die into a Single Chip Module that we utilize to characterize bare die performance. Delphi will be statically and dynamically characterizing the die performance over the next few weeks and will provide the characterization results to the Cree, APEI and Ford team. Delphi is also investigating sintering the die for the chosen package design. In addition, Delphi has had discussion with various SiC device manufacturers to evaluate their current offerings and potential to be able to dual-side cool the various die. In order to utilize these devices in a dual-side cooled package, Delphi will need to have either a top side solderable or sinterable interconnect.

Subtask 4.5.1.4: *Power Semiconductor Device Packaging and Characterization*
Design work continues on the dual-side cooled package and parts will be fabricated, built and characterized over the next few months.

Technology to Market: This project is to develop and demonstrate a power semiconductor device that can be used in traction drive inverter applications meeting DOE 2020 targets and OEM platform requirements for automotive EDV propulsion systems, resulting in a considerably more compact (smaller and lighter) and more energy efficient inverter and associated cooling system that is potentially lower cost as well, when produced in high volumes. While the primary targeted application is inverters for EDVs, this technology is also applicable in adjacent products such as DC/DC converters and chargers, as well as in adjacent markets, such as industrial AC motor drives. Inverters and converters are required for all levels of vehicle electrification, from HEVs to plug-in HEVs (PHEVs) and fully electric battery or fuel cell EVs. Inverters are a critical product in Delphi's Power Electronics product line portfolio, representing over 50% of the revenue plan. Likewise, since inverters are a key element in the global electrified vehicle market space, they represent a strategic component in Delphi's future business growth plan.

Together with DOE's support, Delphi has created a globally competitive U.S. Power Electronics engineering and volume production base in Kokomo, Indiana to compete effectively for the high value-adding, high-tech engineering and production jobs

that will relate to vehicle electrification globally going forward. Such investment is also key to continued growth in the Electrification market globally, by helping to drive the adoption of this new, more energy efficient and cleaner energy technology in the automotive marketplace, by improving overall cost-effectiveness and value for the user.

Plans for the Next Budget Period If Funded: Delphi was not chosen to receive any additional funds in the next budget period.

Project Output: The expected output of this work is a packaged WBG power semiconductor device.

Milestone Summary

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
M4.5.1	OEM Customer Specifications	12/31/2015	In process. Delphi has held discussions with various OEMs and has developed initial performance specifications for traction drive inverter systems for a MY2020 program. We need to further compare the chosen specification with inverter systems from other OEMs to be sure that the chosen specifications can meet the needs of multiple customers. For the targeted system, Delphi has developed an initial volume claim for a traction drive inverter system. Based on the continued design effort, Delphi will further define the inverter design targets.
M4.5.2	Detailed Device Specification	12/31/2015	In process. Delphi is developing the detailed device drawing/specifications. Delphi is behind in the detailed drawing and specifications, but the plan is to complete in time to support the build and characterization.
M4.5.3	Package Layout and Design Complete	03/31/2016	In process. Delphi received the 900V devices from Cree to characterize bare die performance. Delphi has built test fixtures and has statically and dynamically characterized the die performance has provided the characterization results to the Cree, APEI and Ford

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
			team. Delphi is investigating sintering the die for the chosen package design. In addition, Delphi has had discussion with various SiC manufacturers to evaluate their current offerings and potential to be able to dual-side cool the various die. In order to utilize these devices in a dual-side cooled package Delphi will need to have either a top side solderable or sinterable interconnect. Concept work continues on the dual-side cooled package with a plan to finish the activity and build parts for characterization.
M4.5.4	Build, Test and Characterization of Device	03/31/2016	In process. Design work continues on the dual-side cooled package and parts will be fabricated, built and characterized over the next few months.

Organization: Florida State University
Task No./Project Title: Task 4.1 PV Converter development R&D
Technical Point of Contact: Dr. Hui “Helen” Li Email: hli@caps.fsu.edu
Sub-award start date: 02/01/2015

Project Objectives: This project will build and demonstrate a first generation 50 kW transformerless PV inverter towards achieving the goal of 50% smaller and lighter than the equivalent systems by utilizing higher frequency and higher temperature attributes of WBG devices. The converter topology, modulation control and filter will be designed to achieve targeted efficiency ($\geq 98\%$) and power density ($\geq 1\ kw/kg\ , 8\ w/in^3$). Solutions to leakage current suppression and other possible issues that result from fast switching of SiC device will be also investigated to enable the technology to be quickly transferred to new generation commercial PV converters. Therefore this project is able to accelerate the commercial availability of SiC based PV converters to compete with current PV converters using Si device.

Project's Contribution to the PowerAmerica Mission: This project demonstrates the potential and passway of using SiC device to improve the power density and efficiency of commercial grid-tied PV converters. By using 1.2 kV SiC MOSFETs, the cost of SiC PV converters will be comparable with Si based peers. Transformerless PV converters have a large and steady growing commercial markets. As SiC transformerless PV converters have been researched worldwide recently and on the product road map of main PV converter manufactures, this project aims to provide commercial viable technologies to increase U.S. competitiveness and technical leadership in global PV converter markets as well as to create more job opportunities. In addition, this project also contribute in the workforce development by educating graduate students with WBG device characteristics and WBG converter circuit design and system design training.

Technical Approach: Fast switching of SiC device not only affects efficiency and power density, it also affects control, power quality and other system aspects of a PV converter. In order to design a SiC PV converter that can maximize the advantages of SiC device, an integrated system design approach has been developed. It is shown in Fig.1 where the power density, efficiency, stability, total harmonic distortion and leakage current are the main design targets, the design aspects including controller, switching frequency, modulation method, switching frequency related to these design targets will be evaluated in a system level instead of separately. For example, the filter size can be reduced by a higher switching frequency and good modulation methods, however, the reduced filter may cause the system unstable. By utilizing this integrated system design approach, the filter size can be derived with design of switching frequency, controller and modulation together to meet those design aspects instead of satisfying power density requirement only. With this integrated design method, current transformerless PV converter topologies have been investigated and compared with SiC device has been applied. The research finds that as switching frequency increases, the widely adopted LCL filter based PV converter has less power density advantage versus single L filter based PV converter. This is because the heat generated by high frequency flux change in the inverter side inductor requires a large surface area to dissipate. In order to reduce filter further but maintain THD < 3%, an interleaved 5-level PV converter has been developed which can use 1200V SiC MOSFETs and meet all the required design aspects including high power density.

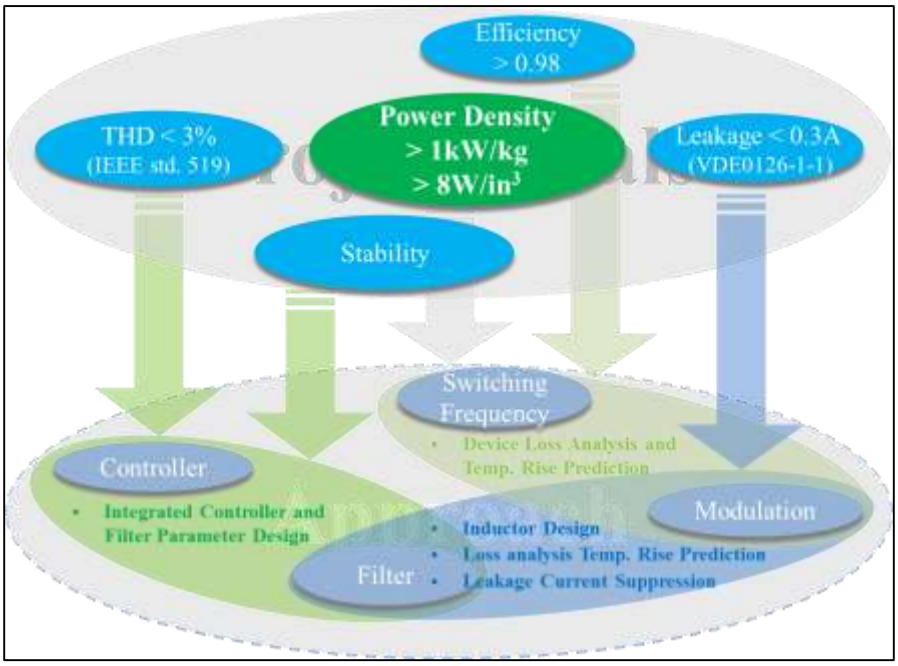


Fig. 1. Proposed integrated design approach for SiC based PV converter

Issues, Risks and Mitigations: One major issue of SiC based PV converter is the CPU speed of digital controller due to the switching frequency of proposed SiC PV converter is about 5 time faster compared with Si peers with same function. The calculation task remains same but the time for calculation is much smaller. In addition, there is need to control the converter every half switching cycle for our proposed topology. This issue will be solved by using DSP + FPGA structure. However the communication between DSP and FPGA will cost extra CPU time, which leaves little margin for additional algorithm. A new modulation method is currently under development to release some of DSP calculation burden to FPGA. Another issue is the internal EMC and cross coupling due to fast switching of SiC devices. The false triggering issue has been found in the testing of converter operation and has been solved by modifications on the drive circuit design. A new protection circuit is under development to solve the false protection. In addition, alternative signal isolation method is under investigation to solve DSP reboot triggered by internal EMI noise.

Significant Accomplishments:
A magnetic coupled five-level filter-less PV converter was developed: The principle of proposed topology to achieve high power density is not to filter out the harmonics but to cancel out the switching frequency harmonics. In this way there is no low frequency flux exists in the magnetic core so that the inductance can be made high enough to prevent high frequency loss. With this magnetic design, the proposed topology is a five-level filter-less inverter. When switching frequency or power rating increases, the proposed PV converter will gain more power density advantage versus LCL based PV converters. The advantages of proposed SiC PV converter can be summarized as follows:

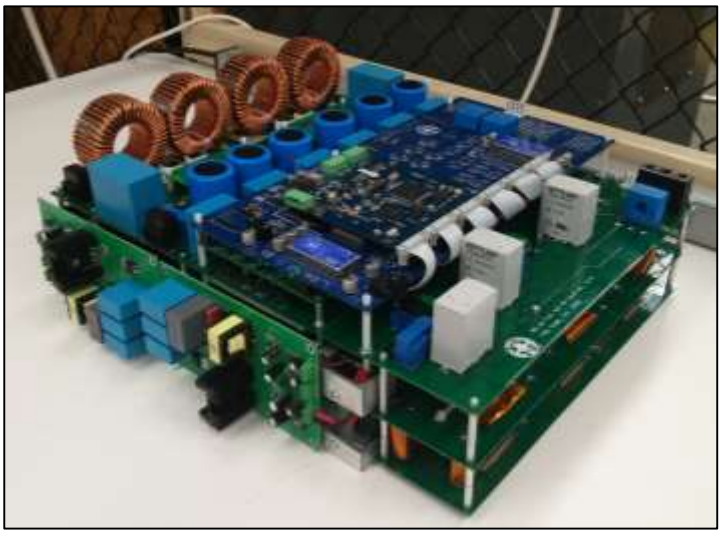
- Achieve filter-less because of 5-level output on grid side;

- Decouple winding loss and core loss of magnetic device, avoid over design of the magnetic components;
- More compact leakage current and EMI filters because the common mode voltage harmonics are decreased and moved to higher frequency range;
- Power density is more competitive under higher power rating (100kW-1MW);
- Power density increases with switching frequency.

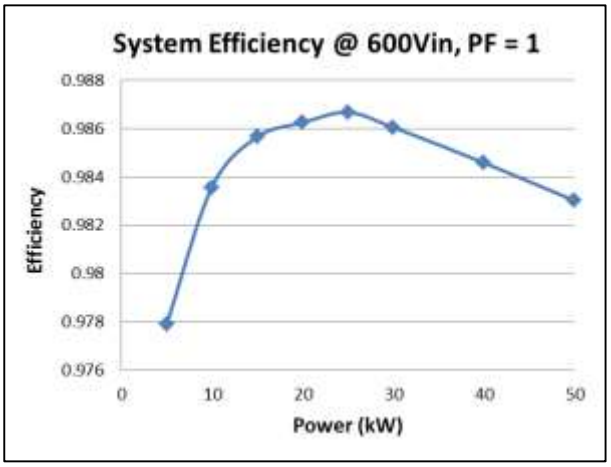
Therefore this PV converter has a brighter future than the LCL based PV converter in the SiC age.

Leakage current suppression method was developed: A ground leakage current suppression method was developed based common mode (CM) voltage spectrum analysis and a newly developed 5-level state-machine modulation. With proposed method, CM voltage source which generates leakage current has been controlled down to 40% compared with traditional three-level PV inverter, and the frequency for largest CM voltage harmonics has been doubled. The CM choke for leakage current suppression can be reduced by 88.6%.

A 50kW PV converter prototype was designed and assembled: A 50kW PV converter prototype was designed and assembled, as shown in Fig.2 (a). This prototype is still under test. The dimension of this prototype (without case) is 18.5” x 17” x 8”, and the weight is 45.4lb. The designed efficiency is shown in (b). The PV converter test bed is illustrated in (c) with measured switching waveforms in (d).



(a)



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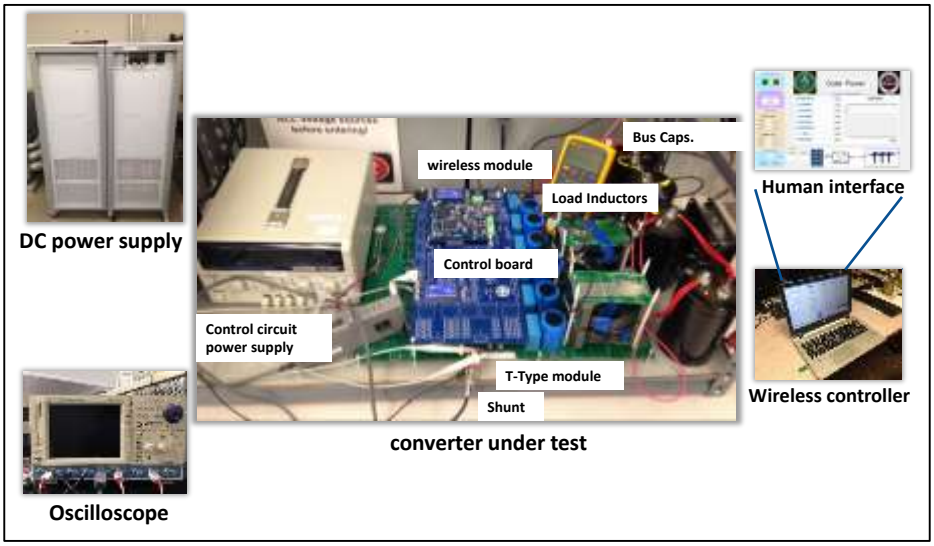
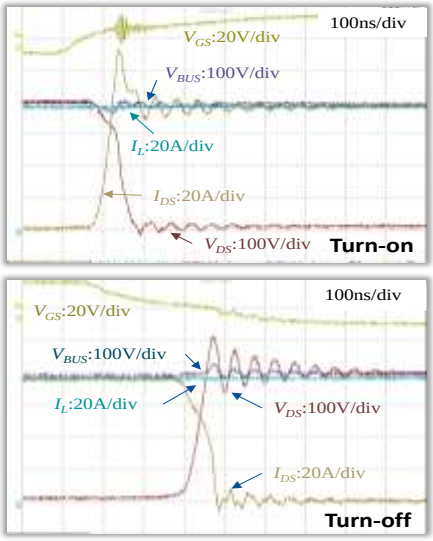


(c)



(d)

Fig. 2. (a) Developed 50kW PV converter prototype; (b) Calculated converter efficiency; (c) Converter test bed; (d) Measured switching waveforms.

Technology to Market: A decade ahead, SiC devices are believed to be the most profitable WBG device for commercial scale inverters. In the past decade, PV inverter industry has serious cost challenge from commodity prices. As the prices of major metal materials include copper, aluminum and steel have large fluctuations, PV inverter manufacturers tend to increase the switching frequency to reduce enclosure and magnetic size. If the increased switching frequency is achieved by Si devices, there will be penalties in thermal management cost and device reliability; more importantly, system

cost will be increased as when efficiency goes down, more PV panels are needed. By far, lots of major PV inverter manufacturers have engaged in the research and development of SiC based PV inverters, include: SMA, Phoenixtec, Danfoss, Mitsubishi, Delta, Siemens, Kaco, PowerOne, etc. For example, SMA has developed 10~20 kW SiC Sunny Tripower 20000TLHE-10 using Enhancement-mode SiC JFETs with T-type three level topology. The proposed research is on the same track with major PV inverter manufacturers, it is easier to transfer the technology. Also with the proposed technology, the advantages of SiC devices can be transferred to system level and become more profitable in the future. Manufacturers can benefit and adopt the proposed technology developed from different stages. The technology including the topology developed in year 1 can be transferred to PV converter manufacturers to improve their design to reach high efficiency and high power density. In addition, the proposed technology can be applied in their paralleled modular inverters, to replace the LCL filter. In this case, most of the development and manufacturer procedures do not need to change, and their products can be benefited with decreased size of power filter and increased stability.

Plans for Next Budget Period If Funded: In year 1 a magnetic coupled multilevel PV converter has been developed and built in the laboratory to demonstrate the operation. The proposed technology has received positive feedbacks from PV converter manufacturers for being technical promising and potential commercialization. In year 2, the PV converter power density and efficiency will be further improved, in addition, the EMI filter design will be also considered so the proposed technology can be pushed into commercial-ready status. Specifically, the boost inductor can be further decreased and the magnetic coupler developed in year 1 will integrate with the function of a passive common-mode (CM) inductor and an active CM filter in year 2. In addition, a control algorithm will be developed in year 2 to enable the PV converter to achieve 99% annual efficiency. In year 2 the education and workforce training will be enhanced by supporting more domestic undergraduate students to be involved in the project.

Project Output: One patent is under disclosure: A Magnetic Coupler with Integrated Hybrid Filter; One patent application on ground leakage current suppression will be filed in Jan. 2016 ; One conference paper will be submitted to ECCE 2016 and two conference papers will be submitted to APEC 2016;

Milestone summary (Include all BP 1 Milestones)

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
1.	Topology Development	4/30/2015	Complete
2.	Converter Paper Design	7/30/2015	Complete
3.	Ground Leakage Current Suppression Method	10/30/2015	Complete

Organization: GeneSiC Semiconductor Inc.
Task No./Project Title: Transfer of 1.2 kV diode process to a 150 mm Foundry line for Commercialization
Technical Point of Contact: Ranbir Singh, PhD
Sub-award start date: 02/01/2015

Project Objectives: The goal of this task is to transfer processes for fabricating 1.2 kV currently used in a 100 mm process line to the PowerAmerica Institute 150 mm foundry. Establishing manufacturable fabrication processes will accelerate the commercialization and volume production of 1.2kV/10 Amp diodes and allow the Institute member to assess the viability of using the foundry to produce other SiC devices such as diodes with higher voltages. Engineering samples of the 1.2 kV diodes will be provided to the Institute and its members for characterization, testing, and other feedback.

1. Transfer of 1.2kV diodes processes to 150 mm wafer foundry.
2. Benchmark device characteristics and yields between established 100mm process and the transferred 150mm process at X-Fab.
3. Fabrication, characterization, and process optimization for volume production of 1.2kV diodes
4. Provide engineering sample die and discrete packaged for Institute and commercialization partners

Project's Contribution to the PowerAmerica Mission: The cost of production of semiconductor discrete devices is often determined by:

1. Size of the wafers used in their manufacture
2. Modularization and repeatability of unit steps used, so that they can be implemented by low-cost personnel
3. Capital depreciation costs of semiconductor foundry equipment

PowerAmerica foundry partner (X-Fab) utilizes the 150mm wafers for manufacture of devices, which is larger than 100mm wafers presently used by all SiC device manufacturers. Since processing costs are roughly same between 100mm and 150mm epiwafers, and the number of chips in a 150mm epiwafer are about 2.25X larger than 100mm epiwafers, the cost of manufacturing per die is lowered by corresponding factor. Further, X-fab uses highly depreciated Silicon foundry with TS16949 quality system to ensure high level in process confidence. This allows the use of technicians, rather than expensive R&D staff to handle wafers. This is expected to reduce the cost of manufacture, and increase device yields.

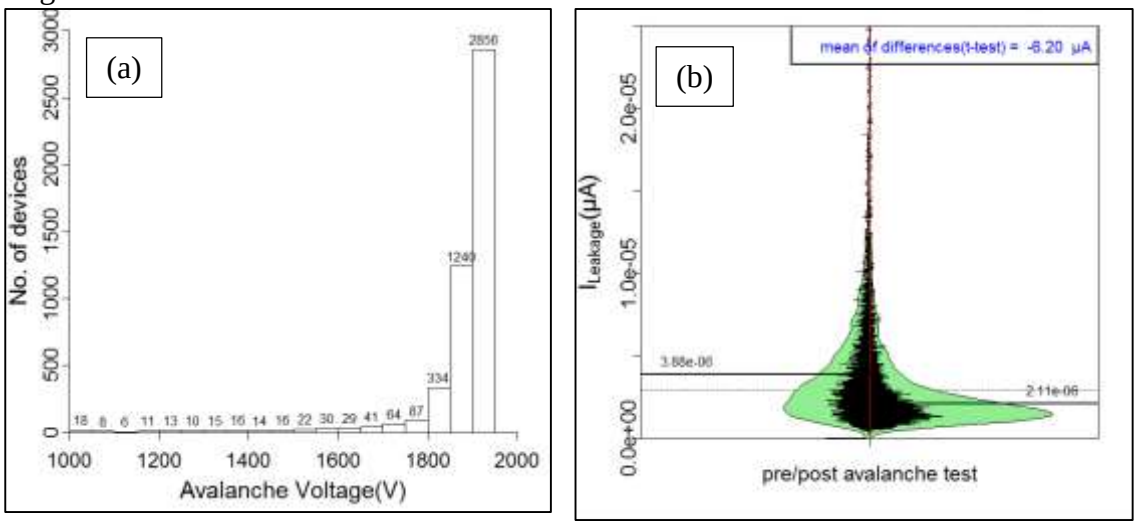
Hence, this project is well aligned with the PowerAmerica vision of reducing the cost of SiC devices (Schottky Diodes), and make them widely available.

Technical Approach: GeneSiC Semiconductor is presently producing its 1200 V SiC Schottky Rectifiers in a 100mm foundry. It has not worked with X-Fab, nor evaluated 150mm wafers for device manufacturing. The first task is to compare yields on small devices between the existing process and the initial process implemented with X-Fab. This is important to benchmark the relative quality of 100mm and 150mm epiwafers; and determine the feasibility of implementing a Schottky Diode process at X-Fab.
A lot of 1200 V/ 2 A and 10 A SiC Schottky diode is to be implemented at GeneSiC's present foundry. Concurrently, a new mask is to be designed towards implementation at X-Fab. Discussions with X-Fab personnel to implement the SiC Schottky diodes to determine the feasibility of processing needs to be completed.

Issues, Risks and Mitigations: Many risks need to be overcome in order to ensure that the project objectives are met. These risks include:

1. 15o mm Epiwafer quality may not be good enough to obtain high yields
2. The toolset at X-Fab may not be compatible with GeneSiC's process flow, necessitating adjustments in process
3. It make take a lot time for the implementation of process flow at X-Fab due to significant changes in Si processing procedures and process parameters. Since the start of the project, only 2 months ago, GeneSiC has made multiple visits to X-Fab, and implemented many process flow adjustments to its standard process flow to make it compatible with the X-Fab toolset. It is too early to say if these issues have been solved.

Significant Accomplishments: As a first step, a "benchmark" batch of 1200 V/2 A and 1200 V/10 A SiC Schottky diodes was run in the present foundry. The purpose of this task is to establish a baseline yield and process integrity, based on which the X-Fab lot would be judged. During this year, one batch of these 100mm wafers was fabricated, and the devices were tested. GeneSiC's custom-designed and built on-wafer testing system will be used for thoroughly characterizing the static performance of devices and test structures. The full suite of device parameters, i.e. blocking voltage, specific on-resistance, ideality factor and Schottky barrier height will be extracted from measurements on every single device on a wafer. The data collected from these measurements will be analyzed via a sophisticated data analysis software package designed by GeneSiC researchers to generate statistical outputs in the form of histograms, bean plots, probability plots, etc. (see **Figure 4**). Using these statistical analysis tools, it will be possible to correlate differences in device performance due to different device designs.



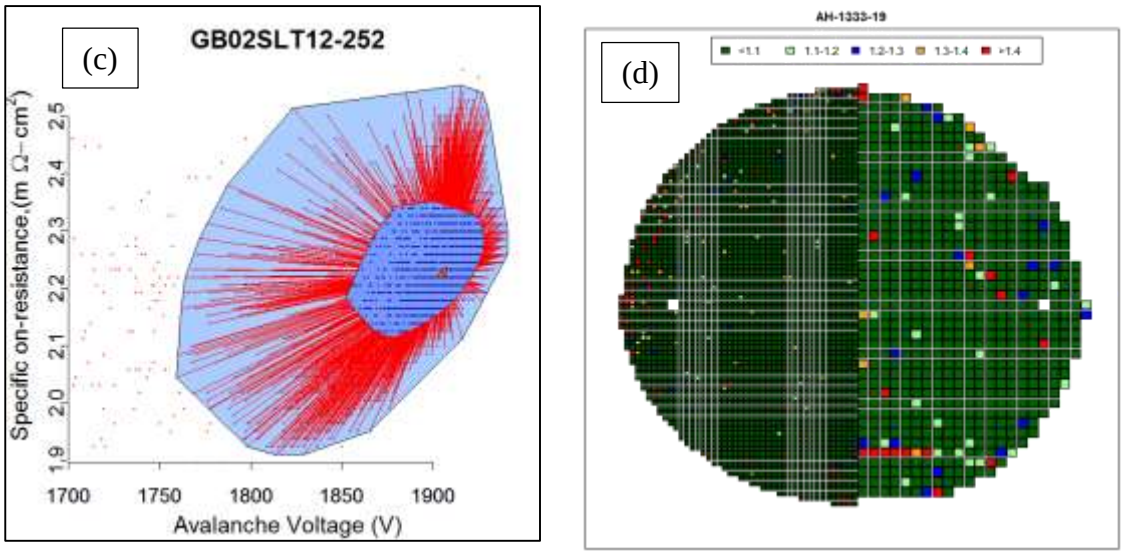


Figure 4: (a) Breakdown voltage histograms, (b) reverse leakage current stability bean-plots, (c) bagplot (or bivariate correlation plot) showing correlation between the breakdown voltage and on-resistance measured on 1200 V/2 A SiC Schottky rectifiers (d) Wafer map of ideality factor measured on 1200 V/2 A and 10A SiC Schottky diodes from one wafer.

In addition, the mask design for the new batch was completed, and process flow was communicated to X-Fab.

Technology to Market: The porting of fabrication of SiC Junction Barrier Schottky (JBS) Diodes and scale up to 150mm production SiC epiwafer process will contribute significantly to the transformative cost reductions. A big part of cost reduction in SiC switches can also be achieved through the realization of economies of scale and through increased volume of production, and the establishment of a viable supply chain (SiC materials-SiC Devices-Reliability-Packaging-Applications-Systems) for these devices. In this proposal, a path that would allow this technology to achieve a "critical mass" and go through and past the "valley of death" towards dominance of GeneSiC SiC Diode products into the marketplace. Hence, a large number of wafers will go through an intensive SiC materials-Device-Reliability-Packaging process. The adoption of these devices is being addressed by significantly improving our applications-system base through our already-established sales/distribution channels, as well as direct customer engagements.

Plans for Next Budget Period If Funded: For the next budget period, if funded, GeneSiC will scale up the current rating of devices to be manufactured. From the present 10 A, the current rating will be increased to 100 A. Further, more sophisticated diode features like avalanche ruggedness, high surge current ratings, and smaller chip sizes will be implemented.

Project Output: None presently, as this project is only 2 months into the first budget period.

Milestone Summary

Milestone No.	Short Title	Due date	**Status (complete/incomplete, notes)**
2.14.1.1	Complete Control batch of benchmark 1200 V/2 A and 10 A Diodes	12/31/2015	Completed.
2.14.1.2	Diode Process finalized for 150mm wafers at X-Fab	2/1/2016	Task initiated with Process Flow given to X-Fab on 10/31/2015. Mask completed and given to X-Fab. 6 wafers procured for lot start. Discussions ongoing on lot start date.
2.14.1.3	Submit data from characterization of test devices fabricated with the two processes	2/15/2016	Control lot data completed. Preliminary statistical data presented in this report.
2.14.1.4	1.2kV SiC JBS diodes demonstrated with BV > 1.2kV, Leakage < 5 mA/cm^2, V_f < 1.7 V at 250 A/cm^2	3/31/2016	Control Lot data matches these metrics. Now, 150mm lot data needs to be completed and presented

Organization : John Deere Electronic Solution (JDES)
Task No./Project Title : Manufacturing and Commercialization of WBG Inverter for off & on Highway Heavy Duty Vehicles
Technical Point of Contact : Dr. Brij N. Singh, Email: SinghBrijN@JohnDeere.com, Phone: (701) 552-8516
Sub-award start date : 02/01/2015

Project Objectives: Project objective of the John Deere Electronics Solutions (JDES) is to establish advantages of wide bandgap (WBG) power electronics in a heavy-duty vehicular application and develop a commercialization pathway for the silicon carbide (SiC) inverter technology. This objective will be fulfilled by the design, manufacture and vehicular deployment of a 200 kW 1050 Vdc SiC dual inverter. Design and development work for the proposed 200 kW 1050 Vdc SiC inverter was originally planned (see copy of JDES SOPO dated 9/24/2014) to go through three iterations, because optimized design can't be achieved without bench-top and vehicle-platform testing. (a) Generation-1 inverter shall be used for bench-top testing in the laboratory using back-to-back dynamometer to establish advantages of WBG material. (b) Generation-2 inverter shall be deployed on John Deere 644k Hybrid Loader to perform fuel economy and loader productivity testing for quantitative determination of projected advantages of WBG technology using a real world application. (c) Generation-3 200kW 1000Vdc SiC inverter shall use test results from Generation-1 and Generation-2 inverters for design optimization, manufacturing and qualification in the 644K Hybrid Loader. Therefore, as stated, three generations of **200 kW 1050 Vdc SiC Dual Inverter** shall be investigated to achieve the final design of an inverter that shall be qualified as per John Deere product guidelines for safety, compliance, durability, and reliability. This 200 kW 1050 Vdc SiC dual inverter shall control PM a generator (175kW continuous power) and PM motor (150kW continuous power) in an electric-drive-train. The PM generator shall have base speed of 5400 RPM and the PM motor shall have base speed of 3200 RPM. Both machines shall have RMS (root mean square line-to-line voltage ratings of 690 V. The proposed power density, weight, and efficiency targets for the optimized final version of a 200 kW 1050 Vdc SiC dual inverter > 27 kW/liter, < 25kg, >96%, respectively.

Technical Approach: JDES's approach is to quickly overcome the WBG technology learning curve by using existing hardware and test facilities in the JDES, Fargo, ND. Then by using the developed know-how design, develop and manufacture an optimized SiC inverter that meets or exceeds the proposed targets for power density, weight, and efficiency. At the start of 200 kW 1050 Vdc SiC dual inverter project, the JDES team had no relevant experience in wide bandgap (WBG) devices. Therefore, to minimize technology development life cycle, the JDES team decided to use PD400 based platform, which is IGBT based inverter, and communicated this minor deviation in project to PowerAmerica and DOE management. This approach has expedited the pace of learning for JDES, as SiC MOSFET retrofitting of the PD400 inverter needed significantly less effort as compared to a new inverter designed and developed from scratch. This has also allowed the JDES team to reuse most of the hardware and focus design efforts where it was most impactful. This approach provided JDES team the necessary platform to develop know-how, gain confidence, and determine key advantages of the WBG technology. The JDES focus is on WBG power electronics advantages which could be successfully exploited in the heavy-duty vehicle application.

The proposed value of the power (200 kW) and the DC bus voltage (1050 V) places the JDES project in a unique position, because none of the PowerAmerica partners offered the 1700 V and 350Adc SiC power module needed for JDES project. To overcome the lack of supply chain for this specific power module, the JDES teamed up with US manufacturers to develop two SiC power modules. For the first module, the

JDES team engaged PowerEx/GE to develop a low-inductance (<5 nH) module that is drop in part for PD400 IGBT based inverter. For the second module, JDES is working with WolfSpeed (formally Cree) to develop a micro-channel based SiC module. The WolfSpeed module will be 50% in volume versus the SiC econo-dual module from PowerEx/GE. These modules are half-bridge in electrical and mechanical configurations and are rated at 1700V, 250Arms, and 350Adc.

To drive the PowerEx/GE module, JDES explored the possibility of an off-the-shelf gate driver. After finding nothing that is compatible with the existing control board, JDES designed and manufactured a SiC gate-driver that seamlessly interfaces with the PD400 inverter control board. JDES's approach was to use existing motor control software. After functional verification of the gate driver, JDES has manufactured one bench-top inverter to characterize the gate-driver and SiC power module at room temperature. This inverter uses JDES's SiC gate driver, 1100 V rated film capacitor module and the rest of hardware from the standard PD400 inverter.

The Gate driver has been used to characterize SiC module and its performance for short circuit protection has been assessed. For the 350Adc rated module short circuit protection is set at ~ 900 A. The gate driver and control board together are designed to respond to a short circuit event within 2 to 3 µs. Also, the PowerEx/GE module has been characterized over a voltage range, e.g. 400V - 1050 V across inverter DC bus and over a current range, e.g. 50 A - 1000 A through the SiC MOSFET. This has resulted in the necessary confidence for JDES to produce a prototype version of a 200 kW 1050 Vdc SiC dual inverter using PD400 hardware, the newly manufactured SiC gate driver, and capacitor module. This inverter is released for back-to-back dyno testing.

Work is in progress to install the prototype of a 200 kW 1050 Vdc SiC dual inverter in a back-to-back dynamometer set-up. An electric motor and generator repurposed from the prototype JD 644 K Hybrid Loader will be operated with this 200 kW 1050 Vdc SiC dual inverter. JDES's short-term objective is to characterize the SiC inverter and assess dv/dt, common mode noise, rise-time, and over-voltage across inverter and electric motor/generator terminals. Therefore, this back-to-back dyno testing will allow the JDES team to get design data for dv/dt filter and insulation systems for the rewinding of the electric motor and generator. An appropriately designed insulation system and electric machine with increased voltage ratings will give the JDES team the necessary confidence to deploy this 200 kW 1050 Vdc SiC dual inverter in the JD 644 K Hybrid Loader and expect it to work without issues. The present JD 644 K Hybrid Loader uses a 700 Vdc IGBT inverter with voltage rating of the electric motor/generator of 460 Vrms, while the 1050 Vdc SiC inverter will produce 690 Vrms at its output. The dv/dt filter will mitigate EMI and EMC issues and will keep the shielding requirement for the power cables to an acceptable footprint. The dv/dt filter will also prevent heating of the power cable between the inverter and electric motor/generator by reducing the amplitude of voltage induced in the shield.

Size and µF value of the DC bus capacitor is a key factor for cost, weight, and power density targets for the SiC inverter. Therefore, the JDES team has used a PD400 IGBT inverter to assess the reduction factor for the DC bus capacitor. Extensive testing in the lab has given enough confidence that if the voltage control loop of the inverter is executed within a 100 µs loop, the SiC inverter could be successfully controlled even at a reduced value of DC bus capacitor. The prototype version of a 200 kW 1050 Vdc SiC

inverter uses a 420 µF film capacitor module, which is more than a three-fold reduction as compared to a 1500 µF capacitor module used in the PD400 standard inverter.
The micro-channel based SiC power module enables JDES to obtain stall current rating even with far fewer SiC die in the power module. The micro-channel and manifold based thermal management method for the WoldSpeed SiC power is co-designed with the technical support from DOE-NREL team. The NREL team has carried out performance analysis using CFD tools. This analysis showed that a micro-channel based SiC module offers a heat transfer coefficient > 30,000 watts/m^2-K, which enables the WolfSpeed to use a lower number of SiC die in the module. PowerEx/GE module uses 12 SiC die per MOSFET, while it is expected that WolfSpeed module will require only 8 SiC die. This will allow the necessary design optimization of the WolfSpeed SiC module, which will result in reduction of cost, stray inductance, and volume as well as increases in module's thermal loading (> 300 watts/cm^2) and performance.

Issues, Risks and Mitigations: JDES team expected that SiC power module for JDES project shall come quickly from one of the module packaging partners in the PowerAmerica. After exploring with the multiple partners in the PowerAmerica and their ability and willingness to develop econo-dual version of the SiC module, JDES team signed development contract with the PowerEx. PowerEx had no experience in this area and needed help form GE. With multiple discussions, PowerEx/GE agreed to develop a low-inductance (<5 nH) SiC module that could drop-in the PD400 housing. Therefore, the risk for SiC module supply chain was understood and was promptly mitigated.

The JDES team understands that commercialization of the WBG technology could only happen if cost targets are at least met at the vehicle system level. The John Deere vehicle platforms are most suitable for an early adoption of the WBG technology. However, the necessary cost targets must be realized. Significant size reduction of the film capacitor module, cable size reduction in the vehicle, elimination of inverter coolant loop, and additional efficiency gains possible due to the WBG power electronics are good incentives for the adoption and commercialization of the WBG power electronics in the heavy-duty off-highway vehicles. The JDES team is designing an engine coolant SiC inverter and when deployed in the vehicle elimination of the dedicated cooling loop for inverter will offset additional costs due to use of expensive power modules.

Micro-channels in the WolfSpeed power modules could have issues of clogging and dandruff build-up. The JDES team is designing a pre-treatment kit that will come with the inverter to pre-treat and filter inverter coolant before it enters in the micro-channels engraved in the SiC power modules. With the technical support from NREL team an extensive testing shall be carried out in the lab before finalizing the proposed fitter kit.

Since SiC power modules switch at a much faster rate, therefore it results on increased values of dv/dt and di/dt. Increased value of dv/dt and di/dt will add additional EMI, EMC and common mode noise challenges versus how these issues exist in the IGBT inverter. To mitigate the dv/dt issue, filter design work is underway and the power PCB in the optimized inverter (generation - 3 inverter) shall have a built-in dv/dt filter.

Significant Accomplishments: John Deere Electronic Solutions (JDES) is on track for development and manufacturing of a 200 kW 1050 Vdc SiC dual inverter. Some key accomplishments are stated in this section along with relevant pictures.

SiC Power Module: An Econo-dual version of the SiC power module has been developed and 15 Econo-dual SiC power MOSFET modules were procured from PowerEx/GE in October 2015. Currently, nine power modules are in use in two inverters. PowerEx/GE module is shown in Figure 1.

Figure 1: Low inductance (< 5 nH) SiC MOSFET module in econo-dual package

For the optimized design and development of a 200 kW 1050 Vdc SiC dual inverter, a purchase order has been placed for the WolfSpeed power modules. These modules are expected to be received by JDES in January 2016. In parallel, JDES has also acquired copper base-plates and sent 25 base-plates to the WolfSpeed in Fayetteville for module packaging. About 25 base-plates are being machined in JDES to learn, "how to engrave micro-channel" and once modules are received from WolfSpeed micro-channels will be engraved in the base-plate of finished module in Feb 2016. WolfSpeed module is shown in Figure 2.

Figure 2: WolfSpeed module (50% volume versus PowerEx/GE module shown in Figure 1)

SiC Gate Driver: The gate driver for the PowerEx/GE module was designed and manufactured in October 2015. It has been characterized for various functionalities, such as, turn-on and turn-off energy minimization, Desat detection and timing control, power supply watch-dog, gain and linearity of the DC and AC voltage sensing circuits, temperature sensing circuit, etc. Gate driver and switching waveforms are in Figures 3 and 4.

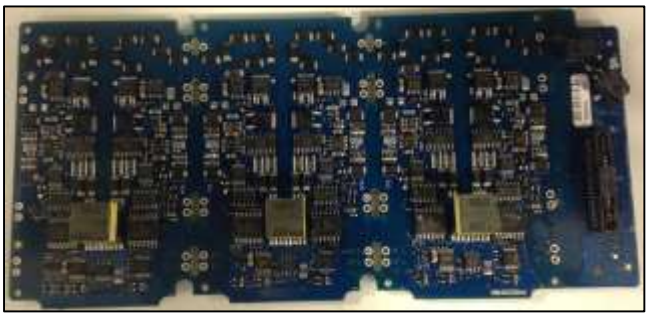
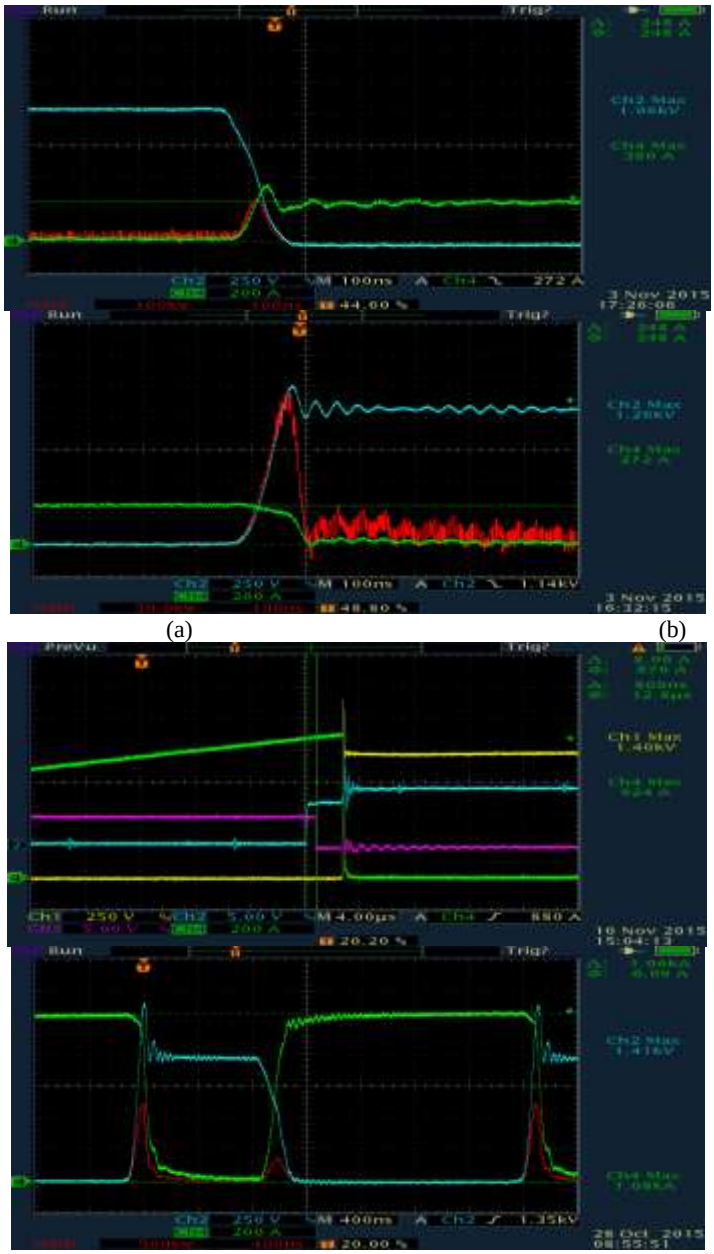


Figure 3: PowerEx/GE SiC module's gate driver design and manufactured by JDES



(a) (b)

(c) (d)

Figure 4: PowerEx/GE SiC module and gate driver characterization waveforms (a) turn-on of MOSFET at 1050 Vdc and 250A (b) turn-off of MOSFET at 1050 Vdc and 250A (c) Desat of MOSFET at 876 A, and (d) turn-on and off of MOSFET at 1050 Vdc and 1000A. Waveforms with red color in a, b and d indicate energy loss during turn-on and turn-off switching events

Capacitor size reduction: Laboratory testing has proved that the 200 kW 1050 Vdc SiC dual inverter can be designed with 300 µF - 500 µF film capacitor. As shown in Figure 5, a capacitor modules using 70 µF 1100 V (@ 85 °C hot-spot) elements have been assembled for bench-top and back-to-back dyno testing of SiC inverter.

(a) (b)

Figure 5: DC bus capacitor module manufactured at JDES using 70 µF 1100 V discrete elements

Inverter assembly: Using PowerEx/GE modules and JDES's manufactured hardware, single and dual inverters were assembled for bench-top and back-to-back dynamometer testing. Test results from these inverters will be used for design optimization of the inverter that will be manufactured using WolfSpeed modules shown in Figure 2 above. Picture of a dual inverter while it is in assembly process is shown in Figure 6.

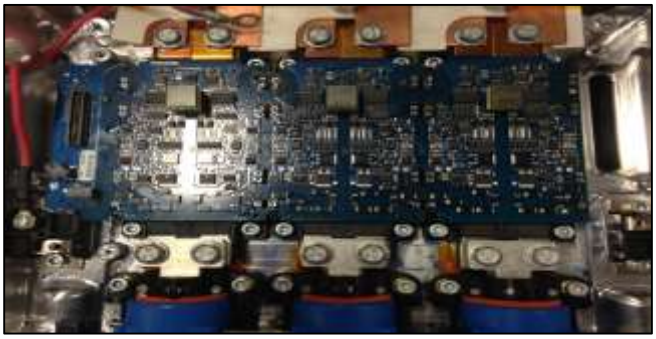
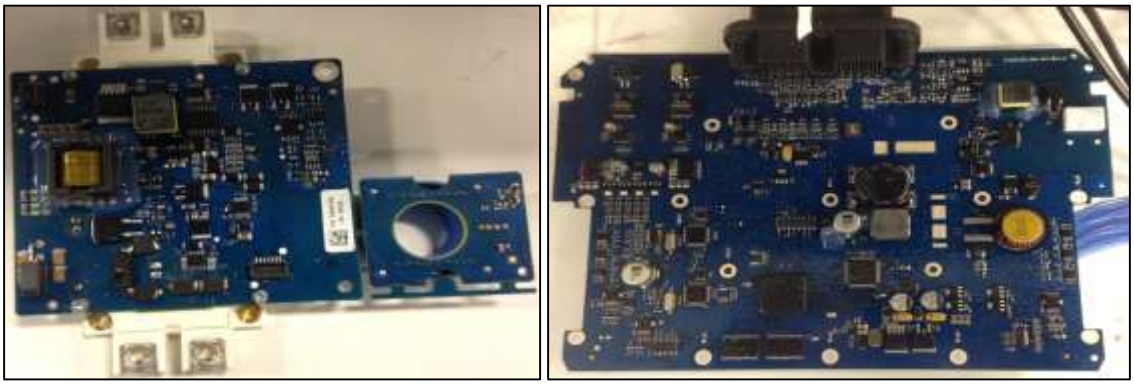


Figure 6: SiC dual inverter manufactured using PowerEx module, JDES Sic gate driver and film capacitor module

Brake chopper board, control board and chopper module: The JDES team has acquired brake chopper gate driver boards and control boards from the PD400 program. IGBTs with specifications 1700 V 600 A were procured from Infineon and these IGBTs will be used to control power resistor to keep the inverter DC bus below 1200 V when the SiC inverter fed electric motor operates in the regenerative/braking mode. The brake chopper and control boards are shown in Figure 7. The brake chopper board also has LEM current sensor.



(a) (b)

Figure 7: (a) Brake chopper gate-driver board, Si IGBT module, and LEM current sensor, and (b) control board

Technology to Market: The John Deere has commercialized JD 644K Hybrid and JD944 K Hybrid Loaders. These vehicles use silicon IGBTs in their electric drive trains. As compared to a conventional 644 Loader, the JD 644K Hybrid Loader offers a 25% reduction in fuel consumption. John Deere motivation is to realize increased fuel economy potentials possible with the SiC based electric drive train. It is highly expected that the proposed 200 kW 1050Vdc SiC dual inverter will have a much smaller footprint and will offer higher efficiency. This will result in a greater fuel savings, such as, 32% less fuel per ton material moved by the SiC version of JD 644K Hybrid Loader versus a conventional 644 Loader. Therefore, JDES objectives for technology to market are to manufacture 200 kW 1050 Vdc SiC dual inverters in Fargo, North Dakota and use them in the JD 644K Hybrid Loader, which is manufactured in the John Deere factory in Davenport, Iowa. Therefore, JDES project will introduce WBG technology in the heavy-duty vehicles and then take this technology to market including penetration in new and niche applications, such as, application where engine coolant power electronics is a key enabler. Also, reductions in fuel consumption will reduce greenhouse gasses, which could eventually entice construction companies to adopt green technologies in their vehicles fleet. Advertising for the increased fuel economy and ability to sustain these claims by the vehicle electrification programs implemented through SiC inverter technologies will be a huge contributing factor and key enabler towards John Deere's market strategy for heavy-duty hybrid vehicles. The micro-channel based SiC MOSFET modules will be produced by the WolfSpeed, which promotes US based WBG technology, supply chain, and a commercialization pathway for WBG power module in harsh environment applications. Following the JDES's lead on the IGBT based inverter commercialization, project team will explore applications of the engine coolant WBG technology in the civilian and military applications. JDES is successful with the application of IGBT inverters in on-highway buses.

Plans for Next Budget Period If Funded: By March 2016, the JDES team will have finished characterization of PD400 based SiC inverter. Data obtained for laboratory testing will be used to design and order parts for the optimized SiC inverter using a micro-channel based power module. By end of March 2016, the majority of the parts for the optimized SiC inverter will be procured. Therefore, building upon successes and accomplishments of Budget Period 1, the JDES team will execute the following strategic plans which are aligned with the JDES objective. This objective is to design, develop, qualify, manufacture, and commercialize an optimized 200 kW 1050 Vdc SiC dual inverter to promote US based manufacturing. The optimized inverter shall meet or exceed the proposed power density (> 27 kW/liter), weight (< 25kg), and efficiency (>96%) targets. High level plans are stated for each quarter of the next budget period.

- Q1: Functional testing of inverter parts and manufacturing of the optimized version of a 200 kW 1050 Vdc SiC dual inverter.
- Q2: Back-to-back dyno testing of the SiC inverter to produce data needed to establish a WBG power electronics technology trade-off
- Q3: Design, manufacturing and testing of the inverter with design improvements needed for engine coolant applications of WBG power electronics technology
- Q4: Deployment of a 200 kW 1050 Vdc SiC dual inverter in the JD 644K Hybrid Loader and carryout limited field testing

Project Output:
One patent application is filed and reported to NC State on June 22, 2015. It is detailed below.

> Chris Schmit and Brij Singh, "A package for a semiconductor device," John Deere disclosure # P23359, filing date April 30, 2015

Also, three patent disclosures are under development and should be filed soon.

Milestone Summary

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
1	Design of mechanical, electronic and electrical parts for bench-top inverter	April 30, 2015	Completed
2	Fabrication of prototype parts for inverter assembly	July 31, 2015	Completed on 10/9/2015. Needed to delay due to design control required for SiC MOSFETs under power supply failures
3	Functional testing of prototype parts of inverter assembly	October 31, 2015	Completed
4	Started prototype assembly of bench-top inverter and testing and verification of bench-top inverter started	January 31, 2015	On-track
5	NREL milestone: Provide thermal management solutions using appropriate thermal interface materials and cooling technologies to enable JDES to complete the design	January 31, 2015	On-track

MONOLITH SEMICONDUCTOR INC.

Organization: Monolith Semiconductor Inc.
Task No./Project Title: 2.4/1200V SiC Diode Commercialization and Production
Technical Point of Contact: Kiran Chatty
Sub-award start date: Not yet awarded

Project Objectives: The objectives of Monolith Semiconductor Inc.'s Power America project are 1) To enable transformation of a commercial 150mm silicon CMOS fab into a high-volume SiC foundry, 2) Develop manufacturable, high yielding and low-cost 1200V SiC diodes with best-in-class performance and reliability at the Institute 's 150mm SiC foundry and 3) Provide 1200V, 10A SiC diode engineering samples to Power America commercialization partners.

Technical Approach: Monolith Semiconductor Inc. selected X-FAB Texas as its SiC device-manufacturing partner in 2013. Monolith has since been working with X-FAB Texas in developing SiC wafer handling procedures, SiC unit process steps and an integrated process flow for manufacturing of SiC MOSFETs and diodes. Monolith's process development approach has focused on compatibility of majority of SiC MOSFET and diode process steps with the tools and processes already available at X-FAB Texas. Si process steps have been re-used when possible and new process steps have been developed only when existing process steps were inadequate. Through smart process integration, exploiting the strengths of advanced silicon CMOS fab with innovative device design and through Monolith team's long experience in SiC R&D and Si power device manufacturing in foundries, Monolith aims to achieve the technical objectives of the Power America program. A 1200V, 10A diode mask set was developed under another program has been re-used for establishing 1200V SiC diode process and design at X-FAB Texas. The 1200V, 10A diodes have been packaged in 2-lead TO-220 packages for package level characterization and reliability assessment. The 1200V diodes and the 1200V MOSFETs developed under other Government funded projects and internal R & D will be provided to Power America's commercialization partners.

Key Accomplishments:

1. SiC wafer handling at X-FAB Texas has been established
2. A manufacturable, high yielding 1200V SiC diode process has been developed
3. 1200V, 10A SiC diode design has been established
4. Key electrical characteristics of the 1200V, 10A SiC diode developed at X-FAB Texas:
    a. Breakdown voltage > 1250V
    b. Forward voltage drop at 10A < 1.8V
    c. Reverse Leakage current at 1200V < 10uA

Experimental Results: This section presents the key experimental results from the 1200V, 10A diodes developed at X-FAB Texas.

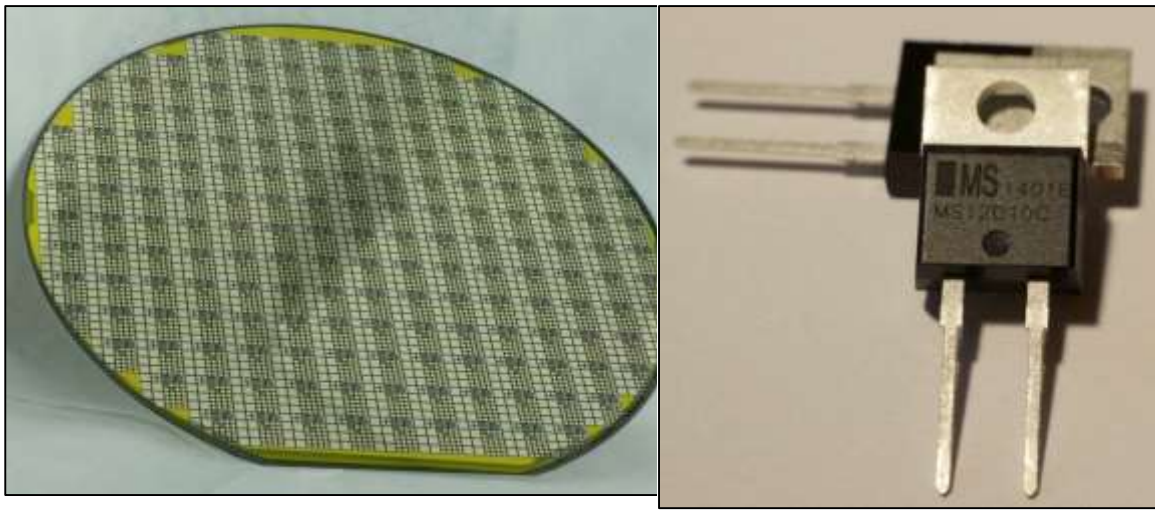


Fig. 1: A 150mm SiC wafer fully processed at X-FAB Texas using Monolith's 1200V SiC diode process (left). The 1200V, 10A diodes have been packaged in 2L TO-220 package (right).

Fig. 1 shows a picture of a 150mm SiC wafer fully processed at X-FAB Texas using Monolith's 1200V SiC diode process. The 1200V, 10A diodes have been packaged in 2L TO-220 package as shown in Fig. 1 (on the right). The diodes have been characterized using 371 Curve Tracer, Keithley 2657 and using Focused Test FT1000 tester.
The forward I-V characteristics acquired on 1200V, 10A diodes (25 samples) using 371 curve tracer is shown in Fig. 2. The typical V_F at 10A for the 1200V, 10A diodes is 1.5V.

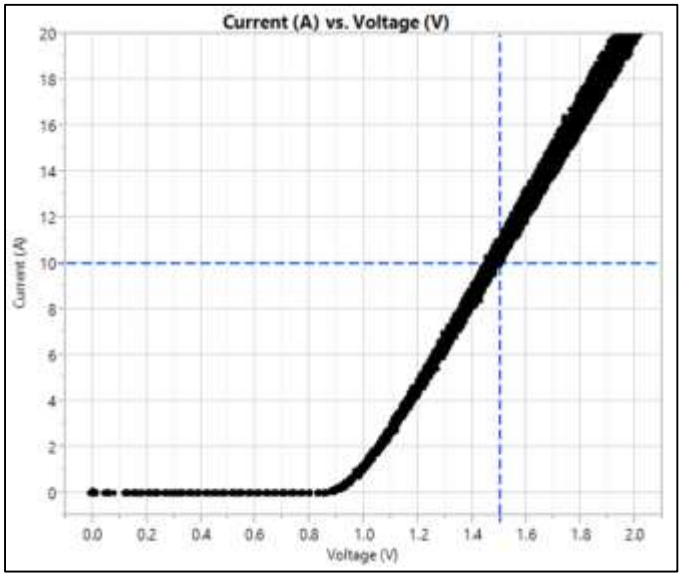


Fig. 2 Forward I-V characteristics of the 1200V, 10A diodes (25 samples) acquired using 371 curve tracer. The typical forward voltage drop (V_F) at 10A is 1.5V.

The reverse I-V characteristics of the 1200V, 10A diodes acquired using 371 curve tracer is shown in Fig. 3. The median breakdown voltage of the diodes is approximately 1600V at 250uA reverse leakage current.

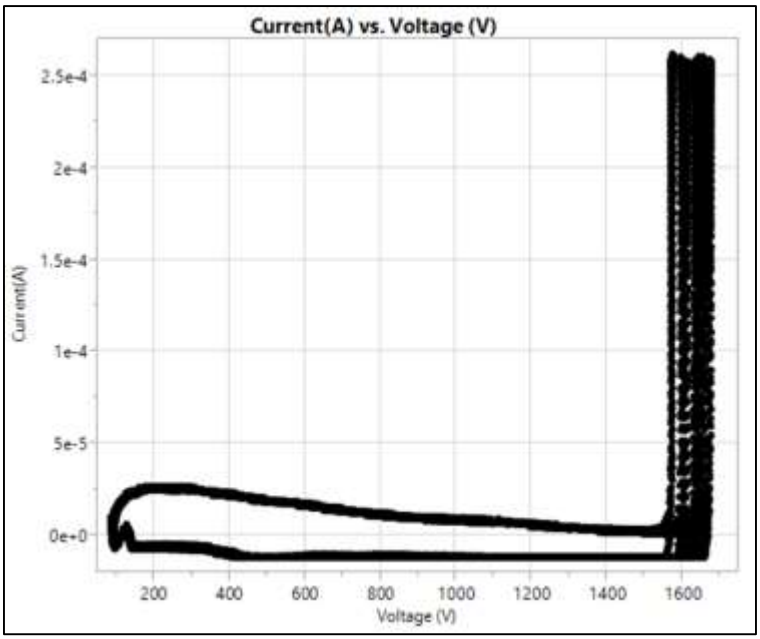


Fig. 3 Reverse I-V characteristics of the 1200V, 10A diodes acquired using 371 curve tracer.

The reverse I-V characteristics of the 1200V, 10A diodes acquired using Keithley 2657 High Power System SMU is shown in Fig. 4. The typical leakage current (IR) at 1200V for the diodes is < 100nA.

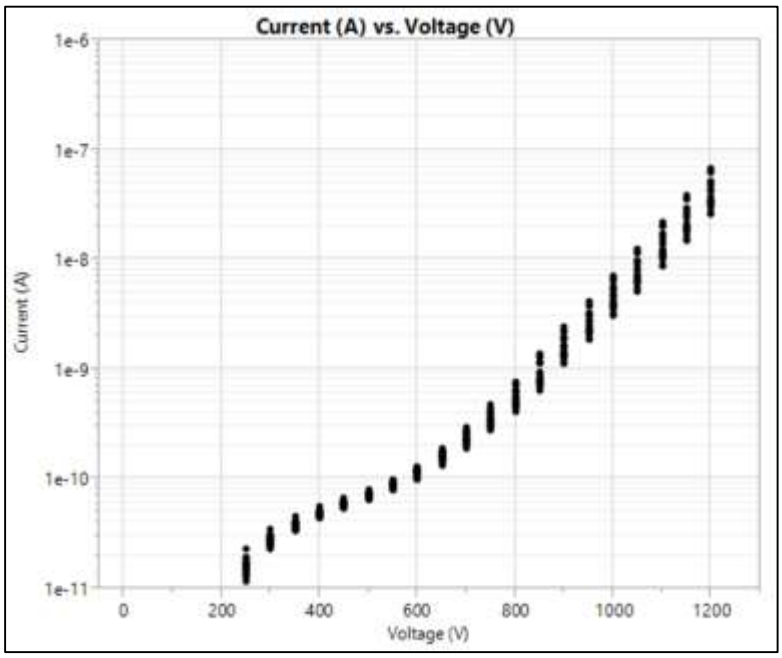


Fig. 4 Reverse I-V characteristics of the 1200V, 10A diodes acquired using Keithley 2657 High Power System SMU.

Summary: Monolith Semiconductor Inc. has developed a manufacturable, high yielding 1200V SiC Schottky diode process at X-FAB Texas. 1200V, 10A diodes designed and fabricated using Monolith's SiC diode process exhibit excellent electrical characteristics. The reliability assessment of the 1200V, 10A diodes is currently in progress. Monolith is expected to announce commercial 1200V, SiC diodes in the near future.

Dr. Jay Baliga

Organization : North Carolina State University
Task No./Project Title : Integrated SiC MOSFET and JBS Diode (SOPO task #2.8.2)
Technical Point of Contact : Dr. Jay Baliga Phone: (919) 515-6169
Start date for internal NC State project: 2/1/2015

Project Objectives: The integration of the JBS diode with the 1.2kV Power MOSFET will be performed in this task. Both devices not only share the forward conducting layer, but also share the edge termination region. Device designs that optimize the size of the diode and power MOSFET are being pursued. In addition, this approach will reduce the number of packages in half bringing down the cost of implementing this technology in power converters. It will improve efficiency and increase switching frequency by eliminating the parasitic inductance between separately packaged devices. A process flow for fabrication of the JBS diode and the power MOSFET will be established. Power MOSFETs with integrated JBS diodes will be fabricated at X-FAB.

Significant Accomplishments:

- Single Ohmic/Schottky metal process established: Development of a single metal, single thermal treatment process for the simultaneous formation of Schottky, and Ohmics to N+, and P+ region was successfully completed. Comparative studies were conducted to examine reverse blocking behaviors as well as forward I-V characteristics of SBD, JBS, and PiN diodes. It was found that Ni can serve as a multiple functioning metal for forming Schottky on n-, n+ ohmic, and p+ohmic when annealed at 850C, for 2min (see Fig. 1, and Fig. 2). Contact resistances estimated from TLM structures were 4.12×10^{-5} ohm·cm^2, and 1×10^{-3} ohm·cm^2 for N+ implanted region, and P+ implanted region, respectively. This approach not only simplifies the mask layout, but it also eliminate two mask processes.

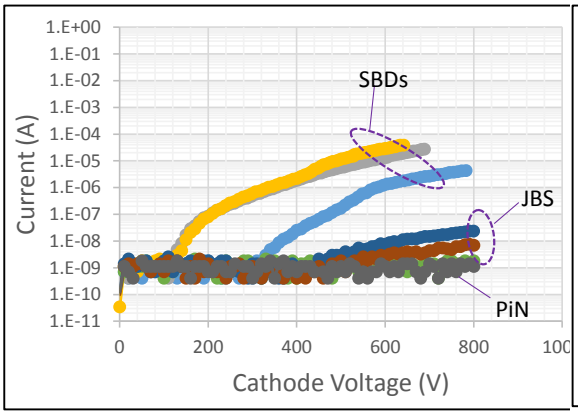


Fig. 1. Measured reverse blocking behavior of SBD, JBS, and PiN diodes. Ni 100nm deposited and annealed at 850C for 2 minutes.

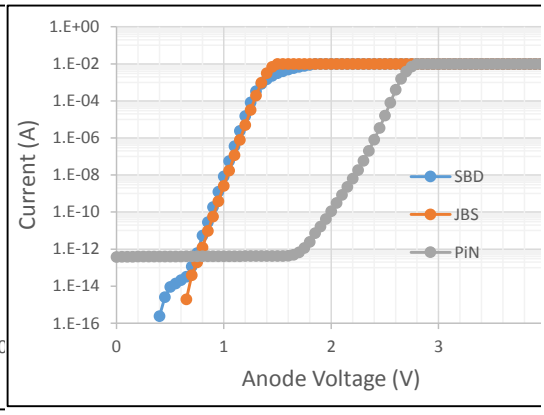


Fig. 2. Measured forward current-voltage characteristics of SBD, JBS, and PiN diodes. No sub-knee current is observed in 850C, 2min annealed sample.

- Optimum designs for JBSFET defined: JBSFET design to minimize the specific on-resistance, and to achieve low leakage current during off-state. Parameters for the JFET region, and Schottky region was carefully designed using 2-D device simulations (see Fig. 3, and Fig. 4).

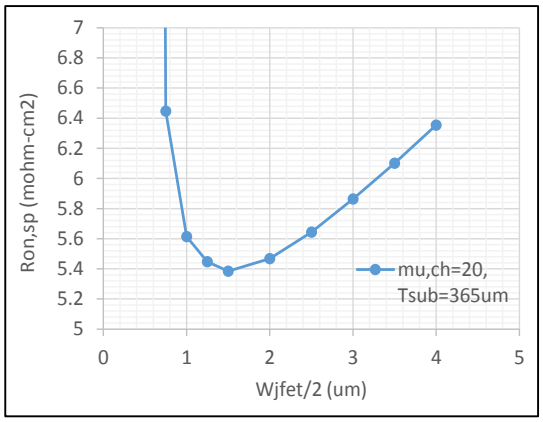


Fig. 3. Optimization of JFET width (Wjfet). Ron,sp is minimized with half jfet width of 1.5um. Enhanced doping for the JFET region is not planned for the 1st run. JFET implant will further reduce the Ron,sp.

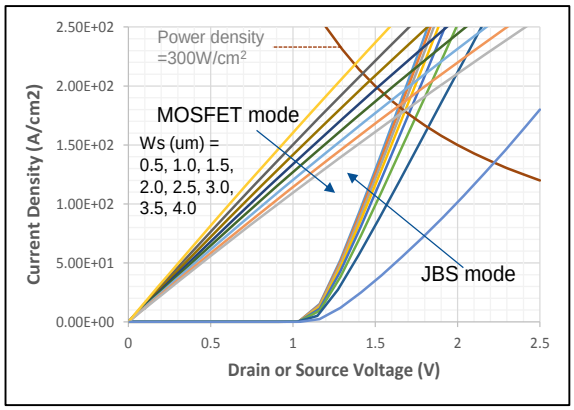


Fig. 4. Optimization of Schottky region opening (Ws). Ws should be kept as low as possible to get lower leakage current of JBS diode. At the same time, on-voltage drop should be comparable to that of MOSFET. Optimum half Schottky width=2um.

- Various layout approaches for JBSFETs proposed: Layout of JBSFET should be designed to target a specific current capability of MOSFET, and JBS diode at the same time. Several layout approaches for JBSFET were proposed (Fig. 5). Total wafer area consumed by JBSFET designs were compared with the conventional approach. About 40% area saving can be achieved by the proposed layout approach as shown in Fig. 6.

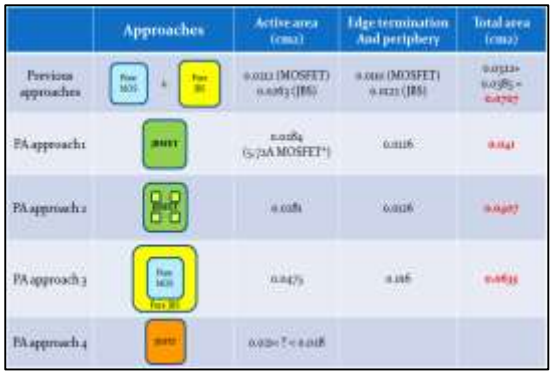


Fig. 5. Summary of proposed layout approaches

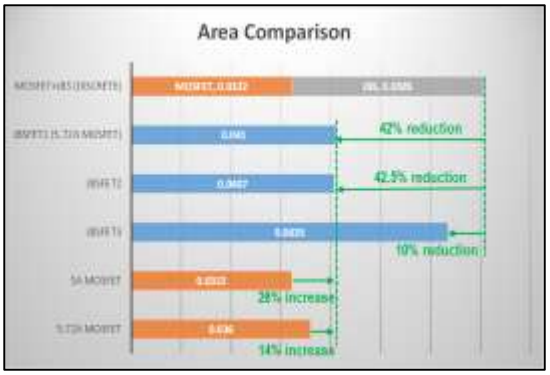


Fig. 6. Wafer area consumption of JBSFET (Ws=2um, target current=5A)

- Best edge termination design identified: Various edge termination techniques such as floating field rings (FFRs), junction termination extension (JTE), and modified edge termination structures (Ring Assisted-JTE, Multiple Floating Zone-JTE) were designed (see Fig. 7, and Fig. 8). PiN diodes with proposed edge termination structures were designed and incorporated in the mask layout.

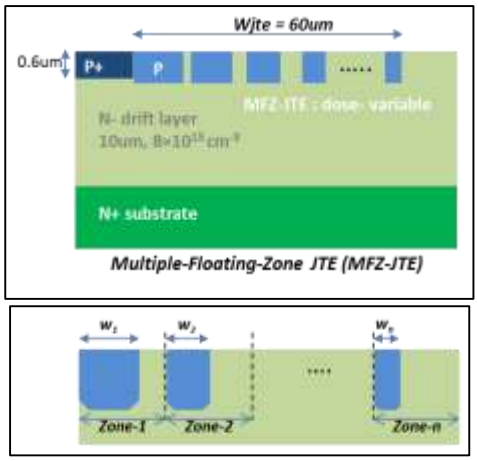


Fig. 7. Simplified cross-sectional view of MFZ-JTE. w_0=total edge termination width/# of zones, $w_n=w_0/\alpha^n$, $\alpha>1$

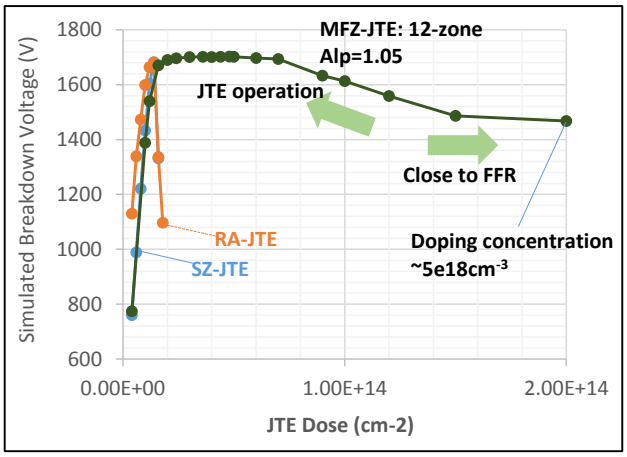


Fig. 8. Much wider process latitude can be accomplished by MFZ-JTE design. It also shows the fundamental difference of JTE based edge termination, and FFRs.

- Process flow for JBSFET defined with X-Fab: Process baseline was established through extensive discussions with X-Fab. NCSU proposed recipes for gate oxidation, NO post oxidation anneal, ion implant schedules, and contact process.

Table1. Process flow for 1.2kV SiC MOSFETs, and JBSFETs.

Mask	Process steps	Description	Specifications	Comments
	Wafer	N-/N+ substrate	10um, 8×10^{15}cm^{-3}	Minimum 5ea per run
1	Alignment Mark	SiC Etch	~0.5um	
2	P-base implant	Oxide dep.	Oxide thickness 1.5um	Oxide thickness depends on the implant schedule
		Photo, Oxide etch		Oxide etch recipe, selectivity (Oxide vs. SiC)
		Al implant, HT	Implant schedule	Wafer split: 3ea for inversion mode, 3ea for accumulation mode
3,4,5	N+, P+, JTE implant module	N, Al imp. For N+, P+&JTE	Same as P-base	
	Activation Anneal			1650C, 10min, Ar, Capping process, Outsourcing
	Sacrificial Oxidation	Oxidation/Removal	20nm	1175C, 20nm / BOE
	Gate Oxide, NO anneal	Oxidation	50nm	1175C, 50nm / POA: 1175C, 2hr, NO
6	Gate Poly dep. W silicide, Photo, Etch	Std process	Poly thk, 5000Å	W etch, Poly Etch
7	Oxide dep., Photo, CT Etch	Std process	LPCVD 0.7um	
	Ohmic, Schottky metal	Single metal, Anneal		Ni, 100nm, Silicide at low temp., wet etch, and RTP: 850C, 2min
8	CT on Poly	Oxide etch		To open the contact on poly
9	Top Metal, B/S Metal	Std process	4um	Ti 2000A, AlCu (0.5%) 4um
10	Polyimide	Std process	5um	Pad open

Milestone and deliverable status

- All milestones have been met.

Table2. Milestones and deliverables of task 2.8.2 Integrated SiC MOSFET and JBS Diode

	Deliverables	Q1	Q2	Q3, Q4 (plan)
2.8.2.1	Schottky contact & Ohmic contacts	-. Literature review -. Layout, mask preparation -. Wafer preparation	-. Fabrication of TLMs, Diodes (PiN, JBS, Schottky) : 5-mask processes done by NCSU -. Characterization of the first set of experiments (Ni)	
2.8.2.2	JBSFET cell design	-. MOSFET cell design, optimization -. JBS cell design, optimization -. Layout approaches, and area comparison -. Edge termination design (FFRs, SZ/RA/MFZ-JTEs)	-. Layout of MOSFETs, JBSFETs, and Diodes -. Reviewed the mask design with X-Fab	
2.8.2.3	Process flow	-. Initiated discussion with X-Fab -. Ver0 process flow suggested	-. Discussions on the unit process : Gate oxidation, Ni silicide process -. Finalized the process flow based on the discussions	
Go/No-Go	Fabrication & Characterization	-. Discussion with X-Fab	-. Wafers were delivered (X-Fab) -. 4-5 days / mask, 1week for each implant, 10 days for the activation anneal	-. Mask production (1st week of Sep.) 3-4wks -. Lot start: 1st week of Oct. It will take ~3 month to finish the 1st lot

Dr. Jay Baliga

Organization : North Carolina State University
Task No./Project Title : Novel Edge Termination for High Voltage SiC Devices (SOPO task #2.8.3)
Technical Point of Contact : Dr. Jay Baliga Phone: (919) 515-6169
Start date for internal NC State project: 02/01/2015

Project Objectives: For discrete high voltage power devices, the edge termination, located at the periphery of the active area, can occupy 50% of the chip area. This subtask will focus on development of edge terminations for 3.3 and 4.5 kV SiC devices with reduced space on the die surface. Approaches to reduce the number of processing steps will be emphasized to reduce the cost of manufacturing of the devices.

Significant Accomplishments: Promising edge termination designs for 3.3kV, and 4.5kV SiC devices proposed: Various edge termination techniques such as floating field rings (FFRs), single zone junction termination extension (SZ-JTE), multiple zone junction termination extension (MZ-JTE), ring assisted junction termination extension (RA-JTE), multiple floating zone junction termination extension (MFZ-JTE), bevel junction termination extension (Bevel-JTE), bevel assisted junction termination extension (BA-JTE) were designed and compared by 2-D simulations.

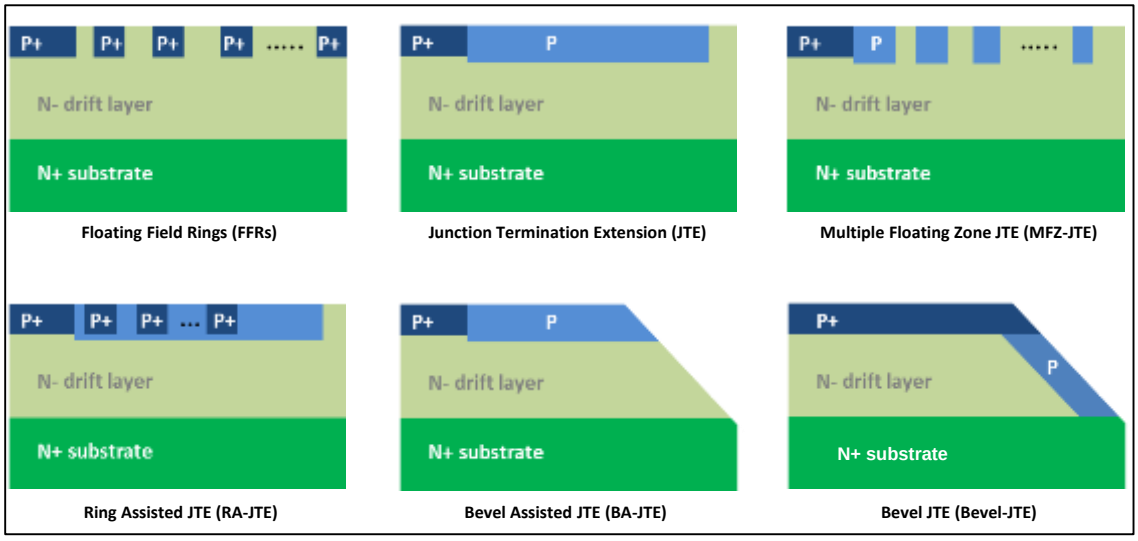


Fig. 1. Edge termination structures for high voltage SiC devices.

- Conventional FFR for 4.5kV devices: optimum design S_0=0.6um, S_i=0.08um

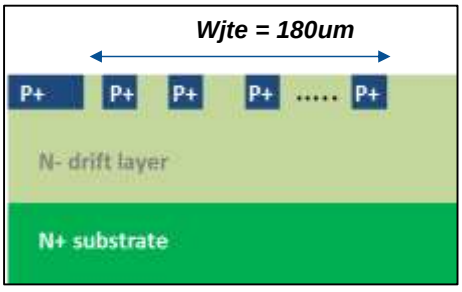


Fig. 2. Design of FFRs. 35 rings, width of each ring W=3um, S_0 (first space)=0.6um, S_i (incremental space)=0.08um, $S_n=S_{n-1}+S_i$

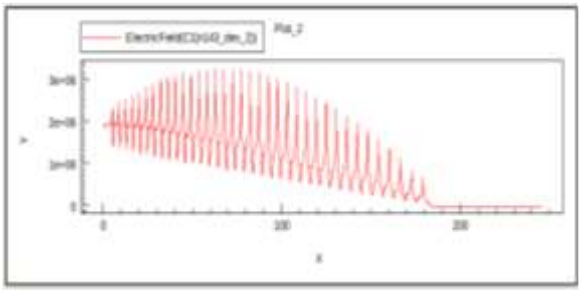


Fig. 3. Electric field distribution of PiN diode with optimized FFR design at breakdown (BV=4730V).

- Conventional JTE for 4.5kV devices: SZ-JTE, and MZ-JTE designs

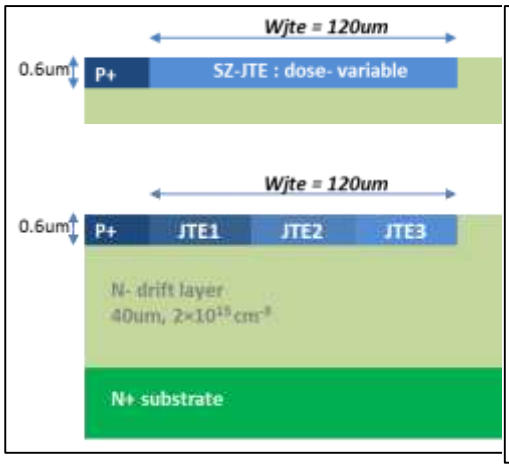


Fig. 4. Design of SZ-JTE, and MZ-JTE. In MZ-JTE,
JTE2 dose=α × JTE3 dose
JTE1 dose=α^2 × JTE3 dose

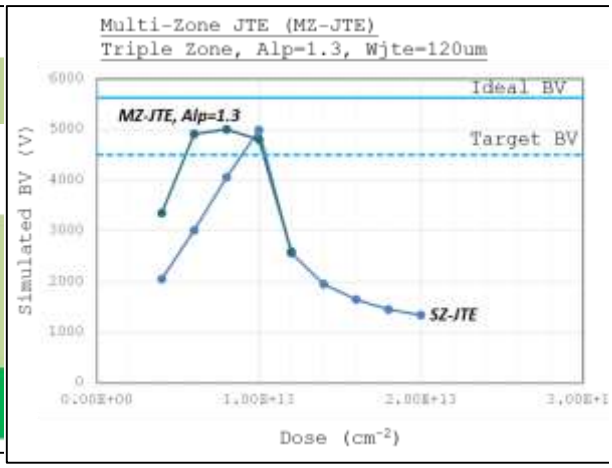


Fig. 5. Simulated BV according to JTE dose. Wider process latitude can be achieved by MZ-JTE design. But, need more process steps.

- Ring Assisted JTE (RA-JTE) for 4.5kV devices

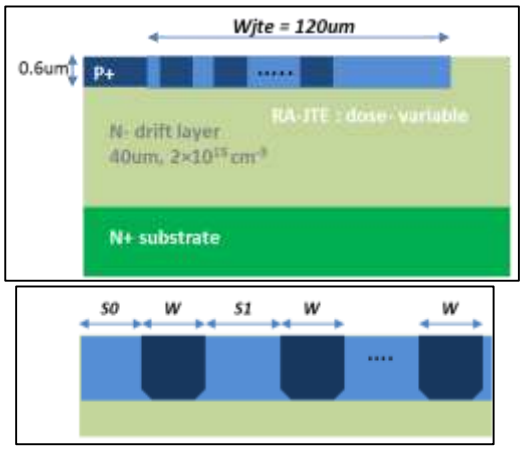


Fig. 6. Design of RA-JTE. Design of rings inside the SZ-JTE is similar to FFR design.

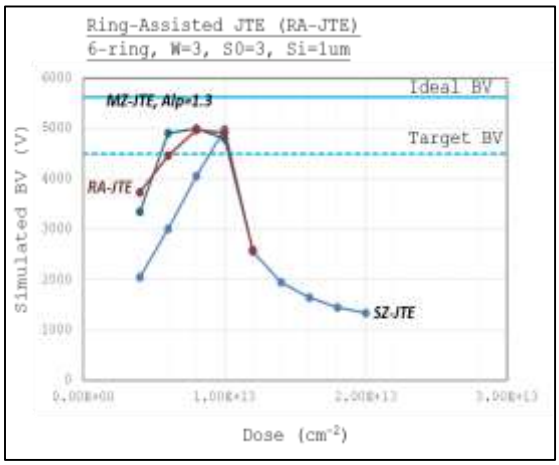


Fig. 7. Simulated BV according to JTE dose. RA-JTE design provide a wider process window than the SZ-JTE design.

- Multiple Floating Zone JTE (MFZ-JTE) for 4.5kV devices

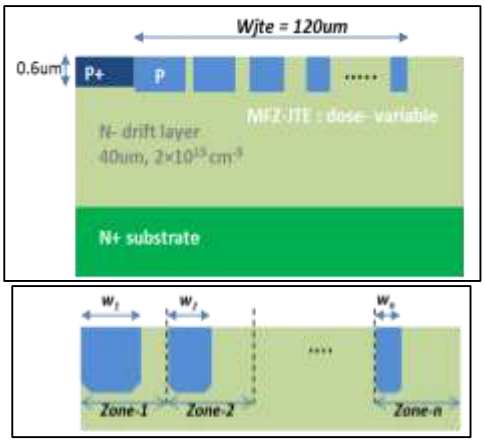


Fig. 8. Design of MFZ-JTE. w_0=total edge termination width/# of zones, $w_n=w_0/\alpha^n$, $\alpha>1$

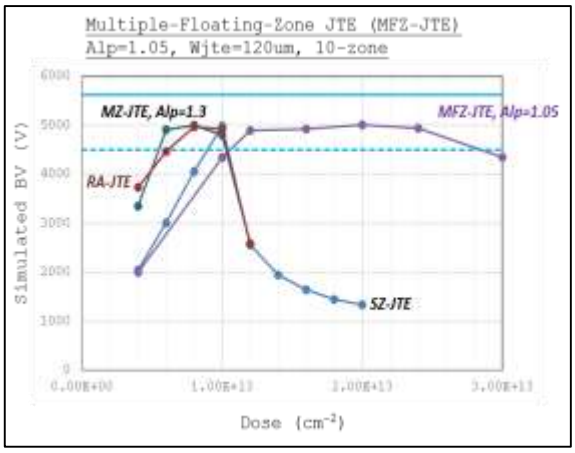


Fig. 9. Simulated BV according to JTE dose. Wider dose range accomplished without additional processes.

- Bevel-JTE for 4.5kV devices

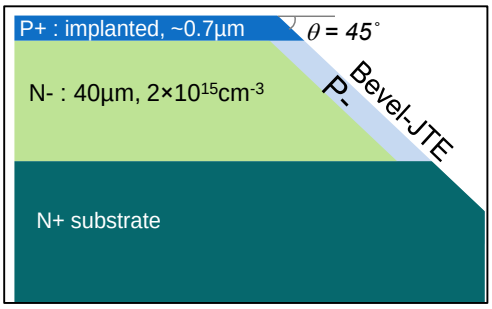


Fig. 10. Design of Bevel-JTE. Electric field curvature is inherently relieved by the bevel structure.

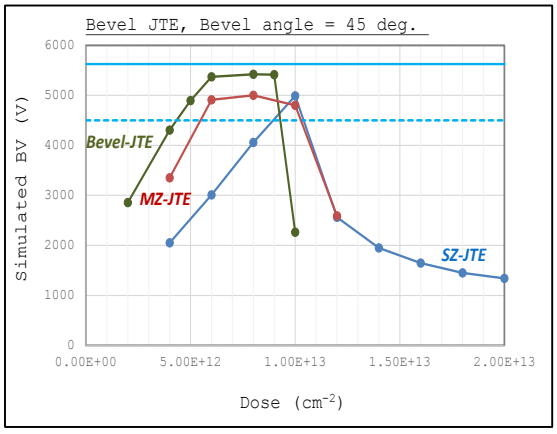
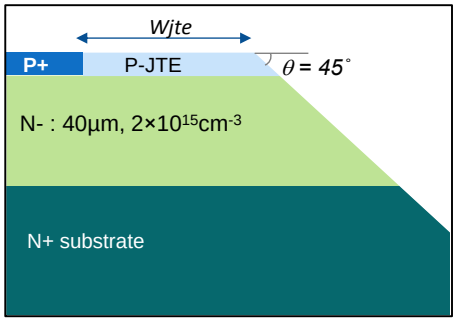


Fig. 11. Simulated BV according to JTE dose. Higher breakdown voltage, and wider dose range can be achieved.

- Bevel Assisted-JTE (BA-JTE) for 4.5kV devices



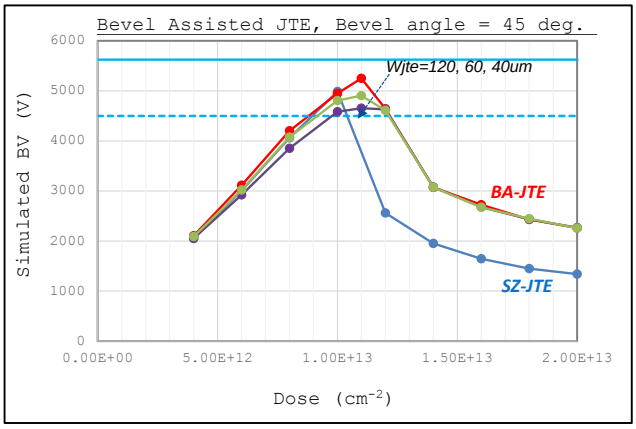


Fig. 12. Design of Bevel Assisted-JTE. Electric field curvature is inherently relieved by the bevel structure.

Fig. 13. Simulated BV according to JTE dose. Higher breakdown voltage, and wider dose range can be achieved.

- Comparison of proposed edge termination structures for 4.5kV devices: Conventional floating ring has width of 180um, and requires very narrow spacing, which may impact manufacturing yield. 3-zone-JTE with width of 120um requires 3 mask-implant steps. MFZ-JTE requires only one mask-implant step. MFZ-JTE has wide process tolerance which should improve manufacturing yield. MFZ-JTE is 1.5X smaller than conventional floating ring edge termination. Bevel-JTE is 4.5X smaller than conventional floating ring edge termination. BA-JTE is 1.8X smaller than conventional floating ring edge termination.

Table1. Comparison of proposed edge termination designs for 4.5kV devices

	Optimum design	Maximum BV	Dose range (>4500V)	Process steps	Edge termination width
FFRs	35 ring, W=3um, S0=0.6um, Si=0.08um	4730V	NA	No additional steps required, **Narrow features, many rings**	**180um**
SZ-JTE	Dose=1e13 cm-2	4990V	Sharp peak	Single pattern, implant for JTE	120um
MZ-JTE	3-zone, Alp=1.3	5000V	6e12 ~ 1e13 cm^{-2}	Triple pattern, implant steps	120um
RA-JTE	6 ring in SZ-JTE, W=3um, S0=3um, Si=1um	4975V	6e12 ~ 1e13 cm^{-2}	Single pattern, implant for JTE	120um
MFZ-JTE	10-zone, Alp=1.05	5010V	**1.2e13 ~ 2.8e13 cm^{-2}**	Single pattern, implant for JTE	**120um**
Bevel-JTE	Bevel with 45 degree angle	5421V	**4e12 ~ 1e13 cm^{-2}**	**No pattern, bevel dicing**	**40um**
BA-JTE	Wjte=60um, 45 deg angled dicing	5250V	**9e12 ~ 1.2e13 cm^{-2}**	**Single pattern, bevel dicing**	**100um**

Milestone and deliverable status

- All milestones have been met.

Table2. Milestones and deliverables of task 2.8.3 Novel edge termination for high voltage SiC devices

	Deliverables	Due
2.8.3.1	Design of a MFZ-JTE for 3.3 and 4.5kV devices demonstrating 1.5x reduction in edge termination space optimized through 2D device simulations. (Month 3)	Apr-15
2.8.3.2	Design of Bevel Termination for 3.3 and 4.5kV devices demonstrating 2x reduction in edge termination space optimized through 2D device simulations. (Month 6)	Jul-15
2.8.3.3	Process for MFZ-JTE and Bevel Termination demonstrating reduction in number of steps by a factor of 3 completed. (Month 9)	Oct-15
Go/No-Go	Diodes using proposed edge terminations with 3.3 and 4.5kV blocking voltages fabricated with leakage currents < 1 mA/cm^2 normalized to total chip area. (Month 12)	Jan-16

Dr. Subhashish Bhattacharya

Organization: North Carolina State University
Task No./Project Title: Task 4.11 Medium Voltage Gate Drive with 10 kHz 10 kV SiC MOSFET for 2.3 kV, Motor Drives (Month 0-12)
Technical Point of Contact: Subhashish Bhattacharya
Start date for internal NC State project: 02/01/2015

Project Objectives: The primary objective of this project is to design, develop and validate a 15 kV isolated gate driver (GD) for 10kV SiC MOSFET suitable for operating at 10 kHz to 20 kHz with integrated diagnostics and active gate driving capability. With industry partners collaboration; the project also aims to commercialize HV 15 kV isolated GD for HV SiC 10 kV MOSFET. Multiple paths for collaboration with industry that may lead to commercialization have been identified with two - three companies interested in HV gate driver, or enabling components/materials for gate driver components.

Project's Contribution to the PowerAmerica Mission: High voltage SiC devices has been of recent interest for medium voltage applications. These high voltage devices will enable use of simpler converter topologies. The major industries focused in the power conversion business are targeting to substantially improve the quality and efficiency of their product. The industrial areas where these high voltage SiC devices can be expected to impact are as below:

- Medium Voltage drives (steel mills, oil drilling, pumps, fans and compressors, all heavy industry applications)
- Traction Applications (railway, electric car, ships)
- Grid-tied PV Applications
- HVDC Transmission (wind, tidal, hydro)
- Medium Voltage DC grid (DC distribution)

The gate driver designed in this project will play significant role in the application of the high voltage SiC devices. It is expected that with the development of the intelligent gate driver industries reluctant to make a move towards use of high voltage SiC devices will also be attracted towards this technology.

The project team consists of 4-5 graduate students, one post-doctoral fellow/researcher and one faculty supervisor. The team of students and post-doctoral researcher received a very good exposure to the complete WBG based power electronics system development. This involved knowledge of device design, module packaging, device characterization, converter system design, thermal management, magnetics design, and design for EMC, analysis of circuit parasitics and their optimization, system and personnel protection. It is expected by the end of the project year, at least 6-7 highly trained manpower in WBG semiconductor applications will be generated. The US power industries can easily tap into these trained resources for further enhancing their capabilities.

Technical Approach: Different tasks like Intelligent Gate Driver (IGD) development, gate driver power supply isolation coupling transformer design with low coupling capacitance, and high frequency converter design for MV motor drives are carried out in parallel. Intelligent gate driver board is designed and developed with different features like device temperature measurement, device collector-emitter voltage measurement during on-state, device current measurement, active gate drive features and voltage de-sat (measurement of device voltage for shoot-through overcurrent) protection. The developed board is tested on double-pulse test circuit for validating active gate drive section, boost converter for low side measurement and boost-buck converter for high side measurement. An interface board is used on the control bench to monitor and analyze the data

transferred from the IGD. Table I shows the initial specification of this 10kV SiC MOSFET intelligent gate-driver.

TABLE I: Intelligent MV Gate Driver Functions

Parameters/Functions	Value [Units]
Isolation Voltage	20 kV
Isolation Capacitance	< 1.5 pF (initial spec was < 5pF)
Drive Voltages	+20/ − 5 V
Optical Communication	Vds(on), Ids , T
Shoot-through Protection	Vgs Controlled
Protections	Local OT (Over Temperature), OC (OverCurrent), ST (Shoot-Through)
Active Gating	Clock Timed

Different versions of gate driver power supply isolation coupling transformer with low coupling capacitance are developed using different cores types and dimensions. The transformer coupling capacitance and magnetizing inductance is measured using LCR meter at different frequencies from 10 kHz to 110 MHz. The finalized transformers are then tested using the power supply board on the buck side device of the boost-buck converter for high side validation.

The three-phase converter is developed using six 10 kV/10 A SiC MOSFETs and six Gen-I gate drivers. Before mounting on the converter, each of the devices is validated using heat-run test in the boost converter. The high side device gate-drivers are tested using the boost-buck converter. The three-phase converter is tested at both 10 kHz and 20 kHz switching frequencies. Using 20 kHz switching frequency, the fundamental frequency has been increased up to 1 kHz.

Issues, Risks and Mitigations: The challenges of operating the gate driver and converter at medium voltage are manifold. The high dv/dt generated EMI from 10 kV SiC MOSFETs switching on and switching off (which can be up to 50-60kV/us) are difficult to handle. This high dv/dt switching causes spiky capacitive coupling currents to flow through the parasitic capacitances everywhere in the system. This results in spurious OC (Overcurrent) tripping of the converter mainly due to the parasitic capacitive coupling currents. This requires filter inductor (or high frequency transformer) design with very low parasitic capacitance to reduce the capacitive coupling currents. Proper EMI shielding techniques have to be used to overcome this issue. Proper thermal design of the converter is also very important to protect the devices from high temperature related damage due to generation of hot spots. Transmission of reliable data from IGD (Intelligent Gate Driver) to the interface board is also a design challenge due to noisy environment. Proper high voltage insulation and isolation requirements are very important to prevent breakdown. Finally, safe operation is the most important factor when it comes to high voltage operation of the power converters.

Significant Accomplishments:

- **Isolated Power Supply Design with Low Coupling Capacitance for Intelligent Gate Driver**

The gate driver isolated power supply transformer coupling capacitance has been reduced to lower than 1 pF. Figs. 1 to 4 show two different versions of the transformer and their measured capacitances using frequency analyzer.

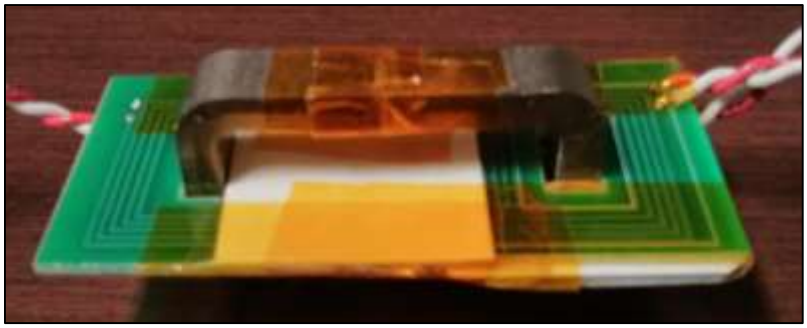


Fig.1. Transformer design 1 with 0.7 pF coupling capacitance

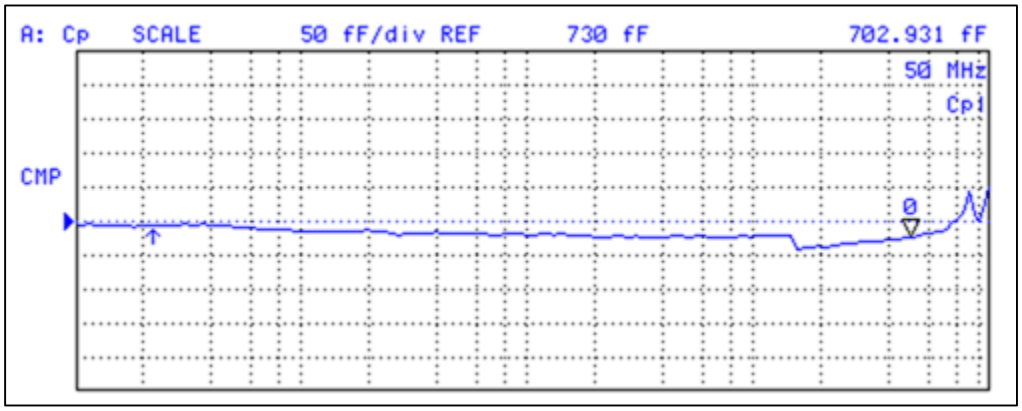


Fig.2. Coupling capacitance vs frequency for Transformer design 1

Fig.3. Transformer design 2 with 0.54 pF coupling capacitance

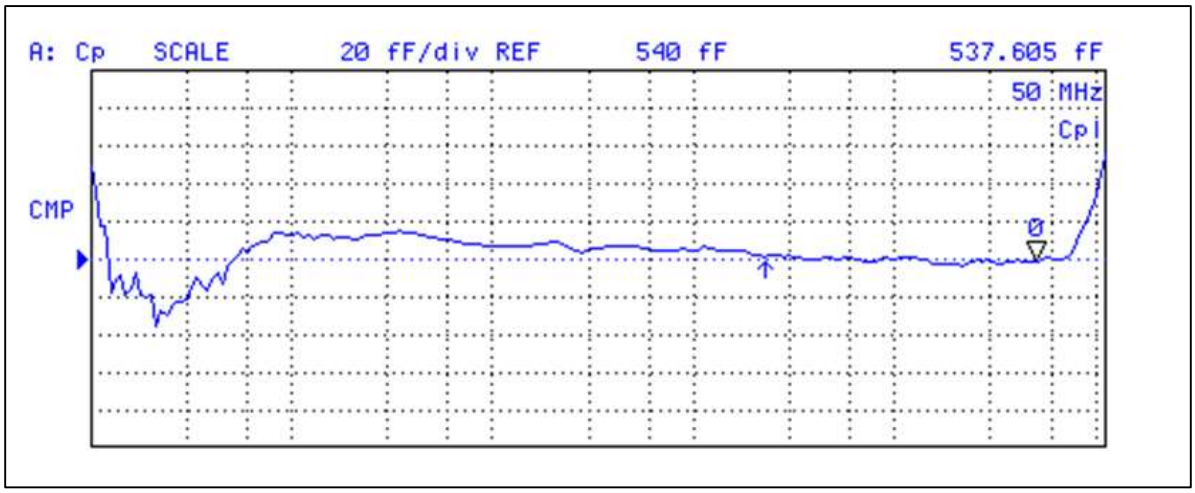


Fig.4. Coupling capacitance vs frequency for Transformer design 2

- **Intelligent Gate-Driver Design, Development and Testing with 10 kV SiC MOSFETs**

Fig. 5 shows the populated IGD board with all mentioned functions and specifications in Table I. It consists of mainly the sensing & measurement, comparators and ADC, communication and the driver stages. A 44pin ALTERA CPLD EPM3032A is used as the local brain. A 6pin, 40MHz serial 8bit, 3MSPS ADCs are used to read the critical measurements. The PWM and fault signals are routed through CPLD. The local Over-Temperature (OT), Over-Current (OC) and fault signals are generated using ultra-fast comparators.

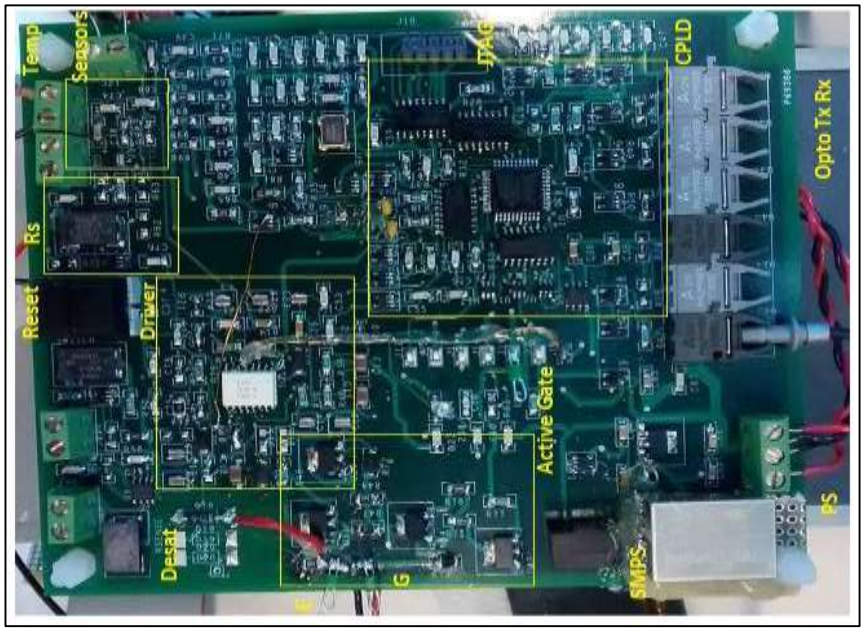


Fig. 5: Intelligent Gate Driver Circuit Board

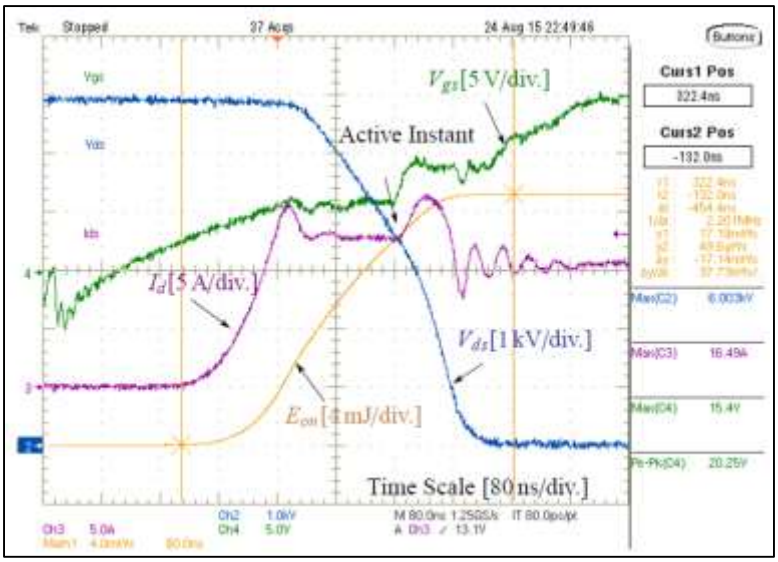


Fig. 6: Active Gating Double-pulse Test

The digitally controlled active gating is implemented and tested. Fig. 6 shows the DP (Double Pulse) test of the IGD (Intelligent Gate Driver) with the active gate driver function at 6kV.

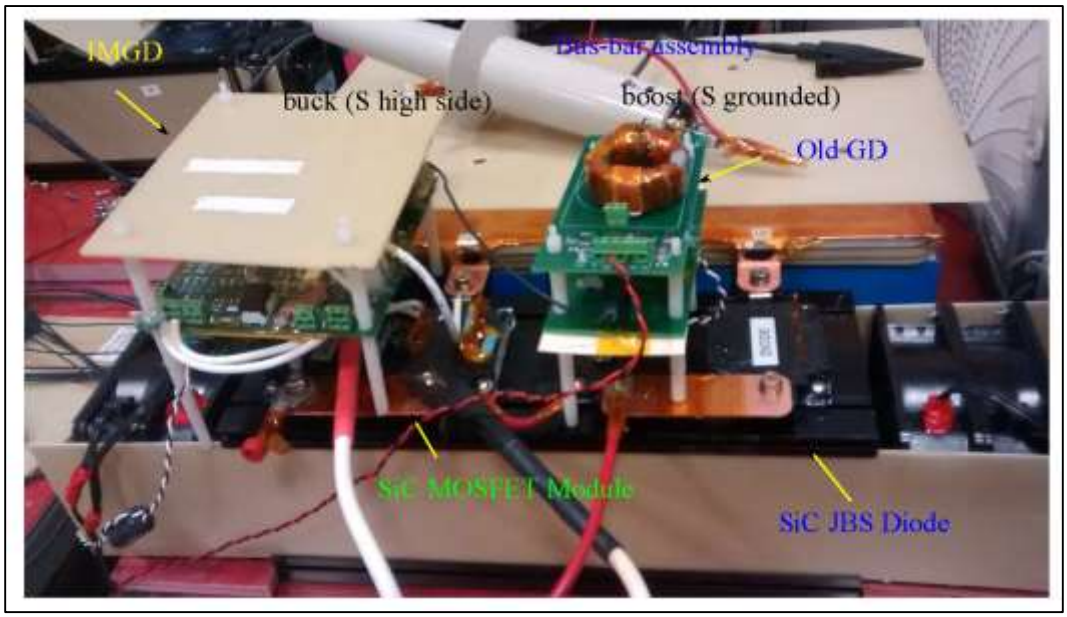


Fig. 7: Boost-Buck Setup

Fig. 7 shows the setup photograph for validating the MV IGD (Intelligent Gate Driver) with its basic functionality only.
Fig. 8 shows the results for 5kV operation for the IGD (Intelligent Gate Driver) at MV voltage potential. The boost input is 1.5kV and output is 6kV. The buck converter 10kV SiC MOSFET switch is now at a higher

potential so that its IGD (Intelligent Gate Driver) gets 5kV pulsating stress.

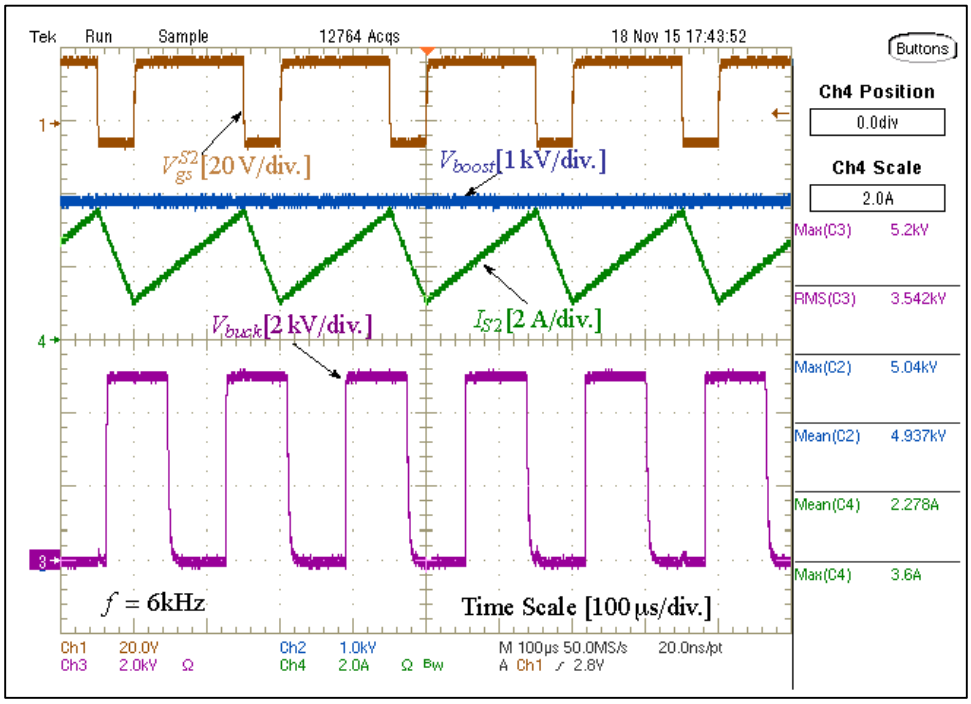


Fig. 8: 5 kV Boost-Buck IGD (Intelligent Gate Driver) Qualification Test Results

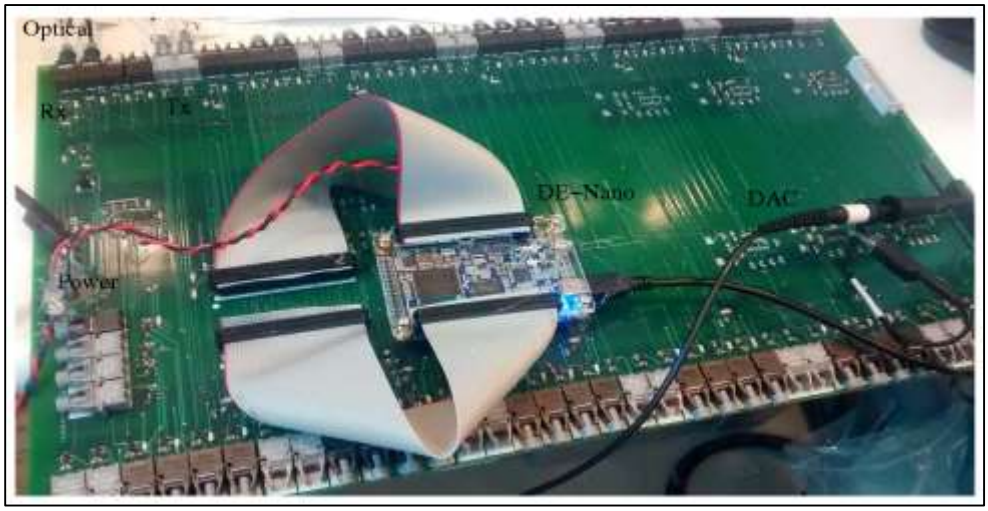


Fig. 9: IGD (Intelligent Gate Driver) Interface Circuit Board

Fig. 9 shows the populated interface board which communicates with all the IGDs of a MV converter. It has onboard DACs and FPGA board for implementing monitoring and data-logging functions. The interface FPGA transmits a common clock for IGD ADC operation and communication. The critical measurements can be converted by DACs for display. Based

on any abnormality or any fault signal from any particular IGD, all the IGDs can also be turned off together for MV converter safety.

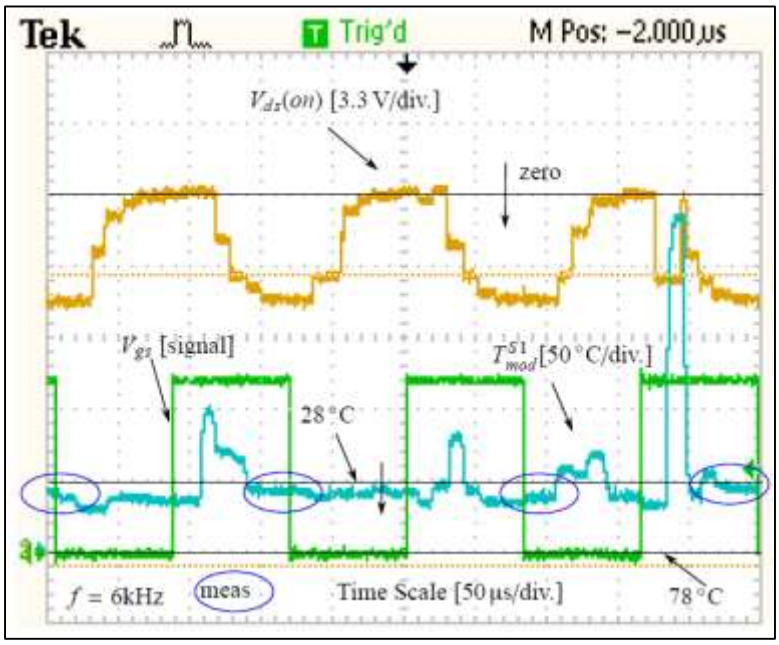


Fig. 10: 5 kV Boost-Buck IGD (Intelligent Gate Driver) Qualification Results on the Interface Board side

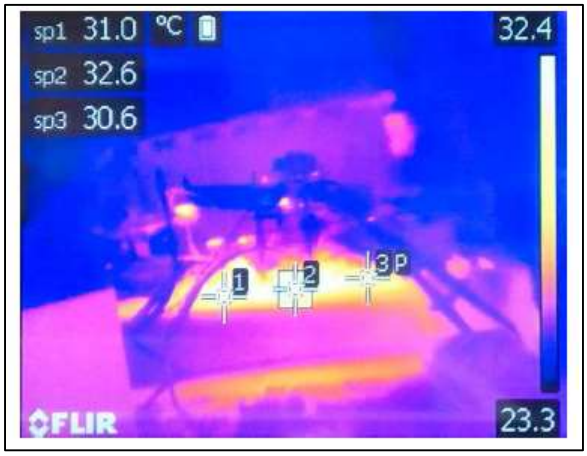


Fig. 11: Boost-Buck Test Thermal Photograph

Fig. 10 shows the optically transmitted Vds and temperature measurements coming from the intelligent gate-driver (IGD) out of the high voltage setup. Fig 11 shows the thermal photograph of the setup in Fig. 7 after 30 min thermal run at 5kV and 3kW power in boost-buck operation.

- **Three-Phase High Frequency Converter Design and Development using 10 kV SiC MOSFETs**

Three-phase MV high frequency converter with inverse power density of **4 m^3/MW** has been developed using Gen-I gate drivers and 10 kV/10 A SiC MOSFETs from CREE/POWEREX. The converter has been tested up to 5 kV dc bus voltage, 2.6 kV ac rms voltage, 3.7 kW, 400 Hz fundamental frequency at 10 kHz switching frequency. The waveforms captured are shown in Fig. 12. The MV converter has also been tested up to 3 kV dc bus voltage, 900 V ac voltage, 1.45 kW, 1 kHz fundamental frequency at 20 kHz switching frequency. The waveforms captured are shown in Fig. 13.

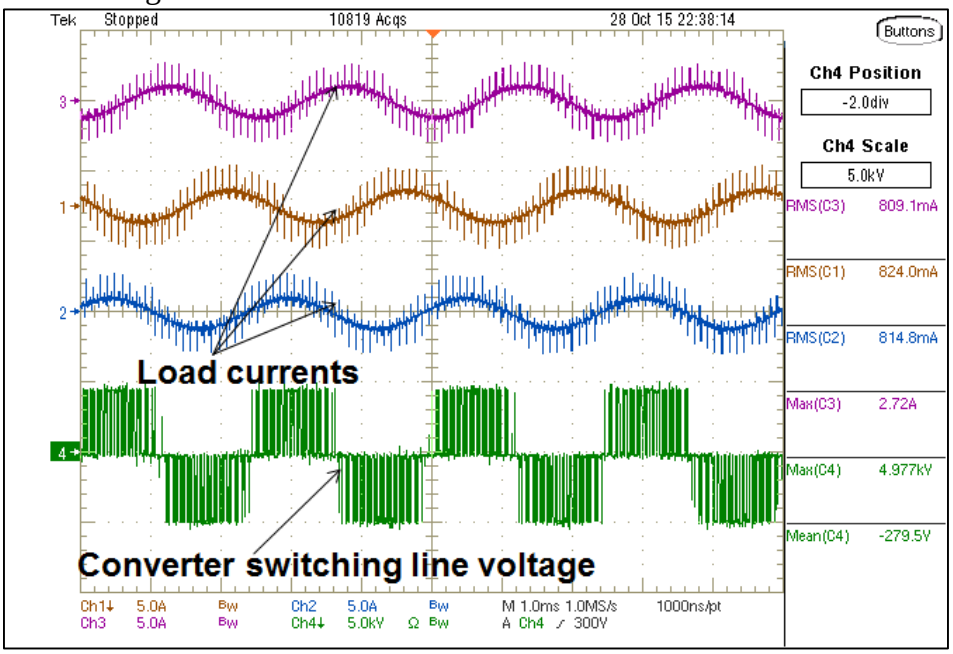


Fig. 12. Three-phase MV converter waveforms at 5 kV dc bus voltage, 2.6 kV ac voltage, 3.7 kW, 400 Hz fundamental frequency at 10 kHz switching frequency

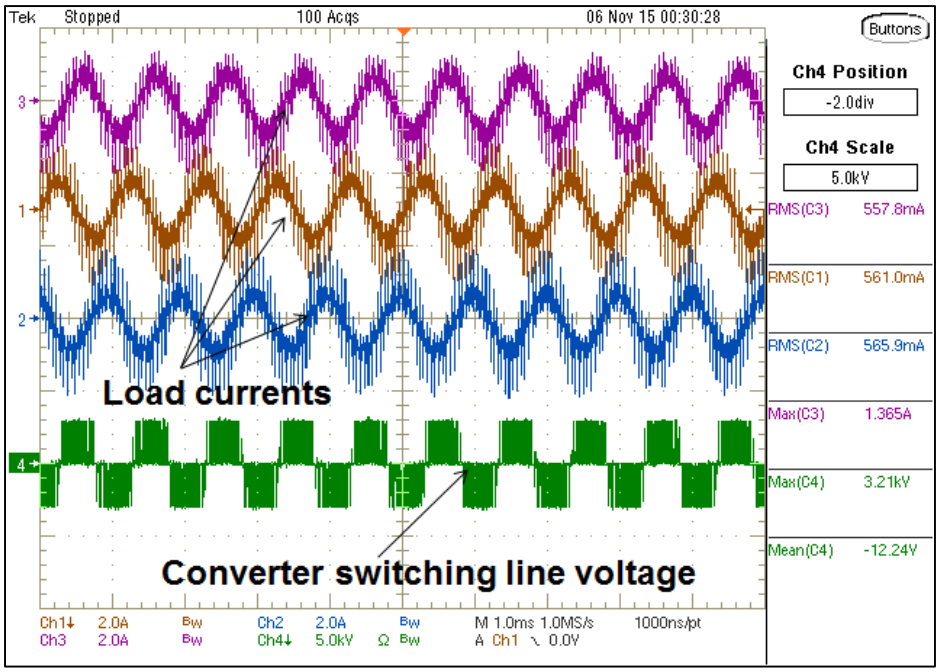


Fig.13. Three-phase MV converter at 3 kV dc bus voltage, 900 V ac voltage, 1.45 kW, 1 kHz fundamental frequency at 20 kHz switching frequency

Technology to Market: The developed intelligent gate driver (IGD) will be demonstrated to industry partners. It will be clearly shown how the developed gate driver will enable the medium voltage power conversion. A detailed HV GD specifications with industry partners will be developed for commercial HV IGD suitable for 15kV. We have had discussions with Toshiba and Eaton for evaluation of the IGD in their MV power converter systems in BP2 period. Leading industries like 3M, Dupont will also be involved in developing optimum high voltage insulation material for HV coupling transformer under high dv/dt, di/dt and high switching frequency of 10-20 kHz.

Plans for Next Budget Period If Funded: Work will continue on the Intelligent Gate Driver and the Three-Phase converter development. Gate driver test set-ups including boost converter, buck converter, buck-boost converter will be developed using APEI modules of 10kV SiC MOSFETs. In addition to these above test circuits, additional testing circuits with Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) will be developed for up to 10 kV . Test circuits for testing upto 10kV at elevated temperatures 150C and “Active Gate Driver” (AGD) suitable for 15kV isolation will also be developed. Three-phase converter with higher fundamental frequency up to 1kHz will be developed using APEI modules and tested at higher powers.

Project Output: The following papers have been accepted for presentation at Applied Power Electronics Conference 2016.

- Design and Evaluation of Isolated Gate Driver Power Supply for Medium Voltage Converter Applications
- Medium Voltage (≥ 2.3 kV) High Frequency Three-Phase Two-Level Converter Design and Demonstration using 10 kV SiC MOSFETs for High Speed Motor Drive Applications
- Series Injection Enabled Full ZVS Light Load Operation of a 15kV SiC IGBT Based Dual Active Half Bridge Converter
- A MV Intelligent Gate Driver for 15kV SiC IGBT and 10kV SiC MOSFET Performance Evaluation of Series Connected 15 kV SiC IGBT Devices for MV Power Conversion Systems
- Patent disclosures (2-3) are being developed to be file with NCSU OTT by Dec 2015.

Milestone Summary

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
4.11.1	Design, development and test of Gen-I GD at 10kV isolation, 10kHz for 10kV SiC MOSFETs	03/2015	Completed
4.11.2	Design, development and test Gen-II GD at 10kV isolation, 10 kHz for 10kV SiC MOSFETs with Vce(sat) de-saturation protection, current sense at 150C device Junction Temperature, Tj.	03/2015	Completed
4.11.3	Design, development and test Gen-III GD at 15kV isolation, 10 kHz for 10kV SiC MOSFETs with Vce(sat) de-saturation protection, current sense at 150C device Tj	09/2015	In progress. Design has been done and testing is in progress
4.11.4	Design, build and test HF transformer using Gen II GD with coupled Boost converter (TS2); Buck converter followed by Boost converter (TS3);	09/2015	Design completed. Prototypes made with coupling capacitances less than 1pF. Power modules have not arrived yet to make the converter system. Converters

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
	Buck-Boost converter (TS4) up to 15kV as test circuit setups		layout and other designs are complete.
4.11.5	Develop HV GD detailed specifications with industry partners to develop commercial HV GD suitable for 15kV. Develop detailed specifications with other industry partners for HV insulation requirements for HV coupling transformer under high dv/dt, di/dt and high switching frequency of 10-20 kHz to enable development of commercial HV GD suitable for 15kV	03/2016	This is work in progress – we have had preliminary discussions with Toshiba and Eaton to understand industry specifications requirements for IGD and testing and qualifications required for commercial MV power converters.
4.11.6	Test Gen-III GD thoroughly at 15kV isolation, 10 kHz for 10kV SiC MOSFETs with Vce(sat) de-saturation protection, current sense at 150C device Tj; with test circuit setups TS1 – TS4	12/2015 – we will get this completed by 3/2016	Work in progress; awaiting packaged devices from APEI.

Dr. Iqbal Husain

Organization: NC State University
Task No./Project Title: Task 4.12/SiC Inverter for Electric Vehicle Traction Drive
Technical Point of Contact: Dr. Iqbal Husain
Start date for internal NC State project: 02/01/2015

Project Objectives: This task includes the design, fabrication and testing of a 55kW automotive electric vehicle (EV) traction inverter using SiC power devices. The use of SiC devices allows the inverter to operate at higher switching frequencies and at higher temperatures resulting in significant efficiency gain, and size and weight reduction compared to the current Si-based technology. Variable switching frequency is used in EV traction inverters in the range of 2-10kHz with the higher end limited by the switching losses and the lower end dictating the DC link capacitor size. A 2-5X increase in switching frequency with SiC devices would improve the total harmonic distortion (THD) in the waveforms while gaining in efficiency, and simultaneously reducing the size of this capacitor module which is the most bulky and expensive component of the inverter package. The improved switching dynamics of the SiC devices characterized by much lower voltage overshoots will also help minimize the EMI filter components. Smaller, lighter and more efficient WBG inverters and electric machines also enhance fuel economy and reduce CO2 emissions, which would help the auto industry meet the aggressive corporate aggregate fuel economy (CAFE) requirements.

The goal at the end of year 1 is to deliver the hardware prototype of the 55kW automotive EV traction inverter using the 1200V, 100A SiC Mosfet and SiC diode power modules. A battery-pack voltage boosted inverter topologies and current source inverters (CSIs) was first be evaluated to identify the topology that can best take advantage of the SiC device features to reduce the footprint and significantly improve the power density and performance of the inverter. The boosted inverter topology allows the electric machines to be operated at speeds as high as 14,000 rpm, which will make the electric machine size smaller, compact and more efficient. The other advantages of voltage boosting are smaller battery-pack size, reduction in filter choke size, smaller DC-link capacitor, and reduction in wiring harness size.

Project's Contribution to the PowerAmerica Mission: The electric vehicle traction inverter using SiC technology is a higher risk RD&D activity with a substantial marketplace potential. The NC State team is focused on bringing this concept from TRL 3-4 to TRL 6-7 proving the viability of the concept in an "open-source" manner, so that the technology can be offered to the Institute partners and industry members for further commercialization and mass production. The project is the starting point of commercialization of a whole new product line for the automotive industry. With increasing investments in projects pertaining to transportation electrification, educating a new generation of engineers in the field of vehicle electrification is critical given the shortage of power electronics and motor drive engineers. Currently, 6 PhD students are being trained with WBG experience leveraging on another FREEDM project for electric vehicle motor design and controller development, so that they can contribute to the US workforce. The project also provides the platform to evaluate the fundamental concepts proposed by the PhD students. This task is motivating and training PhD students to innovate without losing focus of fabricating a practical EV traction inverter with metrics that would qualify for use in the current and future EV industry. The PowerAmerica mission towards commercializing and manufacturing is also addressed through discussions with Institute partners for adoption of the technology in their field of use.

Technical Approach: This project will design, fabricate and test a 55 kW automotive EV traction inverter using 1200 V all-SiC power devices. Three inverter topologies were analyzed using analysis and detailed switching circuit based simulations to identify and down-select the most appropriate inverter topology that can take the most advantage of the SiC features for the 55kW automotive traction application. Switching frequencies were selected though simulation and analysis for the inverters using SiC devices by evaluating the losses. This task was used to determine the optimal current rating of the power module. Other performance metrics included in the evaluation are: EMI/EMC component size savings and overall kW/kg power density of the packaged inverter. The specifications for inverter were developed through evaluation of the power module under normal and extreme operating conditions and requirements under fault modes for EV traction drives.

The project has a two prong approach where one is based on using the most suitable commercial-off-the-shelf SiC modules and another based on refined customized SiC modules with the minimized parasitic inductance from the SiC die to bus capacitor. The optimized thermal impedance from the coolant to the SiC die has been designed through multi-physics simulation and testing. Optimized gate driver for SiC 1200V power modules suitable for 100 kHz switching frequency operation with required shoot through gate protection has been developed. This gate driver design is scalable in terms of SiC 1200V power module current rating up to 500A. The gate driver will be tested in continuous mode (heat run test) for both the high-side and low-side gate driver with a developed buck-boost converter, which will be used to also validate the thermal performance of the power module.

The project is also investigating the cost, size and VA rating reduction possible of the passive components with the optimal choice of switching frequency. The passive components including the DC-link capacitors and EMI/EMC filters has been sized and selected evaluating the impact of SiC devices to enable dc bus film capacitors and their performance at high temperatures.

The system integration phase of work has begun with the assembly of the gate driver, SiC power modules and DC bus to develop the preliminary 55kW automotive traction inverter. The busbar design, and layout of the SiC devices, gate driver and the passive components have been completed. Initial testing of the inverter will be conducted with passive loads. Size, weight, and efficiency of the first prototype inverter will be obtained through measurements and experiments and will be quantified. This analysis and testing data will be used to perform the 2nd cut design for further improvement in the BP2.

Issues, Risks and Mitigations: No unexpected technical issues and risks have been identified.

Significant Accomplishments: There are four significant accomplishments made in this project within the 3 quarters of BP1: 1) Low profile (<6mm height) SiC device isolated gate driver; 2) Current ripple 10X reduction by interleaved bidirectional converter with small sized inductors; 3) Multi-physics based system modeling and simulation; and 4) Manufacture and assembly of parts for the SiC 55kW EV inverter.

Low profile (< 6mm height) SiC device isolated gate drive. The proposed ultra-low profile SiC MOSFET gate driver with wide operating temperature range (-40°C to 125°C) has been designed, fabricated and tested in NC State University as shown in Fig. 1. The Infineon isolated gate drive integrated chip 1ED020I12 is upgraded by Texas Instruments isolated gate drive integrated chip ISO5852S because of the improved common mode transient immunity, which is higher than 100 kV/μs @1500V with reinforced capacitive isolation technique commercialized in 2015. The ultra-low profile with < 6mm height is realized by the customized 500 kHz transformer with minimized parasitic capacitance between the primary and the secondary side. As shown in Fig. 2, the gate drivers are tested for both the high-side and low-side devices operating at 100 kHz with 0.5μs deadtime. The experimental results verified that 1200V SiC gate driver with desired maximum rise time of 100ns and fall time of 40ns have been achieved.

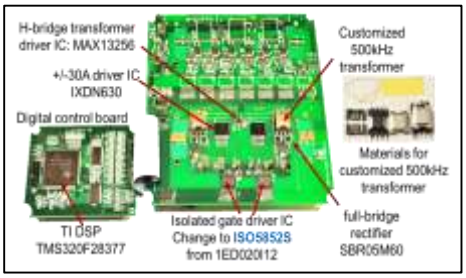


Fig. 1. Picture of the low profile gate driver.

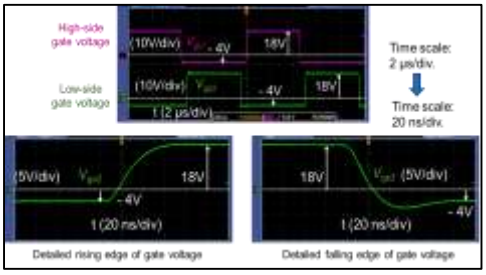


Fig. 2. Experimental waveforms of the gate drive.

Current ripple 10X reduction by interleaved bidirectional converter with small sized inductors. Fig. 3 illustrates that both the battery current ripple and dc link current ripple are effectively more than 10 X reduced by changing the parallel SiC MOSFETs into interleaved configuration in the bidirectional dc-dc converter. Moreover, the number of SiC semiconductors, the die area and the associated cost of SiC semiconductors are the as same as the non-interleaved converter. The total volume of the inductors is reduced 56% in comparison with the 2010 Toyota Prius boost inductor shown in Fig.4.

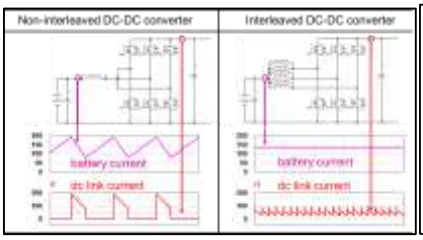


Fig. 3. Current ripple reduction.

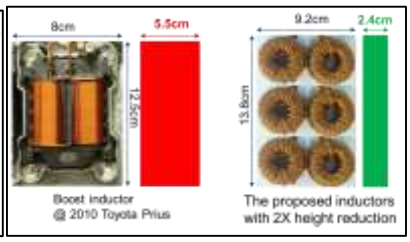


Fig. 4. Inductor size comparison.

Multi-physical system modeling and simulation. Fig. 5 demonstrates that the physical measurement-based CAD model yields accurate parasitic inductance and resistance using ANSYS Q3D Extractor simulation software. The simulation results verify that the lower height of the module is achievable with better performance of the parasitics. As illustrated in Fig. 6, power chip on bus adapted solution with double sided cooling for the devices and the passives is capable of achieving the low thermal resistance (0.1K/W from junction to case) and low electrical parasitics (10 nH phase loop parasitic inductance).

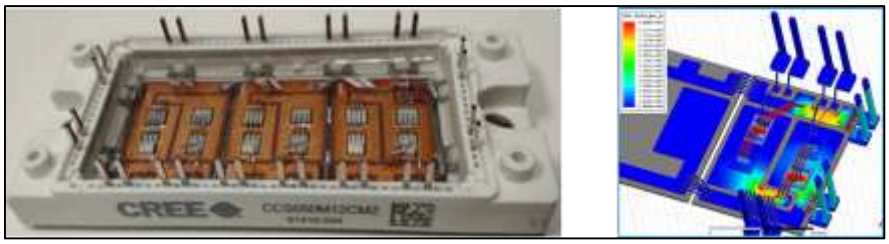


Fig. 5 Physical measurement-based ANSYS Q3D model.

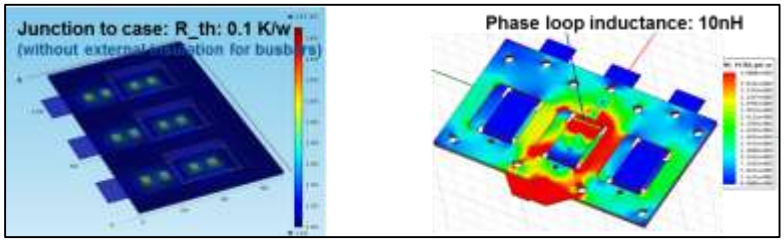


Fig. 6 Simulation results of the proposed power chip on bus adapted solution.

Manufacture and assembly of SiC 55 kW EV inverter. The software SolidWorks and Surfcam are used to generate CNC g-code to machine Aluminum for the cold plate. Stratasys PolyJet 3D printer Connex350 with rigid photopolymer (RGD525) is implemented to 3D print the custom turbulator for cold plate. The custom machined adapter Cu plate with Nickel plating is made as the cover. The Fel-Pro Karropak gasket sheet 3011 with 15mil thick is deployed to seal the coolant. The fabrication process of the cold plate is shown in Fig. 7 and the system assembly of the key components is drawn in Fig. 8. The picture of the preliminary 55 kW prototype is shown in Fig. 9.

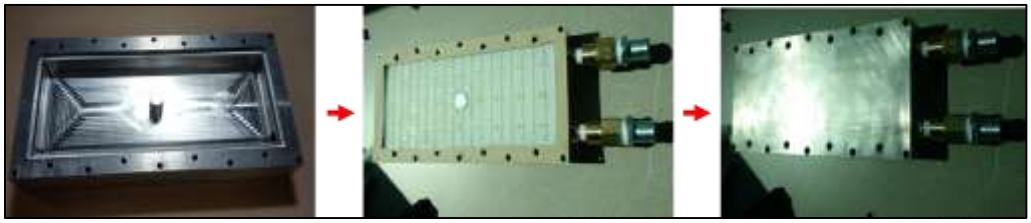


Fig. 7 Fabrication process of cold plate

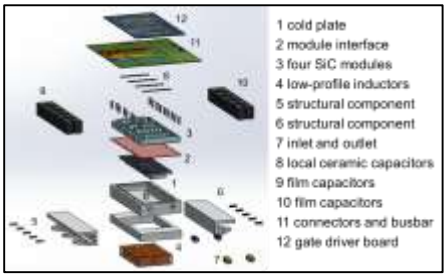


Fig. 8. System assembly of key components

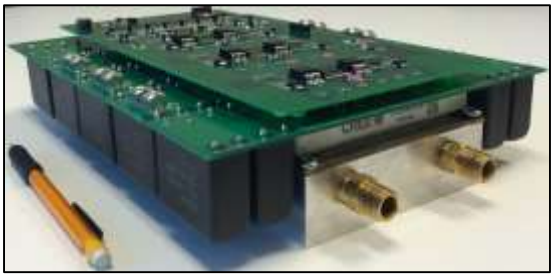


Fig. 9. Picture of preliminary 55 kW prototype

Technology to Market: Identified market segments for this task are the automotive, off-road traction, aerospace and other motor drive applications. The project development

platform supports manufacturers in the identified market segments. This task has established system requirements and platform capabilities allowing us to identify industrial partnerships. Partnership with 900V, 1200V or 1700V, 100-200A SiC MOSFET manufacturers and automotive OEMs and industrial drive manufacturers are essential. Discussions are underway with two Institute members, John Deere and Lockheed Martin for commercialization technology development.

Plans for Next Budget Period If Funded: North Carolina State University proposes to design, fabricate and test a 100kW automotive electric vehicle (EV) traction inverter with 1700V all-SiC power module. Based on the successful development of the 55 kW SiC EV traction inverter with interleaving boost in the BP1, the planned project in the next budget period will demonstrate that the boosted SiC inverter solution is capable of taking best advantage of the 1700 V SiC device features to reduce the footprint and significantly improve the power density and performance of the 100 kW EV traction drive. The 100kW design is targeted with a power density of 6.25kW/L, 6.25kW/kg, >98% system efficiency, and <5% THD. The power level and performance metrics proposed is going to provide the automotive industries with the most high performance EV traction inverter that has been reported.

All major components including power module package, cold plate, filter inductor, capacitor, bus bar and connector, gate driver, sensors and DSP control board will be holistically developed in the mechanic, thermal, electric and electronic multi-physics layers to meet the efficiency, power density and specific volume requirements of 100 kW EV traction inverter. The commercial-off-the-shelf SiC modules and refined customized SiC modules with the minimized parasitic inductance from the SiC die to bus capacitor and the optimized thermal impedance from the coolant to the SiC die will be designed, simulated and tested.

Project Output:

1) Conference paper: Adam J Morgan, Yang Xu, Douglas C Hopkins, Iqbal Husain, Wensong Yu, "Decomposition and Electro-Physical Model Creation of the CREE 1200V, 50A 3-Ph SiC Module," IEEE APEC, 2016.
2) A disclosure in NCSU was submitted. Disclosure Number 16051: Double-sided cooling power chip on busbar (PCoB) power module.
3) In preparation of disclosure of an inverter topology for electric vehicle traction application, which has unique features including elimination of additional boost stage for three-phase inverter with wide voltage range, elimination of the bulky and expensive DC link capacitor, and taking advantage of WBG device high frequency capability while eliminating the output common-mode issue.

Milestone Summary

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)

M4.12.1.1	Comparative efficiency and size evaluation results of three 55kW EV traction inverter topologies	Month 1-3	Completed
M4.12.1.2	SiC EV traction inverter design specifications for 55kW power delivery	Month 1-3	Completed
M4.12.2	1200V SiC gate driver with expected rise time of 100ns and fall time of 40ns	Month 4-6	Completed
M4.12.3	SiC EV traction inverter passive component sizing with 20% reduction in size and weight compared to Si-based inverter	Month 7-9	Completed
M4.12.4	Preliminary 55kW SiC EV traction inverter hardware testing with passive loads	Month 10-12	To be completed

Dr. Srdjan Lukic

Organization: North Carolina State University
Task No./Project Title: Task No. 4.13/Medium Voltage Fast Charger
Technical Point of Contact: Srdjan Lukic
Start date for internal NC State project: 02/01/2015

Project Objectives: The objective of this task is to design and build a medium voltage electric vehicle (EV) fast charger using WBG devices. The MV rectifier design that is highly flexible and permits wide input and output voltage variation, can also serve as a building block for powering DC data centers, industrial automation, and other DC power distribution systems. The motivation for introducing a WBG solution for medium voltage (MV) rectification is: (1) potential for higher efficiency (2) higher power density and (3) system-level cost savings. In the case of the EV chargers, the introduction of high voltage WBG devices allows single phase MV charger to replace the three phase 480V equivalent. This approach substantially reduces the electric charging infrastructure costs, since it eliminates the need for running three phase lines from the distribution system to the fast charger installation point, while also eliminating the bulky and expensive three-phase, low-frequency transformer. By feeding power to the fast charger directly from a single phase medium voltage line, the utility or site owner can substantially reduce the installation cost (EPRI has estimated that the installation costs would be reduced by 50% or more, depending on the site), and reduce the system footprint (important criteria in densely populated areas). Fig. 1 shows the projected volume comparison between the proposed MV fast charger and the ABB Terra 51. As a result, the WBG solution would have a distinct competitive advantage if it can be manufactured at parity or even at a premium over the conventional solution.

The objective of this project is to design and build a MV EV fast charger. The proposed converter utilizes off-the-shelf SiC devices to step down and rectify the single phase medium-voltage input. The first-year goal was to demonstrate a 25kVA (stretch goal: 50kVA), 2.4kVac/400Vdc system with very high efficiency (above 95%), high power quality (PF $\geq$ 0.98, THD $\leq$ 2%), and reduced footprint (3x size reduction). The NC State team will bring this concept from TRL 3-4 to TRL 6-7 proving the viability of the concept in an "open-source" manner, so that the technology can be offered to the Institute partners and industry members for further commercialization and mass production.

Project's Contribution to the PowerAmerica Mission: Due to the unique properties of the WBG devices, a simple drop-in design for WBG is not feasible and existing topologies and controls cannot be used directly, without redesign. To enable immediate commercialization efforts at TRL6-7, additional RD&D at TRL3-5 must be conducted to build an industry business case for WBG that reduces risk. The MV rectifier using SiC technology is a higher risk RD&D activity with a substantial marketplace potential. The fast charge prototype will be a building block that can be a starting point for commercialization of a whole new product line serving a set of emerging applications. The developed technology can be attractive value-add to the Institute current and future members. Importantly, the project involves two PhD students, one Visiting Scholar, and six undergraduate students in the project. The undergraduate students are engaged through the Senior Design program and on volunteer basis.

Fig. 1. Volume comparison of the MV Fast Charger to the ABB Terra 51; all dimensions are in mm

Technical Approach: The approach taken to achieve our stringent performance goals, while delivering a highly flexible, modular, and

scalable MV rectifier platform, was to systematically trade-off topologies that support these goals. The key criteria in choosing the optimal topology were: (1) efficiency over a wide output voltage range (2) power density and (3) modularity. Availability of commercial SiC devices that can serve the application was another design constraint. The team chose to work with commercially available devices to minimize risk and deliver a working prototype by the end of BP1. The result of the topology tradeoff was the selection of so-called the Multi-Cell-Boost (MCB) topology, shown in Fig. 2. The MCB topology features three input-series-output-parallel-connected dc/dc converter modules. Fig. 2 shows the details of a single module, including the selected switching devices. The topology can be optimized to perform at high power density, high efficiency, low cost, use a relatively small number of switches and exhibit high reliability.

With the topology and the devices selected, the team proceeded to do develop a high-fidelity model of the converter. The device models were extracted from double pulse tests, and all passive components were designed, built and characterized to extract detailed operation and loss models. A breadboard prototype of the system was then built to test out key system components. Breadboard prototype performance was tested against simulation results to provide further confidence in the system model. The module was fully tested at rated power, and the results were used for further system optimization and simulation model validation. With the module developed, passive components, and system layouts were further optimized, and redesigned, before the entire system was built. The entire system prototype is currently in testing.

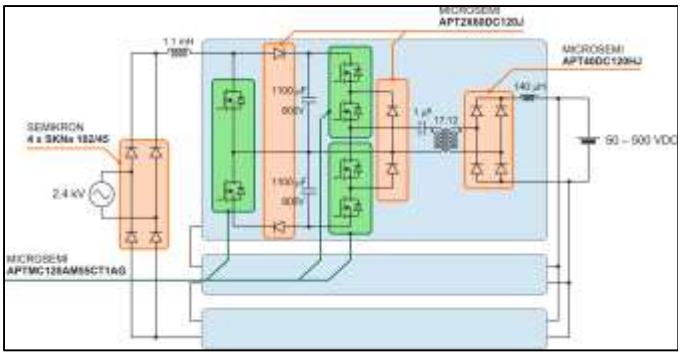


Fig. 2. Multi cell boost topology selected for MV fast charger implementation.

Issues, Risks and Mitigations: The team has not faced any major issues in executing the project. In the longer-term, two issues will need to be resolved for a successful demonstration and productization of the MV charger platform. First, due to the power supply limitations in our laboratory, the team is having challenges supplying 50kVA to the charger at 2.4kV. This will be resolved in BP2 by possibly purchasing an additional transformer. Another concern is the fault tolerance of the controller implementation under fault conditions. Since fault conditions cannot be tested in hardware in a safe manner, controller hardware-in-the-loop (HIL) approach is typically used. Due to the limitations of the controller HIL system that is available at NC State, it was not possible to perform these tests. Instead, the control algorithm that was thoroughly tested in simulation was implemented on a Texas Instruments microcontroller. In BP 2, we will explore purchasing additional components to expand the capabilities of the Opal RT HIL platform. Finally, determining efficiency at high voltage levels will be a challenge when the complete system is tested. This will be resolved by testing sub-systems individually, and calculating the overall efficiency. Additionally, the team has procured a high-voltage isolated voltage probe, which will allow to precisely measure the input voltage.

Significant Accomplishments: The project goal in BP1 was to demonstrate a 25kVA (stretch goal: 50kVA), 2.4kVac/400Vdc MV fast charger with efficiency above 95%, high power quality (PF ≥ 0.98, THD ≤ 2%), and reduced footprint. To achieve this goal the team has undertaken three major tasks: (1) simulate, design, build and test a breadboard prototype as proof of concept that performance goals are attainable; (2) further optimize system based on high fidelity simulations and experiments; and (3) develop, design, build, and test the MV fast charger prototype. Our current projection is that the system prototype will meet or exceed all of the performance criteria. Importantly, the team is on track to meet the stretch goal of delivering 50kW power rather than 25kW.

Breadboard Prototype: Based on the system topology presented in Fig. 2, the MV fast charger was first modeled, and it was shown that the converter has the capability to meet all of the design goals. All converter parameters were determined from simulation, and the components were built and tested. The resulting validated models where then integrated into a high fidelity simulation for further optimization.

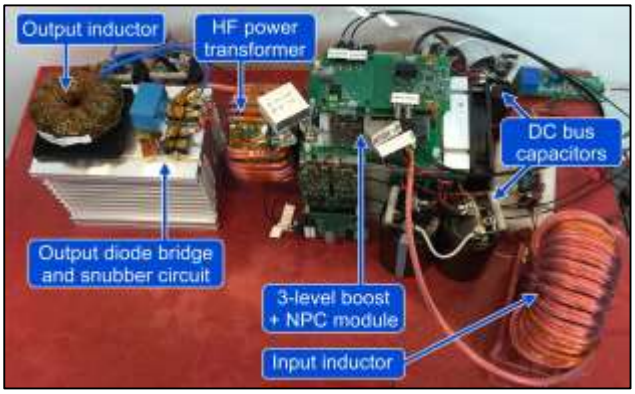


Fig. 3. MCB module breadboard prototype tested at 16.7kW

The MCB breadboard prototype module operation was simulated and the module efficiency was obtained by using thermal descriptions of the semiconductor components, obtained experimentally. The control structure makes use of three nested control loops that ensure (1) high power quality through interleaved control of the boost/power-factor-correction stage, (2) balanced capacitor voltages at the output of the boost stage, and (3) precise output voltage control of the neutral-point-clamped (NPC) DC/DC stage that delivers power to the battery.

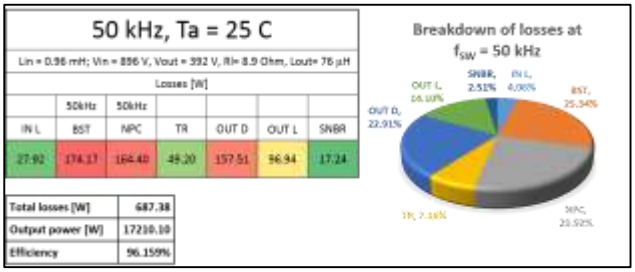


Fig. 4. Simulated module efficiency and breakdown of power losses.

With the system modeled, and the control approach validated in simulation, the breadboard prototype was constructed and tested. The system is shown in Fig. 3. The prototype features a single MCB module shown in Fig. 2, and the input rectifier stage. The module was tested up to 16.7kW, which corresponds to the full system power of 50kW when all three modules are in operation. The breadboard prototype features a custom designed bus-bar with minimal leakage inductance, transformer design with fully characterized parasitic inductance and capacitance, custom designed transformers, input and output inductors, custom designed isolated sensing, signaling, and control. Gate drivers, and switches are off-the shelf Cree/Wolfspeed products.

With both the breadboard prototype and fully validated simulation model available, system efficiency and performance were tested. The simulation results of module efficiency and breakdown of losses are shown in Fig. 4. The corresponding experimental result was measured at 95.94%, which is sufficiency close to the experiment, verifying that

the developed component models are valid. Referring to the simulated losses in Fig. 4, the bulk of the losses occur in the boost stage (BST), the neutral point clamped (NPC) stage, and the output diode rectifier (OUT D) stage. All active switches were operated at a frequency of 50kHz.

System Optimization: Based on the experimental results, and system simulation, the team determined that the system efficiency can be improved further through control and component optimization. In order to increase the overall system efficiency, the switching frequency of the interleaved boost converters was reduced while still meeting the stringent requirement of total harmonic distortion (THD). As a result, the switching frequency was reduced to 25 kHz, at which point the THD reached the imposed limit of 2%. Additionally, it was shown that increasing transformer leakage inductance allows the outer switches of the NPC to be soft-switched, reducing the switching losses. The optimal value of this leakage inductance should be large enough to ensure soft switching, but as small as possible to minimize the reactive power flow through the main power delivery path. Through simulation and experiment, we have determined the optimal value of the leakage inductance as a function of the load current. Based on these results, we have selected to build a transformer with leakage inductance of 20 µH, which enables soft switching of the outer NPC switches for loads exceeding 30A.

Changing the switching frequency of the interleaved boost converters to 25 kHz, and using an optimized transformer further improves efficiency. As shown in Fig. 6, the optimized design reduces the boost (BST) stage and the NPC stage losses, resulting in the simulated efficiency of the entire 50 kW system of 96.6%, which corresponds to a 15% reduction in losses. Additional efficiency improvement can be obtained through (1) replacing the output rectifier with synchronous rectification (2) using an active snubber topology which recirculates the snubber energy and (3) designing a saturable inductor to achieve soft switching of NPC outer switches across the entire load spectrum.

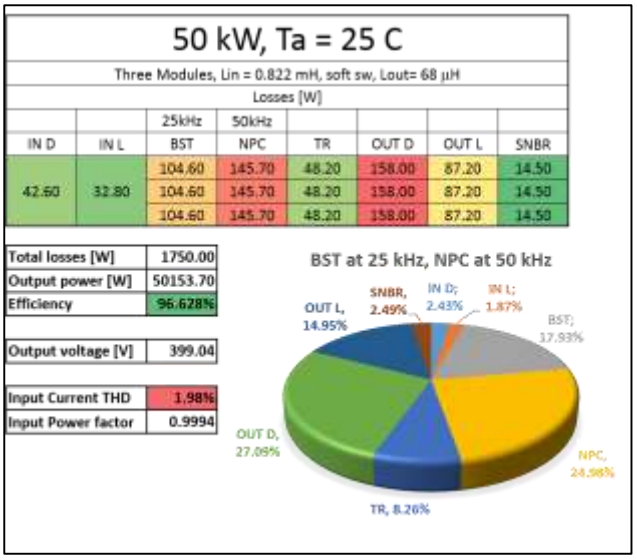


Fig. 5. Simulated efficiency of the 50 kW system with boost switching frequency reduced to 25 kHz and slightly improved input and output inductors

Fully Integrated System Design: The team is currently in the process of designing and building the optimized EV fast charger prototype. A 3D rendering of the optimized system is shown in Fig. 6. The system projected volume is compared to the state of the art ABB 51 EV fast charger in Fig. 1. The system shows a significant reduction in size, compared to the state-of-the-art low voltage chargers with low-frequency step-down transformer. Currently, the team is in the process of building and testing the complete 50kW prototype, shown in Fig. 7. The new design incorporated the new transformer design, optimized, custom-designed film capacitors, redesigned input and output inductors for further volume improvement, redesigned protection circuitry, and an entirely new bus-bar construction.

Technology to Market: The focus of the team in BP 1 was to demonstrate the MV fast charger as a proof-of-concept, to quantify cost/ performance tradeoffs, and deliver a platform technology that can serve multiple applications including EV fast chargers, data centers, and military applications. As the system costs, and performance are better understood, the team is reaching out to industry, including Duke Energy and Eaton. Duke energy could serve as a potential demonstration partner, and ultimately a customer, given the MV fast chargers would be very attractive to the utilities. Eaton could serve as a commercialization partner, given that Eaton currently builds and sells conventional EV fast chargers. The team is also working with the NCSU Accelerating the Commercialization of Technology (ACT) Program at the Poole College of Management at NC State, to define a student project in BP2 to explore commercialization potential for the project. Additionally, the team is working with a Senior Design team that is responsible for designing a human machine interface for the MV fast charger. The senior design team has also performed an initial market analysis for the product, and has determined that the product can be sold at a premium, due to the cost effective installation.

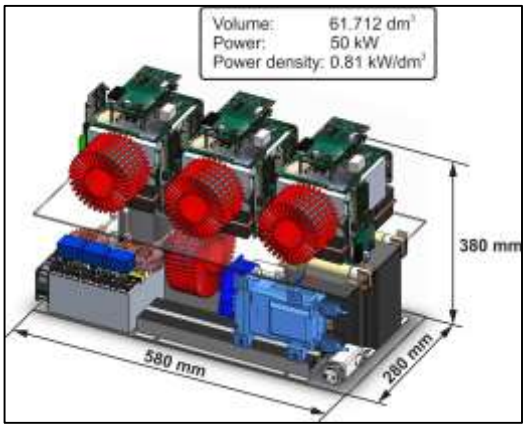


Fig. 6. 3D rendering of the optimized fast charger.

Fig. 7. EV fast charger prototype in develpment.

Plans for Next Budget Period If Funded: If funded, in BP 2 we plan to focus on the following tasks:

- *Robustize System Control and Protection:* Control approach will need to be further improved to implement additional protection layers. Importantly, the entire protection approach will be re-evaluated taking into account different operating scenarios.
- *Efficiency and Power Density Improvement:* The team will continue to fine-tune the prototype to exceed 95% efficiency target, and further improve system power density. Specifically, the team will focus on eliminating the low frequency auxiliary transformer (occupies 5.4% of the total system volume) with a high-frequency equivalent. Eliminating the low frequency auxiliary transformer also reduces the stand-by losses.
- *System Packaging:* In BP 2 the team will package the fast charger for outdoor installation. The developed system will abide to all pertinent standards. The team will spend a significant effort on designing an appealing and functional enclosure for the charger unit.
- *System Installation and Comprehensive Testing:* The team will install the charger at the NC State Keystone Science Center parking lot. The parking lot is publically accessible, and the team has access to a fast-charge enabled Nissan Leaf vehicle. This public installation provides the team easy access to the charger, and reduces demonstration costs, as the parking deck has installed conduit between the charging spot and the main laboratory, allowing the team to provide 2.4kV to the deck by running cables through the conduit.

1. Project Output (publications, conference presentations, awards/recognition, IP disclosures, patent filing; list all)

In BP 1, the project has received significant recognition, serving as the showcase project for the Power America Institute d in BP1. The project summary has been presented at a number of conferences by the Power America Staff. The NC State team also plans to present the paper listed below:

Srdjan Srdic, Chi Zhang, Xinyu Liang, Wensong Yu, and Srdjan Lukic, "A SiC-based Power Converter Module for Medium-Voltage Fast Charger for Plug-in Electric Vehicles" accepted for presentation at *2016 IEEE Applied Power Electronics Conference*, Long Beach, CA, March 2016.

Milestone Summary

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
4.13.1.1	Demonstrated target performance based on preliminary system simulation.	3/1/2015	Complete
4.13.2.1	High Frequency transformer built and tested	6/1/2015	Complete
4.13.2.2	Gate Driving Circuit designed and tested	6/1/2015	Complete
4.13.2.3	Detailed system simulation, with experimentally validated component models demonstrating target performance	6/1/2015	Complete
4.13.3.1	System operational at reduced power (5kVA) achieving high power quality	9/1/2015	Complete
4.13.4.1	System operational at rated power of 25 kVA at 2.4 kVac input and 400Vdc output and meeting all design goals	12/1/2015	Ongoing

Dr. Veena Misra

Organization: North Carolina State University
Task No./Project Title: 2.8.1: SiC channel mobility enhancement 2.8.4: Enhancement mode GaN devices
Technical Point of Contact: Dr. Veena Misra, Professor of Electrical and Computer Engineering
Start date for internal NC State project: 02/01/2015

Project Objectives: The overarching objective of this project is to develop highly manufacturable and high mobility SiC metal-oxide-semiconductor field effect transistor (MOSFET) devices for medium voltage (<1700V) power switch device application and enhancement mode GaN devices for 600V application through device innovation, refinement and standardization to substantially reduce the cost per Ampare of the device. Particularly, SiC device with interface engineering using rare-earth oxide/silicate layer will provide excellent interface resulting in high channel mobility while atomic layer deposited SiO_2 bulk dielectric will provide the low leakage and highly reliable gate dielectrics. The performance of proposed SiC device would surpass that of conventional SiC devices in terms of high mobility and high positive threshold voltage (> 3V). GaN device with a novel FLASH approach by high quality dielectrics will realize normally-off device operation without any performance degradation. The specific objectives in BP1 are to (a) demonstrate highly reliable atomic layer deposited (ALD) dielectrics to have dielectric strength of 8 MV/cm, (b) develop high mobility (>50cm^2/V-s) SiC lateral MOSFET with V_T shift is less than 0.5V under 4 MV/cm of DC bias stress, and (c) demonstrate enhancement mode GaN device using a new transistor device structure and operating method that enables high efficiency and normally-off GaN devices.

Project's Contribution to the PowerAmerica Mission: The main goal of the Power America Institute is to build the large-scale manufacturing of wide bandgap (WBG) semiconductor based power electronics. The WBG electronics can realize smaller, faster, more efficient and reliable power electrics as compared to the devices made from Silicon (Si). The proposed pricing targets of the Power America Institute in 2015 is set to $0.3/Amp for 1200V switch that is 20% reduction as compare to the current market price. This can be realized in several ways such as reduction in discrete device cost and high volume manufacturing. Our first approach for device innovation is based on separate and independent control of the interface layer by incorporating ultrathin silicate layer resulting in 4 times high mobility than current state-of-the-art SiC MOSFETs. Our second approach is based on atomic layer deposition method that has proven to provide a high quality and low damage dielectrics for both SiC and GaN devices. ALD is currently using in high volume Si CMOS manufacturing so this technique can be implemented in high volume SiC foundry. Moreover, our SiC device does not require any additional mask, it could be easily implement in the foundry process with the Power America Institute .

Technical Approach:

SiC device: To break mobility-threshold voltage trade-off, we proposed a novel approach using ultra-thin group III and rare-earth oxide layer as an interface control layer and atomic layer deposited low damage and low defects SiO_2 as a main gate dielectric in order to achieve high mobility and high threshold voltage at the same time. It is known that the thermal oxidation process should be avoided to limit the carbon related defects or the transition layer between SiO_2 and SiC substrate. High quality deposited SiO_2 is the ideal candidate to replace the thermally grown SiO_2. In our proposed work, we utilized Atomic Layer Deposited (ALD) SiO_2 as a main gate dielectric material because ALD is known to provide several advantages such as low

temperature processing, conformal deposition, and precise thickness control over conventional dielectric deposition method such as thermal oxidation and plasma enhance chemical vapor deposition (PECVD). In our previous work, ALD SiO_2 dielectric on SiC substrate has been demonstrated in and it was confirmed that the peak field effect mobility value remains similar as thermal oxide results. Furthermore, a high quality deposited gate dielectric is required when ultrathin interface engineering layer is deposited for the interface control at the SiO_2/SiC interface, which cannot be achieved using thermal oxide. In order to achieve high mobility a novel interface engineering using Rare-earth oxide has been proposed and experimentally demonstrated. Rare-earth oxides such as La_2O_3, Gd_2O_3, Dy_2O_3, and Er_2O_3 are extensively studied as a potential candidate for CMOS high performance devices since these dielectrics have high dielectric constant (20~30), reasonable energy bandgap (5 eV~6 eV), and thermally and chemically stable with Si substrate. For example, La_2O_3 have been the focus of investigation because of its combination of high dielectric constant, large band offsets compared to silicon, amorphous phase stability, good chemical stability, and tunability of device threshold voltage. Moreover, La_2O_3 has also been studied to passivate the interface states for GaAs and GaN interface. The high reactivity of silicate formation as well as proven thermal stability of La_2O_3 layer on Si motivates our proposed study where the low quality SiO_2 layer growth at SiO_2/SiC interface can be converted to stable and good quality silicate layer when La_2O_3 layer is presented at the SiC interface. Moreover, we have found that the atomic layer deposited SiO_2 has net negative fixed charges that prevent negative shift of threshold voltage. Thus we could achieve high mobility values for a given V_T that has not been possible by the conventional SiC oxidation and high temperature 'NO' annealing process. Therefore, the interfacial layer, consisting of ultra-thin La-silicate layer was used to suppress the interfacial layer growth resulting in large reduction of the interface state density while controlling the device threshold voltage using the ALD SiO_2 layer as a main gate dielectric.

GaN Device: Normally-off or enhancement mode operation devices are essential for power device applications such as the SST and other power converters in order to maximize efficiency and achieve safe operation. However, conventional GaN heterojunction field effect transistors (HFETs) are normally on (depletion mode) due to a buried channel formation. Moreover, off state gate leakage current due to the conventional Schottky gate dissipates power in the off state resulting in an efficiency reduction. Gate leakage suppression can be achieved via the use of insulators between the gate metal and AlGaN barrier, however the device threshold voltage (V_T) becomes even more negative due to the increased separation of the gate from the channel. Our approach is to develop novel normally off GaN power devices by using a charge storage layer in the gate stack associated with atomic layer deposited dielectrics such that the device threshold voltage can be modulated and controlled. By using an atomic layer deposited SiO_2 tunnel dielectric, Hf based charge storage, and a high-k blocking dielectric; low leakage, high performance, normally off GaN devices are realized.

Issues, Risks and Mitigations: Most of the technical risks in this project are mitigated by the extensive expertise of the Power America Institute in the device

technology and commercialization of wide bandgap semiconductors and by our technical approaches that have already taken into account risks associated with device fabrication. We have been working on gate stacks and dielectrics on various substrates from silicon, Ge, GaAs to wide bandgap semiconductors (SiC, GaN) and have all the process flows for device fabrication. We have witnessed, studied, and helped solve a wide variety of unanticipated problems in these technologies, such as threshold voltage instability and variation, effect of processing conditions (post deposition annealing and post metallization annealing), low field-effect mobility in SiC MOSFETs, passivation of AlGaN/GaN device and reliability. As there will undoubtedly be unanticipated issues to address in SiC and GaN device reliability and large-scale manufacturing, it is through our vast cumulative experiences in the WBG semiconductor field inside the Institute and our large professional network within this community to solve these issues.

Significant Accomplishments:

SiC Device: In BP1, we have demonstrated excellent 4H-SiC channel mobility employing interface engineering by La-silicate with ALD SiO_2 dielectric while maintaining high positive threshold voltage (>3V). The interfacial layer, consisting of ultra-thin La-silicate layer was used to suppress the interfacial layer growth resulting in large reduction of the interface state density while controlling the device threshold voltage using the ALD SiO_2 layer. As shown in Figure 1, the basic electrical characteristics with 1nm La_2O_3/30nm SiO_2 are much improved. The sample with 1nm La_2O_3/30nm SiO_2 layer shows significantly lower low-field (< 7 MV/cm) gate leakage compared to the one without La_2O_3 layer. The leakage reduction can be attributed to improved carrier injection interface without the interfacial layer and the high-k/low-k dielectrics stack which modulates the electrical field distribution in the gate dielectrics. These initial results were very encouraging because all dielectric deposition can be deposited at relatively low temperature (< 300 ^oC) and relative short anneal time (1min at 900 ^oC) as compared to conventional oxidation (>1175 ^oC) and NO anneal (2 hours at 1175 ^oC).

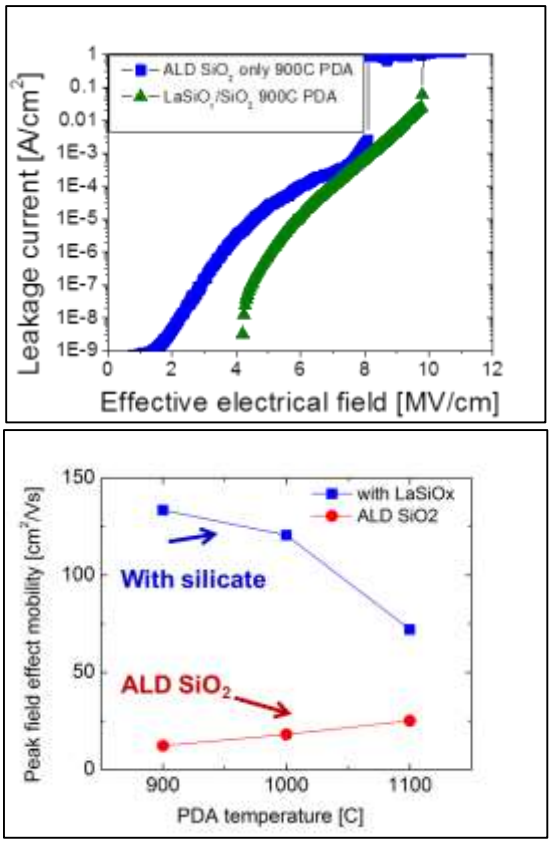


Figure 1. (a) Gate leakage results with and without 1nm La_2O_3 interfacial layer after 900°C N_2O annealing for 1min. Low field leakage as well as the breakdown field are improved with 1nm La_2O_3 incorporation. (b) Peak inversion channel mobility of lateral MOSFET as function of PDA temperature. Improved mobility was clearly seen with La2O3 incorporation.

Lateral MOSFET were also fabricated on Si face of p-type 4H-SiC Fig. 1 (b) shows the mobility comparisons with and without 1nm La_2O_3 interfacial layer. The sample with 1nm La_2O_3/30nm SiO_2 shows the highest mobility with a peak mobility of 133.5 cm^2/V-s which is at least 5X higher than typically obtained using thermally oxidized dielectric with high temperature NO annealed, for the similar positive V_T value. The gate leakage of the transistor remains at least 6 orders of magnitude lower that drain current in on state. In BP1, the reliability of lateral MOSFET has initiated and V_T instability under high electric field has evaluated. As shown in Figure 2 and summarized in Table 1, the V_T shift under 4MV/cm stress was less than 0.5V that is achieve decision point milestone for this project in BP1 and is very promising. For SiC MOSFET with 0.3nm La_2O_3/30nm ALD SiO_2, the mobility value is 48 cm^2/V-s and the threshold voltage is about 5V. After high temperature forming gas anneal, the mobility is enhanced to 60 cm^2/V-s with V_T shift is less than 0.5V under 4MV of DC bias stress.

Table 1. Reliability (V_T shift) and mobility summary of 0.3 nm La_2O_3 /30 nm ALD SiO_2

	V_T shift at 3 MV/cm	V_T shift at 4 MV/cm	Peak mobility $Cm^2/V\text{-}s$
900°C PDA No FGA	1.6	1.93	40.7
900°C PDA 700C FGA	0.03	0.27	44
900°C PDA 800C FGA	0.16	0.34	48.5

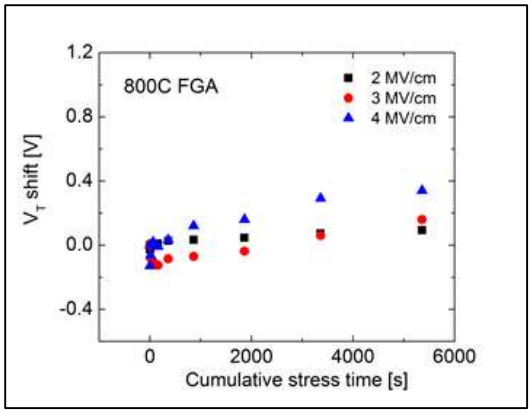


Figure 2. V_T shift vs. different E-field

GaN Device: For GaN device, the main challenge is AC-DC dispersion (or current collapse or gate/drain lag) and normally-on operation (device is on when the gate bias is removed). For this we have proposed a high quality dielectrics for reliable device operation and novel flash approach for enhancement mode GaN power device. In BP1, we have purchased a new AlGaN/GaN on Si wafer from DOWA chemical in Japan and evaluated basic electrical characteristics. Emphasis was placed on high-k passivation to lower the gate leakage and to decrease device on-resistance. We also proposed a tapered structure in order to improve the device retention characteristics by reducing electric field concentration at the drain side of the gate edge. As shown in Figure 3, a tapered field plate structure was fabricated using photoresist reflow process and the dry etching selectivity control. We have fabricated both normal angle as well as tapered angle field plate using photoresist reflow and anisotropic dry etching process. Figure 3 shows field emission secondary electron microscopy (FE-SEM) image of fabricated device with tapered angle. The achieved angle was about 45° but this can be lowered by tuning the process parameters. In order to confirm the effect of electric field reduction by tapered angle, a 2-D device simulation was performed. The simulation results in Figure 4 clearly shows at least 3 times reduction in the electric field at the edge of the gate electrode to drain side with 45° tapered angle as compared to the 90° angle structure.

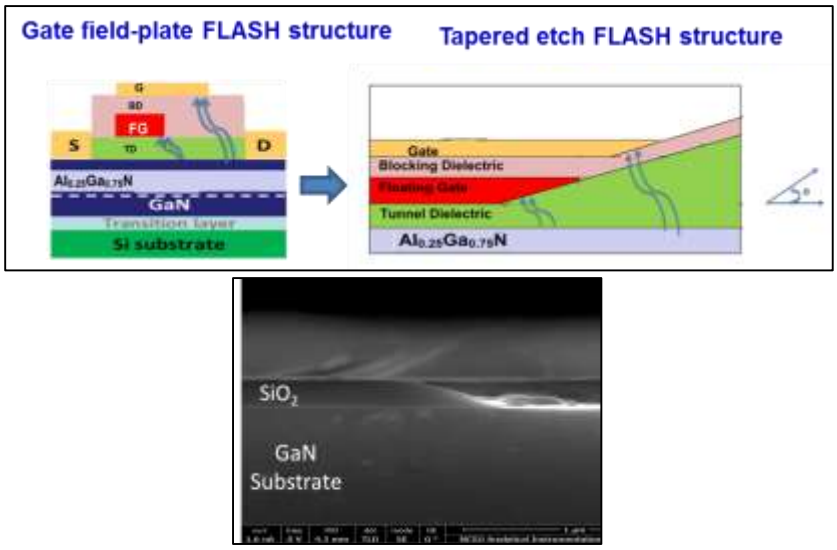


Figure 3. Schematic illustration of proposed Tapered field plate FLASH MOSHFET and FE-SEM image of device with tapered angle.

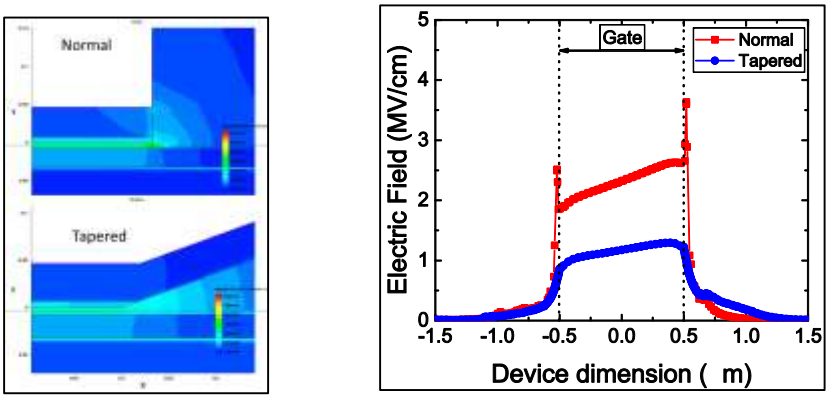


Figure 4. TCAD 2D simulation results. (a) Electric field contour plot for normal angle vs. tapered angle and (b) extracted electric field at the gate edge to the drain side with V_D=400V.

Technology to Market: Our project embodies a disruptive device technology that provides excellent system level performance (high energy efficiency) at a cost lower than current WBG technologies. Therefore the technology has great market potential and can drastically change the WBG market landscape in the next five years. We have proposed to develop unit process module for deposited oxide using ALD that are able to achieve better performance than grown SiO_2 layer. For this, we will use foundry's existing process flow and substitute different ALD gate oxide layers in BP2 to see the feasibility of high volume manufacturing. In terms of intellectual property management, the Office of Technology Transfer (OTT) at North Caroline State University (NCSU) is responsible for management and commercialization of intellectual property assets developed by this project in NCSU.

Plans for next budget period If Funded: For BP2, we continue to develop a highly manufacturing compatible device technology that can enhance the SiC inversion channel mobility at least 4 times higher than the current commercial SiC MOSFET via interface

engineering using rare-earth metal oxides with atomic layer deposited SiO_2 bulk dielectric while maintain the device threshold voltage is more than 2V. The main focus of proposed work for SiC will be 1) to control the interface layer by using ultrathin rare-earth metal oxide layer such that the VT shift is less than 0.5V at elevated temperatures while maintain the mobility is >75 cm^2/V-s, 2) to develop and optimize atomic layer deposited SiO_2 process to serve as main gate dielectrics to implement to the high volume foundry process, and 3) to evaluate the reliability (TDDB and SILC) and instability for proposed gate stacks in SiC MOSFETs at elevated temperatures. Normally-off GaN device can be realized without performance degradation by using ALD method and device engineering. The main focus of proposed work for GaN will be 1) optimize tapered angle FLASH device with minimum threshold voltage shift and 2) to evaluate reliability and stability of ALD dielectrics at elevated temperatures. The successful achievement of this projects will significantly benefit the performance of SiC and GaN power switching devices and hence the market transformation.

Project Output:

X. Yang, B. Lee, and V. Misra, "Investigation of lanthanum silicate conditions on 4H-SiC MOSFET characteristics", IEEE Transactions on Electron Devices, vo. 62 (11), pp. 3781-3785, 2015.

X. Yang, B. Lee, and V. Misra, "High mobility 4H-SiC lateral MOSFETs using lanthanum silicate and atomic layer deposited SiO_2", IEEE Electron Device Letters, vol. 36, no. 4, pp. 312-314, 2015.

Milestone Summary

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
2.8.1.1	Robust ALD dielectric with breakdown electric field in excess of 8MV/cm	Month 3	Complete
2.8.1.2	Lateral SiC MOSFET with ALD dielectric with inversion channel mobility of 25cm2/V-s	Month 6	Complete
Decision Point	Reliability of ALD gate stacks on lateral channel MOSFETs with threshold voltage shift of less than ± 0.5V under constant DC bias (± 4MV/cm)	Month 9	Complete
2.8.1.3	Lateral SiC MOSFET with inversion channel mobility >50cm2/V-s on 5E16cm-3 doped p-epi.	Month 12	Complete (with p-doping of 5E15cm-3, high doped wafer has been ordered)

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
2.8.4.1	E-mode with VT of 1V and breakdown of 600V with ALD dielectrics	Month 3	600V of breakdown was achieved, E-mode fabricate was delayed due to the delay of wafer delivery
2.8.4.2	600V breakdown and specific on resistance value of 3mohm-cm2 with ALD dielectrics	Month 6	Complete
Decision Point	E-mode with threshold voltage of 2V and gate shift is less than 1V under DC stressing	Month 9	Incomplete (NNF cleanroom delay)
2.8.4.3	E-mode with threshold voltage > 3V, maximum gate voltage of 10V, and gate shift of <0.5V	Month 12	Incomplete (NNF cleanroom delay)

Dr. Mehmet C Ozturk

Organization: NC State University
Task No./Project Title: Task 2.9 / Device and Process Flow Development for WBG Training and Foundry Operations
Technical Point of Contact: Mehmet C. Ozturk
Start date for internal NC State project: 02/01/2015

Project Objectives: The objective of this task is to develop a university WBG power device and process flow to:

- Train students in WBG semiconductor processing for power electronics, and provide the education and workforce development platform to support future WBG foundry operations and WBG process development, as well as the knowledge base for workers and students to fabricate, characterize and test devices.
- Encourage academics and small companies to innovate, test, and fabricate device ideas at low cost before transferring to domestic manufacturing foundry production through well-defined process steps.
- Address specific problems of interest through R&D projects to accelerate WBG device manufacturing.

Project's Contribution to the Power America Mission: The main contribution of the project to the Power America mission is education and workforce development. The first year of the project was dedicated to acquisition of the i-line stepper and establishing the tool as a resource for Power America research and education efforts through developing lithography processes. If the funding for this program is continued, we will be following a multi-pronged approach to teach wide bandgap device manufacturing in hands-on undergraduate and graduate level device fabrication courses. We will also establish annual workshops on WBG device theory and fabrication participants from industry and other institutions.

Technical Approach: The main focus of this year was acquisition and installation of an i-line stepper in the NCSU Nanofabrication Facility. Because it would not be possible to acquire a new instrument with the available funding, we have decided to purchase a refurbished stepper. A GCA Autostep I-Line Stepper was identified as the best tool that would meet the specifications and acquired.

Through discussions with Power America researchers, we decided to establish a simple GaN process flow to teach transistor fabrication in the laboratory. The process flow is a simplified version of the flow used by Veena Misra's group in her research. The main difference is that our process uses a basic Schottky gate architecture. The process flow also provides us the opportunity to demonstrate several fabrication processes for patterning, deposition and etching. Our goal is to teach this flow in a hands-on graduate level fabrication course relying on the NCSU Nanofabrication Facility as a teaching laboratory. Graduate and undergraduate course modules will be developed for other institutions interested in adopting our approach in their programs. The module will include the mask design, detailed process specifications and a lab manual.

We also plan to create an annual workshop to teach WBG device theory and fabrication. The participants may be engineers from the WBG industry or students from other institutions, which do not have similar fabrication capabilities.

Issues, Risks and Mitigations: None

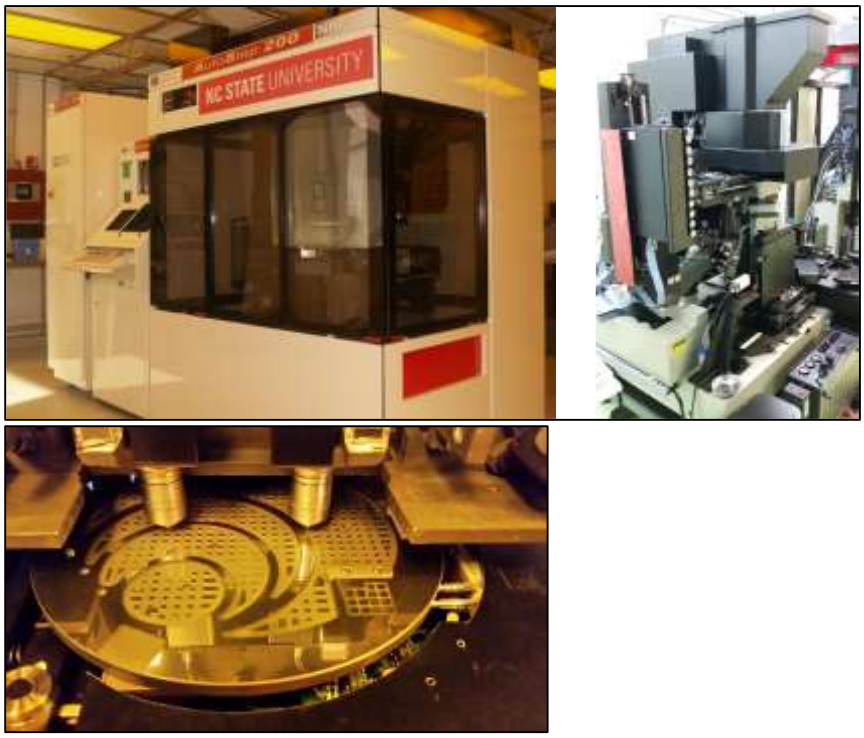


Figure 1. GCA Autostep I-Line Stepper and the multi-purpose wafer chuck

Significant Accomplishments: A GCA Autostep I-Line Stepper was located at Stepper Care Services (SCS) the leading company servicing the GCA steppers and a reputable equipment reseller. The tool was completely refurbished by SCS and included a 1-year warranty. A key advantage of this particular tool was that it came with a brand new lens, which was kept at Sandia Research Labs as a spare lens. We have also ordered two chucks that would allow us to accommodate sample sizes ranging from small chips to full 8" wafers. Another requirement was to accommodate wafers of different thicknesses since the users could be using SiC, GaN and Si wafers of different thicknesses. A special wafer chuck to accommodate small chips as well as wafer diameters ranging from 2 to 8 inch was designed and manufactured.

The tool was successfully installed in the NCSU Nanofabrication Facility and a series of experiments were carried to verify the tool specifications. The key requirement in our SOPO was demonstration of 0.6 micron resolution with a wafer bow. The tool's capability is demonstrated in Figure 2, which includes four optical microscope images taken from the four corners of a Si wafer with a wafer bow of 65 microns. The wafer bow was measured by a Veeco Dektak profilometer with stitching capability in our facility and verified by a Tencor Flexus 2320 Thin-Film Stress Measurement Computer at Research Triangle Institute . It can be seen that the tool was able to define 0.5 micron lines at the four wafer corners despite the significant bow the wafer has.

Another key tool specification was the ability to write on wafers with different thicknesses. To verify this capability, experiments were carried on wafers whose thicknesses varied from 370 to 550 microns. Shown in Figure 3 is the result of such an attempt on 370 micron thick GaN wafers. The two images were taken using an optical microscope and a scanning electron microscope. The photoresist used was 1.3 micron thick Shipley 1813 and the sample size was 10 mm x 10 mm. It can be seen that a minimum resolution 0f 0.5 micron is achieved on the sample. This minimum resolution was achieved on all samples tried up to a thickness of 550 microns. Another chuck capable of reaching 250 micron thickness – to further expand the thickness - is also on order.

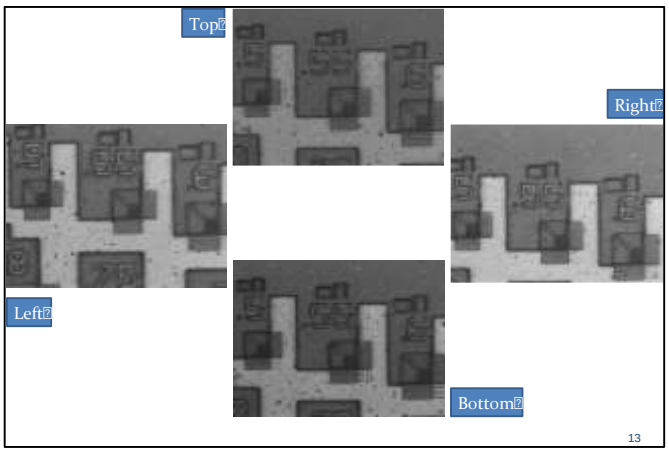


Figure 2. Resolution at four corners with a wafer bow of 65 microns

Shown in Figure 4 is the resolution at the corners of a single flash. Again, the images demonstrate the same minimum resolution indicative of no tipping of the lens.

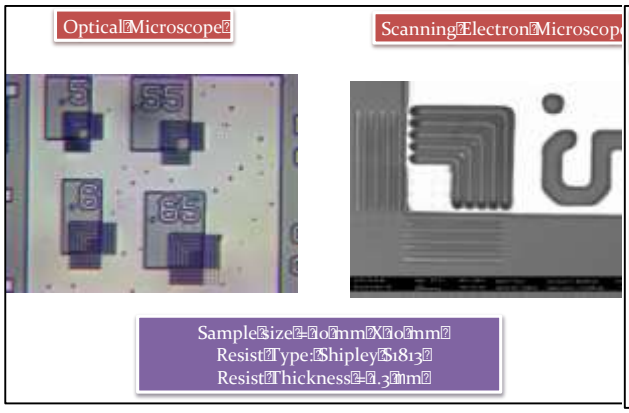


Figure 3. Experiment to verify 0.5 micron minimum resolution on a GaN wafer with thickness of 370 microns

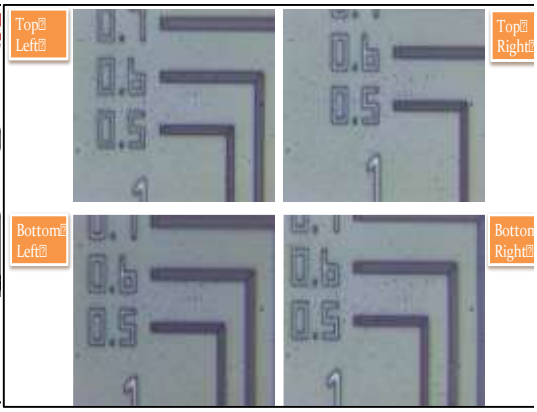


Figure 4. Resolution at four corners of a flash – excellent resolution at all four corners indicate no tip of the lens.

Figure 5 demonstrates the minimum resolution of the tool applied to copper lift-off. The resist used for this sample was AZ nLOF 5510 negative lift off photo resist. The sample was developed in AZ 300 MIF developer. The metal stack consisted on 100 nm Cr, followed by 500 nm Cu, both deposited by evaporation. Lift off was achieved in NMP (1-Methyl-2-pyrolidinone).

Typical teaching laboratories on device fabrication target Si MOSFETs. Naturally, these courses focus on standard processes used in silicon integrated circuit fabrication. While many of these processes (e.g. lithography, plasma etching, metallization) are common to fabrication of all semiconductor devices, it is not truly possible to educate the students on specific manufacturing challenges encountered in fabrication of power devices on WBG semiconductors. This is due to the fact that every semiconductor material brings its own challenges requiring processes and process conditions to be tailored according to its needs.

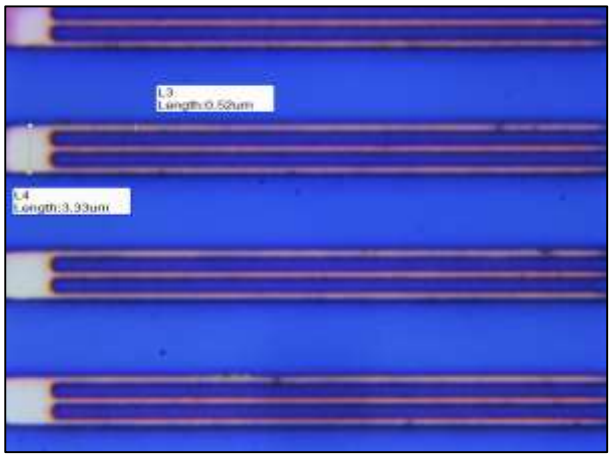


Figure 5. Copper lines defined by lift-off on silicon demonstrating 0.5 micron minimum resolution.

In this effort, our goal is to create teaching modules targeting transistor fabrication using a process flow as close as possible to those used in manufacturing of commercial devices. We chose GaN as our material simply because the equipment used in manufacturing of GaN devices do not include high-temperature oxidation and diffusion furnaces that their SiC counterparts require, which are not common in university teaching laboratories. In addition, the NCSU Nanofabrication Facility is already providing services to graduate students working on GaN transistors for their dissertations. The intent is to include the GaN transistor fabrication module in an existing course (ECE 739 – Integrated Circuits Technology and Fabrication Laboratory) offered in the Department of Electrical and Computer Engineering at NC State University.

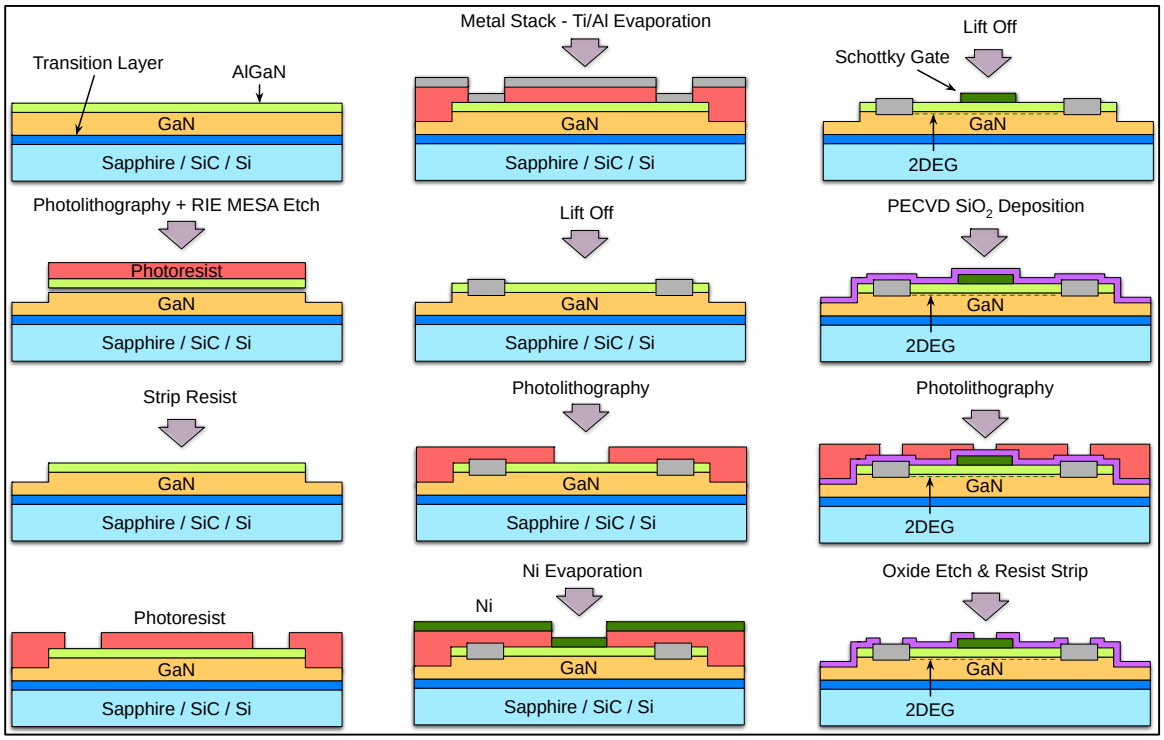


Figure 5. Process flow for GaN transistor fabrication

Through discussions with Power America researchers, we have decided to adopt a process flow inspired by the ongoing work in Dr. Misra's group. The process flow is illustrated in Figure 6. The mask set for these devices has already been designed and ordered. The students registered in this class will go through the entire process flow learning along the

way the fundamentals of key processes used and the unique challenges introduced by the specific semiconductor material.

Technology to Market: Since this project is mainly focusing on education, there is no new technology developed for the market. However, a teaching module on GaN transistor fabrication is planned for dissemination.

Plans for Next Budget Period If Funded: If the project is funded, the project will have four major tasks:

1. The GaN transistor fabrication module will be incorporated in an existing course (ECE 739 – Integrated Circuits Technology and Fabrication Laboratory) offered in the Department of Electrical and Computer Engineering at NC State University. In the current implementation of this course, advanced graduate students are exposed to theory and practice of standard manufacturing processes used in fabrication of silicon integrated circuits. The course is structured such that the students attend two 75 minute lectures every week and spend 3 hours in the NCSU Nanofabrication Facility learning about fabrication tools and processes. Working in groups of 5 – 6 students, they fabricate devices and perform wafer level probing for electrical characterization and parameter extraction. In this project, the course contents will be modified to educate the students on the aspects of (WBG) device fabrication leading to fabrication and characterization of transistors.
2. An undergraduate module will be created based on the graduate module but will include a theory section providing an introduction and overview of power device concepts at an introductory level. The module will include a series of power point slides and video lectures that will be available for dissemination to other institutions. The main objective is to facilitate incorporation of WBG device fundamentals and fabrication in existing undergraduate courses at NCSU and other institutions. Undergraduate courses that do not have a hands-on component will especially benefit from this module. To keep the video lectures engaging, we will supplement them with demonstrations captured in the clean-room and it will include animations describing different processes. The video lectures will go through transistor fabrication and cover the material at an introductory level.
3. An annual workshop will be created and publicized through the Power America web site. The objective is to create a nationally advertised go-to workshop for new engineers joining the WBG work force that do not have the background on power semiconductor device theory and fabrication. Workshop participants will be charged a registration fee to cover the participant costs including hotel, meals and supplies. The workshop module will be based on the materials created for the courses but it will be tailored for professionals. Essentially, its level will be higher than that of the undergraduate module and it will attempt to provide a broader view of devices manufactured in industry and an overview of state-of-the-art devices researched in academic laboratories. The workshop participants will spend the first day in a classroom learning about device theory and fabrication. The PI will serve as the workshop coordinator and the primary instructor. He will recruit other NCSU PIs (e.g. Misra and Baliga) as well as industry participants supported by Power America for guest lectures throughout the workshop. The remaining two days will be spent in the

NCSU Nanofabrication Facility focusing on hands-on demonstrations and device characterization. The facility staff will provide the instructions and help with the hands-on demonstrations.

4. Funding is requested to acquire a refurbished etcher for dedicated GaN etching. The existing etcher in the NCSU Nanofabrication Facility is severely outdated and it no longer provides reliable operation. It also has some key shortcomings such as lack of substrate cooling and an outdated computer system. In Fall 2015, a series of equipment problems have forced the tool to be out-of-service for an extended period of time (close to two months). The age of the tool is an issue making it more and more challenging to maintain it. As such, we believe it is critical for both the education effort and GaN fabrication research, we need to acquire a reliable etch tool designed to support chlorinated plasma chemistries (e.g. BCl_3) used for GaN etching. Due to the corrosive nature of these gases, such a tool must have a load-lock for wafer loading. An inductively coupled plasma etcher is also desirable for throughput. Realizing the scarcity of the funds for such an investment under the Power America program, the PI will explore the possibility of acquiring a refurbished system better suited to our needs for under $150K. New tools with ICP capability and load-lock typically cost over $500K.

Project Output: None yet

Milestone Summary

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
2.9.1.1	I-line Stepper (0.6 microns resolution with wafer bow up to 40 microns, wafer held in place by vacuum chuck, column capable of moving +/- 100 microns) specified and ordered.	Month 3	Complete
2.9.1.2	Site work for purchased equipment in 2.9.1.1 completed.	Month 6	Complete
2.9.1.3	Installation of purchased equipment in 2.9.1.1 completed.	Month 9	Complete
2.9.1.4	Equipment Purchase Evaluation Plan ((1) Plasma Enhanced CVD for Oxide, (2) Metal Sputtering System, (3) High Temperature Annealing Furnace, (4) High Temperature Oxidation Furnace, (5) Atomic Layer Deposition System, (6) Reactive Ion Etching System) for BP2 submitted for DOE review. (Month 9)	Month 9	Complete
2.9.1.5	Unit processes to support R&D and manufacturing projects in place with	Month 12	Complete

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
	line width control through SEM and TEM imaging.		
G/No-Go Decision Point	I-line Stepper installed and operational to vendor's specifications (0.6 microns resolution with wafer bow up to 40 microns, wafer held in place by vacuum chuck, column capable of moving +/- 100 microns).	Month 12	Almost Complete – A second wafer chuck has been ordered to increase the range of wafer thicknesses the stepper will be able to accommodate.

Organization: National Renewable Energy Laboratory
Task No./Project Title: Task 4.1: Manufacturing and Commercialization of WBG Inverter for Off-Highway and On-Highway Heavy-Duty Vehicles (Support for Design and Development of Hardware Parts for Generation 1 SiC Inverter)
Technical Point of Contact: Kevin Bennion
Sub-award start date: 02/01/2015 (Interagency agreement with DOE)

Project Objectives: This task shall design, produce, test, deploy and commercialize a 200kW 1000Vdc wide-bandgap (WBG) dual inverter (two inverters connected back-to-back on a common DC bus) for heavy-duty off-highway and on-highway electric and hybrid vehicles. The budget period 1 objective is to fabricate key hardware parts for a 200kW 1000Vdc SiC Dual Inverter and start testing these parts. The National Renewable Energy Laboratory (NREL) is supporting and assisting the John Deere Electronics Solutions (JDES) project team in Task 4.1 through analysis of the thermal management system with thermomechanical considerations during the development of the dual inverter. NREL, in collaboration with JDES, is supporting the development of thermal management solutions using appropriate thermal interface materials and cooling technologies to enable JDES to complete the design, fabrication, and test verification of mechanical and electrical parts (hardware parts) of the bench-top inverter.

Project's Contribution to the PowerAmerica Mission: The contribution of the project to PowerAmerica focuses on a few areas related to the PowerAmerica's mission. Working with JDES the project emphasizes the production and demonstration of WBG applications that are intended for commercialization. In addition the work provides the opportunity for education and workforce development as engineers work to integrated WBG materials into commercial applications.

Technical Approach: The technical approach for NREL's supporting effort is outlined within the statement of project objectives (SOPO). The four subtasks for the JDES led project are outlined below, and a summary of NREL's support for each subtask is included.

- Subtask 4.1.1: Design of mechanical, electronic and electrical parts for bench-top inverter
    - NREL Subtask Summary:
        - Provide design support including modeling and analysis of thermal management systems for the inverter operating in accordance with specifications provided by JDES.
- Subtask 4.1.2: Fabrication of prototype parts for the inverter assembly
    - NREL Subtask Summary
        - Provide simulations of selected designs to support selection of cooling strategy that delivers necessary heat dissipation, keeps temperatures within limits, and helps meet inverter-level targets.
- Subtask 4.1.3: Functional testing of prototype parts of the inverter assembly
    - NREL Subtask Summary
        - Quantify thermal performance of thermal management approach for prototype parts by comparing cooling performance and pumping power for single-phase liquid cooling using water-ethylene glycol (WEG) over a range of flow rates and coolant temperatures as specified by JDES.
- Subtask 4.1.4 Prototype assembly of bench-top inverter

- NREL Subtask Summary
  - Support thermal simulation and reliability analysis in collaboration with JDES through thermomechanical simulations (finite element analysis solving for temperature and stress/strain simultaneously) to predict potential areas of high stress and reliability concerns.

Issues, Risks and Mitigations: As a supporting partner to JDES, work at NREL is performed in close collaboration with JDES. Progress is reviewed regularly with JDES during project review meetings in which issues or concerns are captured as action items with priority levels. Capturing critical action items supports communication between NREL and JDES to identify and mitigate issues in the thermal design efforts.

Significant Accomplishments: During budget period 1 heat load estimates were calculated and thermal performance metrics were established. A thermal design was identified that could meet the thermal performance targets identified by JDES using the selected prototype fabrication hardware as illustrated in Figure 1. The solid blue curve represents the total package junction to coolant ($R_{th,ja}$) thermal resistance of the module package and cooling technology as a function of the heat exchanger thermal resistance of the active cooling technology. The green box highlights the target total package thermal resistance ($R_{th,ja}$) specified by JDES, which provides targets for the heat exchanger thermal resistance. The red markers represent two potential thermal management designs that meet the thermal performance targets at a flow rate of 10 L/min.

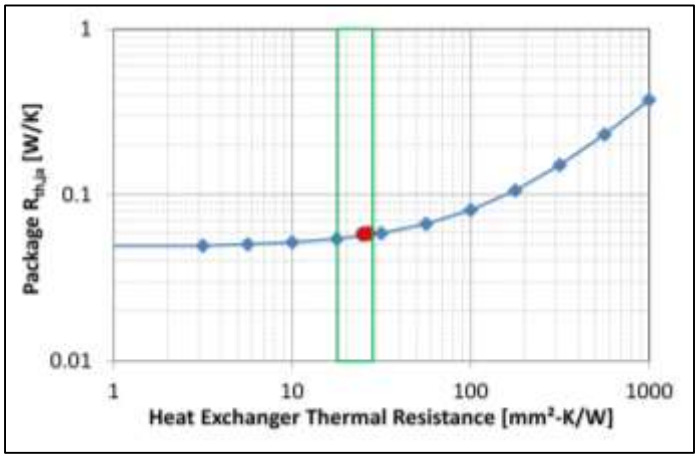


Figure 5: Total package thermal resistance versus heat exchanger resistance for the selected power module package (blue curve), thermal performance target region (green box), and prototype design performance estimates at 10 L/min total system flow rate (red markers).

In consultation with JDES, NREL performed thermal design studies of thermal performance, pumping power, and flow rates. Two key parameters were studied to identify designs that could enable increased fluid flow rates with comparable pumping power requirements. Figure 2 illustrates two of the design variables that were studied. The left figure in Figure 2 demonstrates the impact of offsetting the manifold structure of the design from the bottom of the power module. As seen in the figure, an offset of approximately 75 µm enables slightly improved convective cooling with a higher system flow rate at the same parasitic fluid pumping power. The right figure of Figure 2

illustrates the impact of increasing the number of micro-manifolds that are used to distribute coolant to the cooling structures on the bottom of the power module. As shown in the figure, increasing the number of micro-manifolds allows for higher convection coefficients with increased fluid flow at the same parasitic fluid pumping power. As the number of micro-manifolds increase, the improvement in the convection coefficient reduces, and the number of micro-manifolds is also constrained by the available footprint dimensions of the power module.

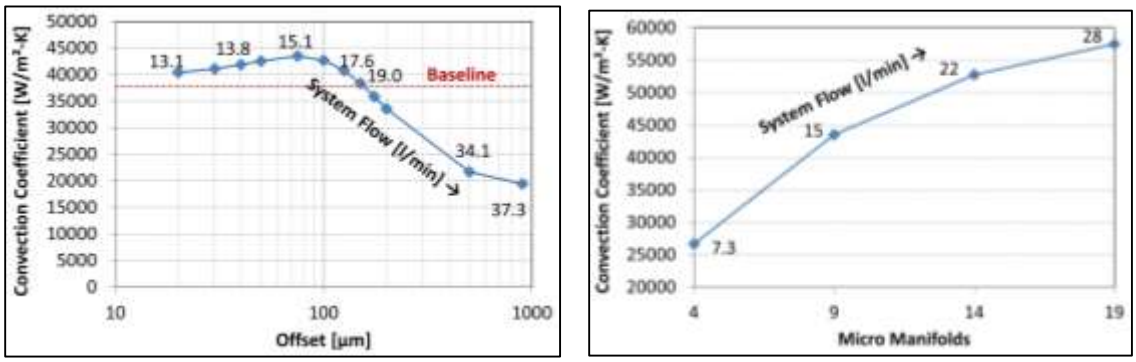


Figure 6: Impact of micro-manifold to power module base offset on convection coefficient at fixed fluid pumping power, enabling increased system flow rates (left). Impact of the number of micro-manifolds on the convection coefficient at fixed fluid pumping power, enabling increased system flow rates (right).

The convection coefficient performance estimates from channel flow computational fluid dynamics (CFD) simulations were applied to a thermal finite element analysis (FEA) model to estimate the temperature gradients through the power module (Figure 3, Left). In an effort to confirm the analysis results a full conjugate heat transfer and fluid dynamics model was generated for the full module and micro-channel heat exchanger consisting of over 130 million elements and run using NREL's computational resources. The preliminary results shown in the right image of Figure 3 show that the full module conjugate heat transfer results are similar to the earlier performance estimates.

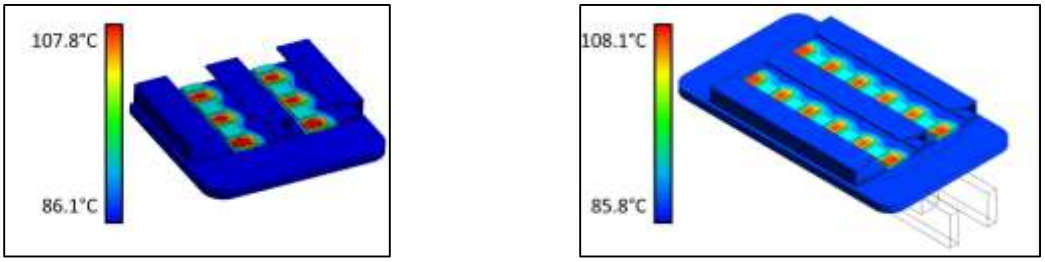


Figure 7: Comparison of module thermal FEA with convection heat transfer boundary condition (left) and full module and micro-channel CFD conjugate heat transfer solution (right).

Technology to Market: The work performed by NREL is in direct collaboration with JDES, and JDES is focused on manufacturing and development of a vehicle application.

Plans for Next Budget Period If Funded: The primary objective for the JDES led project during budget period 2 is to manufacture and test the high efficiency SiC dual

inverter in the JD644 K Hybrid Loader. NREL's efforts in support of JDES will focus on the follow key items:

- Optimize thermal analysis based on JDES lab data for module and support of module thermomechanical modeling for stress computation
- Verify CFD analysis of inverter and its interconnects with lab data
- Perform CFD analysis for inverter interconnects improvements & film capacitor package
- Submit summary report of inverter thermal management and thermomechanical results to JDES

Project Output: No papers related to this work have been published by NREL. All publications would be submitted with JDES.

Milestone Summary

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
4.1.1	Complete specification and design of TIM and thermal management system for power interconnects, as well as failure mode and reliability analysis.	Month 3	Complete: CAD provided by Partner. Brought into thermal simulation software. Calcs made for heat loss of devices. Materials and specs defined. Design plans for interconnects and cooling were discussed. Modeling approach determined to evaluate system cooling.
4.1.2	Deliver interconnect thermal map with potential thermal interface material solutions to improve thermal management to support prototype parts fabrication for the bench-top inverter.	Month 6	Complete: Supported JDES inverter development. In consultation with JDES, NREL performed thermal design studies to support JDES in selecting fabrication methods for prototype parts. NREL also performed thermal simulations to quantify the impact of thermal management options on temperature map of module components.
4.1.3	Deliver thermal performance (resistance) and pumping power metrics for candidate cold plate that meet the thermal requirements.	Month 9	Complete: Supported JDES inverter development. In consultation with JDES, NREL performed thermal design studies of thermal performance, pumping power, and flow rates.

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
4.1.4	Deliver results obtained from thermomechanical simulations and testing for various components.	Month 14	2 month extension
Go/No-Go	Provide thermal management solutions using appropriate thermal interface materials and cooling technologies to enable performing company to complete the design, fabrication and test verification of mechanical, electronic and electrical parts (hardware parts) of the bench-top inverter with desired mechanical and electrical specifications.	Month 14	2 month extension

Organization: Naval Research Laboratory
Task No./Project Title: 2.10 Study of Defects in SiC Epitaxy through Ultraviolet Photoluninescense
Technical Point of Contact: Robert Stahlbush
Sub-award start date: 02/01/2015 (Interagency agreement with DOE)

Project Objectives: NRL's objective is to collaborate with other Power America members that manufacture SiC power devices and to assist these manufacturers in minimizing the materials extended defects that degrade the yield, performance and reliability of their power devices. The materials extended defects include basal plane dislocations (BPDs), in-grown stacking faults and inclusions. These defects can be present in the wafers as grown or can be introduced during the processing. NRL will provide whole-wafer, nondestructive imaging that will screen and identify materials defects present in the incoming wafers as well as identifying fabrication steps that are introducing materials defects.

Project's Contribution to the PowerAmerica Mission: Agreements are in place with United SiC and GeneSiC Semiconductor to screen and to identify extended defects such as BPDs present in the incoming wafers as well as to provide them with feedback about extended defects introduced by their fabrication steps. This feedback shortens the process of adjusting the fabrication parameters to minimize the introduction of new extended defects.

NRL has also contributed to Power America's mission by hiring two graduate students over this past summer and training them to use the Ultraviolet Photoluminescence (UVPL) technique to identify and quantify extended defects in SiC epitaxial layers.

Technical Approach: The primary technique employed for observing and quantifying material defects is Ultraviolet Photoluminescence (UVPL) imaging. UVPL is a noncontact, non-destructive technique that can image extended defects in the SiC epitaxial layers, which are critical for device operation. These defects can be imaged in samples ranging from full 150 mm wafers to individual dies. UVPL imaging also tracks the path of BPDs through the whole epitaxial thickness. UVPL assists device manufacturers in producing reliable, high performance devices in multiple ways. It can screen incoming wafers and identify quality differences between wafer suppliers as well as differences between batches of wafers from the same vendor. UVPL is not limited to imaging incoming wafers. It can also image extended defects before and after any processing step as long as metal layers are not present. This makes it possible to evaluate individual processing steps to see if new extended defects are created. For example, NRL has shown that the combination of implantation and high temperature annealing can introduce BPDs into devices. With UVPL imaging, it is also possible to examine individual die after electrical testing to determine if BPDs or other extended defects are responsible for dies that fail electrical testing.

NRL has also developed automated analysis of UVPL images to provide BPD counting and characterization. An example of BPD wafer mapping done by NRL for wafer screening wafers is shown in Fig. 1. The SiC wafer is 150 mm in diameter with a 35 um epitaxial layer. The results are derived from an automated analysis of an UVPL image, and graphically displays information about BPDs present in the epitaxial layer before any device fabrication steps. The figure includes two wafer maps and two whole-wafer histograms. The top wafer map shows the distribution of BPDs by dividing the wafer into 2x2 mm areas and counting the number of BPDs in each of these areas. The false color wafer map bins the number of BPDs. For example, green is for 2x2 mm areas

with no BPDs, yellow areas have 1 BPD and blue areas have 2-3 BPDs. The histogram to its right shows the distribution of BPDs per area over the whole wafer. In many cases the BPDs in the epitaxial layer originate in substrate and convert into threading edge dislocations (TEDs) during the epitaxial growth. The bottom wafer map and histogram show the distribution of epitaxial thicknesses at which the BPDs convert into TEDs.

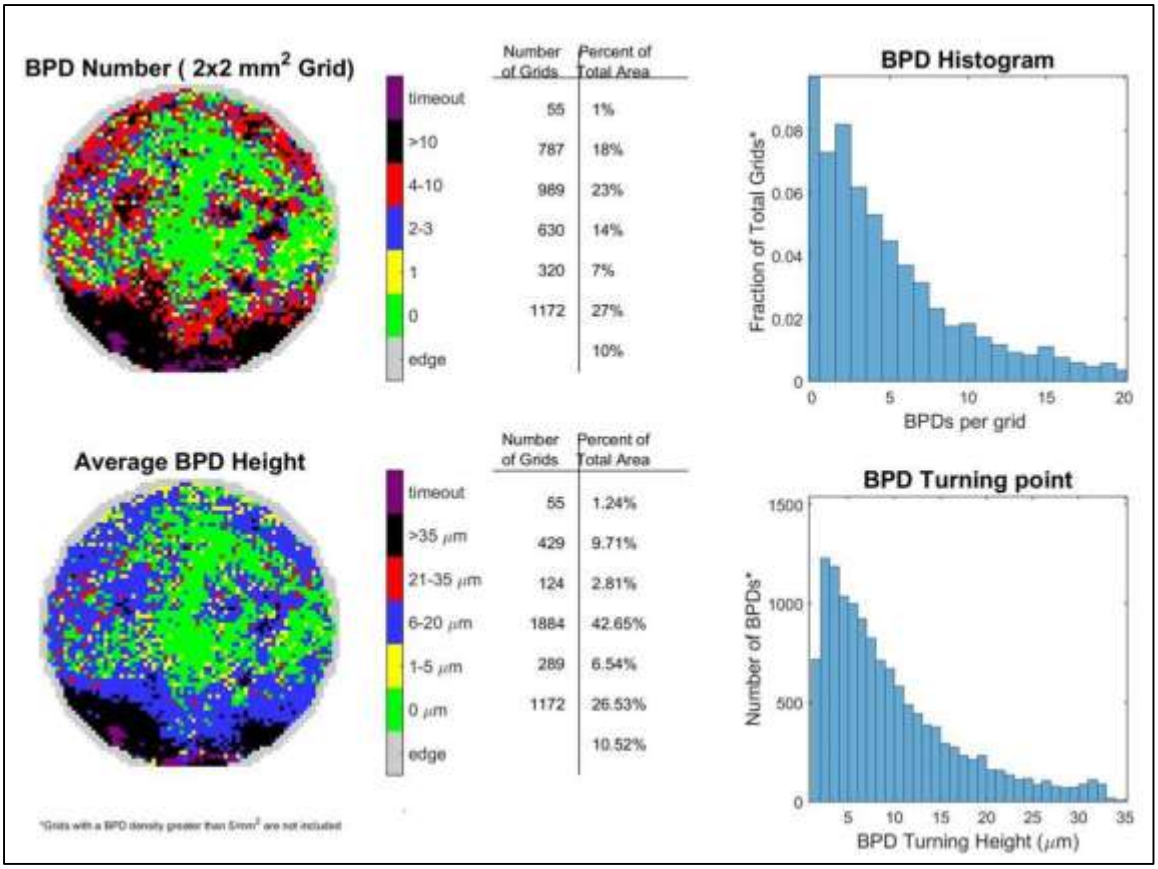


Fig. 1. Wafer maps showing the distribution and properties of BPDs derived by automated analysis of an UVPL image of an incoming wafer.

Issues, Risks and Mitigations: The adverse effects of materials extended defects, such as BPDs, on the performance and reliability of SiC power devices has been a continuing issue for many years. Significant progress has been made in reducing these defects in SiC substrates and epitaxial layers over the last decade, which has opened the path for commercially viable SiC devices. For this market to continue to expand, better and more cost-effective monitoring and identification of extended defects need to be incorporated into the manufacturing of SiC power devices.

UVPL imaging provides mitigation for the extended defects issue by providing non-destructive, direct observation of these defects. It provides quick and cost-effective method for screening wafers before fabrication and for discovering extended defects introduced by processing steps. Observing BPDs or other extended defects either before or partially through the fabrication process directly identifies the source of the defects and significantly speeds up the process of minimizing these defects to acceptable levels.

Significant Accomplishments: Agreements have been established for collaborating with Power America manufacturing members USCi and GeneSiC to assist them in identifying the source of evaluating extended materials defects. The first step is screening of incoming wafers to identify the number and types of defects . Six wafers have been screened for USCi and two for GeneSiC. Plans are in place to re-image the wafers after various fabrication steps. For both companies, NRL has also examined die after electrical testing to determine the role, if any, that extended defects played in degradation observed by electrical testing.

Technology to Market: The collaborations with other Power America members that are manufacturing SiC power devices will provide them with faster and more cost effective methods to control the BPDs and other extended defects that reduce the yield, performance and reliability of their SiC power devices.

Plans for Next Budget Period If Funded: NRL's next budget period does not begin until June 2016. The plans for this next period involve continuing the collaboration with USCi and GeneSiC Semiconductor described below and starting new collaborations, which will be similar, with other Power America members.

Project Output: The first few months of NRL's time as a member of Power America has been spent establishing collaborations with USCi and GeneSiC Semiconductor. These collaborations involve both screening wafers for BPDs and other extended defects before fabrication and after various fabrication steps to determine if any new extended defects are introduced by the processing. The screening of initial wafers has been done for both companies and these wafers will be reevaluated after the agreed upon fabrications steps.

Milestone Summary

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
2.10.1.1	Image BPDs pre- and post-fab	Q1	complete
2.10.1.2	Image BPDs pre- and post-fab, 2nd round of devices	Q2	Incomplete, 2nd round of devices not yet made by collaborating partners
2.10.2.1	EL imaging of reverse-biased leakage	Q1	Incomplete, collaborating partners preferred UVPL screening
2.10.2.2	EL imaging of reverse-biased leakage	Q2	Incomplete, collaborating partners preferred UVPL screening
2.10.3.1	Pre-fab BPD maps	Q1	complete
2.10.3.2	Pre-fab BPD maps	Q2	complete

TOSHIBA
Leading Innovation

Organization: Toshiba International Corporation
Task No./Project Title: Task No. 4.3
Technical Point of Contact: Peter Liu, peter.liu@toshiba.com
Sub-award start date: 02/01/2015

Project Objectives: There is very strong demand for Small Commercial PV inverters (10 kW to 99 kW) to supply rapid growth markets. Customers (PV integrators) have clear requirements for ultra-light-weight and high-efficiency PV Systems. The ultra-light-weight can significantly reduce the cost of installation, maintenance, logistics and inventory. As a result the system cost is significantly reduced. The high-efficiency plays a critical role to reduce return of investment for PV systems. However, most of existing Small Commercial PV inverters cannot meet the customers' above requirements. Taking the example of existing 50 kW outdoor PV inverters, they weigh more than 300 pounds and have 96% or less CEC efficiency.

Targeting on a high growth market of the small commercial PV inverters, the project objective is to design and manufacture the small commercial PV inverters (10 kW to 99 kW) with SiC devices. The first product being designed is SiC devices based 50 kW PV inverter. The product line of SiC devices based small commercial PV inverters with other power ratings (such as 75 kW, 25 kW, 10 kW) will be designed and released after the 50 kW PV inverter's launching. The advanced battery integration with the PV inverters is also planned in roadmap.

Project's Contribution to the PowerAmerica Mission: The project of the SiC devices based Small Commercial PV inverter contributes to two missions of PowerAmerica. Firstly, the large volumes of SiC devices based PV inverters demanded by the Market dramatically increases the volumes of SiC devices used for the PV inverters, which will scale up the productions of SiC devices. Secondly, the project also contributes to manufacturing-level innovations of reducing manufacturing assembling cost and increasing system reliability for integrating SiC devices into power electronics products.

Technical Approach: The Gen-1 50kW PV inverter is required for 1000 V PV system, 480 VAC grid. Its weight need be less than 143 pounds and its size shall be smaller than 36 in × 36 in × 12 in. Its weighted Efficiency is required to be 98% or greater. Its enclosure rating meets NEMA 4 or IP66. It targets passive cooling if possible. Its operation temperature range shall be from -40 C to 60 C. De-rating is acceptable above 50 C. Customers also demand the easy-to-use, easy-to-transport, easy-to-install and friendly-to-inventory. The new 50kW PV inverter will provide much premium performance than existing products in market.

The requirements of the 1000 V PV system and the 480VAC grid determine the system-level architecture is a two-stage system which includes a DC-DC converter and a DC-AC inverter. It is very hard to achieve 98+% efficiency with Si devices based the two-stage system. The premium performance of SiC devices benefits the PV inverter to meet specification, but the high cost of SiC devices leads to a careful balance between cost and performance. Gen-1 50kW PV inverter deploys 1200V SiC MOSFET in DC/DC converter, which not only increases efficiency, but also reduces size and weight of inductors in DC/DC converter. Multiple-phase interleaving technology applied in DC/DC converter will also reduce the inductor size. Due to unavailability and potential high cost of SiC inverter module, the Si 3-level IGBT module is used in the stage of DC-AC for Gen-1 product, which improves the power quality to utility and provides reasonable efficiency. The SiC devices will be used in DC/AC stage in Gen-2 product.

Issues, Risks and Mitigations: The original plan is to use discrete SiC MOSFET and SiC diode into the Gen-1 50 kW PV inverter. The first prototype based on discrete SiC MOSFET and SiC diode was built and tested, but the thermal performance is poor. The second built prototype is based on discrete MOSFET and SiC diode and metal PCB technology. The metal PCB technology greatly improves thermal dissipation of the discrete SiC MOSFET and SiC diode. However, the mental PCB and complicated mechanical assembling structures associated with it makes it difficult to assemble in plants, which will increase assembling cost and increase scrap rate.

	AE	Power one	Fronius	Fronius	Kaco
	75kW	50kW	60kW	75kW	50kW
Installation	Outdoor	Indoor	Indoor	outdoor	indoor
	Ground mount	Ground mount	Ground mount	Ground mount	Ground mount
Weight	N/A, very hevay	700kg	303kg	732kg	173kg
Eff	95.5%	95.8%	95.5%	96.7%	97.5%
DC	600V	600V	600V	1000V	1000V
DC range	295-595V	330-600V	230-500V	460-950V	250 – 850V
AC	208/480/600V	208/480V	400V	400V	480V
Transformer	60Hz, built in	60Hz, outside	HF	50Hz	No transformer
MPPT	1	1	1	1	3

Table 1: Analysis of competitor products

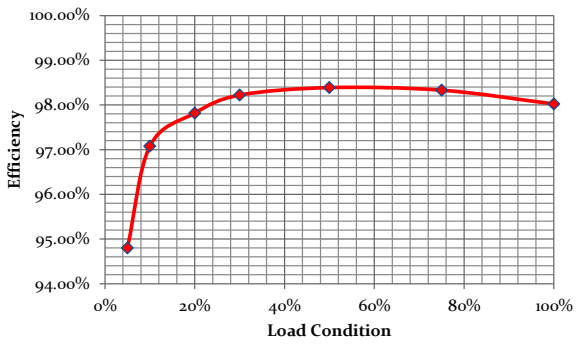


Figure 1: Efficiency of the 50kW PV inverter

Several major vendors of SiC devices claim the module of SiC MOSFET and SiC diode will be released in 2016. Considering poor performance of discrete SiC devices in the 50 kW PV inverter and promising news from vendors about SiC Module, the plan has been adjusted to use modules of SiC MOSFET and diode.

Significant Accomplishments:

Specification of the 50kW PV inverter: the specification has been determined after several rounds discussion with customers. The analyses of existing competitor products have been conducted as shown in Table 1 at the beginning of the project. The Gen-1 50kW PV inverter is required for 1000 V PV system, 480 VAC grid. Its weight need be less than 143 pounds and its size shall be smaller than 36 in × 36 in × 12 in. Its weighted Efficiency is required to be 98% or greater. Its enclosure rating meets NEMA 4 or IP66. It targets passive cooling if possible. Its operation temperature range shall be from -40 C to 60 C. De-rating is acceptable above 50 C. Customers also demand the easy-to-use, easy-to-transport, easy-to-install and friendly-to-inventory. The new 50kW PV inverter will provide much premium performance than existing products in market.

System-level architecture: the requirements of the 1000 V PV system and the 480VAC grid determine the system-level architecture is a two-stage system which includes a DC-DC converter and a DC-AC inverter. It is very hard to achieve 98+% efficiency with Si devices based the two-stage system. The premium performance of SiC devices benefits the PV inverter to meet specification, but the high cost of SiC devices leads to a careful balance between cost and performance. Gen-1 50kW PV inverter deploys 1200V SiC MOSFET in DC/DC converter, which not only increases efficiency, but also reduces size and weight of inductors in DC/DC converter. Due to unavailability and potential high cost of SiC inverter module, the Si 3-level IGBT module is used in the stage of DC-AC. The calculation and simulation shows that peak efficiency of the 50kW PV inverter is 98.39% at 50% of load and the weighted efficiency (CEC efficiency) is 98.24%, as shown in Figure 1. Figure 2 shows a pie chart of power losses distribution.

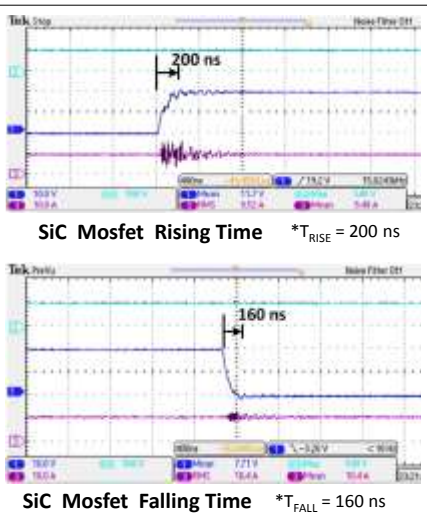


Figure 3: SiC MOSFET turn on/off

Experiment prototypes of DC/DC converters: two prototypes of SiC MOSFET based DC-DC converter have been built and tested. The SiC devices in these two prototypes are Cree SiC MOSFET C2M0080120D and Cree SiC Diode C4D10120D. Both are discrete devices package as TO-247-3. In the first prototype, SiC MOSFET and diode are mounted on the heat sinks. Testing results for the first prototype demonstrated acceptable performance of switching frequencies and turn-on and turn-off characteristics as shown in Figure 3 and Figure 4, but it also showed unsatisfied thermal performance. With 25C ambient temperature, the case temperature can be as high as 95C under full load. In order to improve the thermal performance, the metal core technology has been applied in the second prototype. The SiC devices are soldered on the metal core PCBs. Then these PCBs will be mounted on heat sink. The metal core PCBs provide large area of heat dissipation. The case temperatures of SiC devices have been reduced significantly in the second prototype based on ongoing experiments. The second prototype also showed the difficulty of assembling metal PCBs, which could significant increase assembling cost and scrape rate.

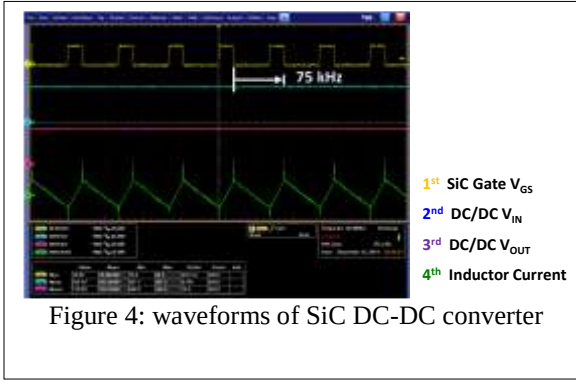


Figure 4: waveforms of SiC DC-DC converter

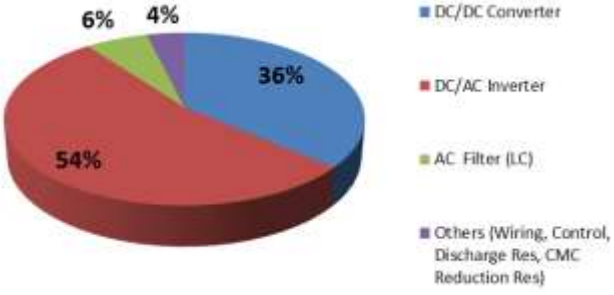


Figure 2: Pie chart of power losses

Several SiC device vendors claimed that it will release SiC module for DC-DC converters soon. These SiC modules are planned to be used in the final product of Gen-1 50kW PV inverter.

Figure 6: Mechanical Design

Experiment prototypes of DC/AC inverters: two prototypes of Si 3-level DC-AC inverter have been built and tested. The first prototype with oversized 400A IGBT module is used to develop and verify 3-level inverter control. The control has been successfully developed and tested in the first prototype. The second prototype use 100A IGBT T-type 12-in-1 module in order to reduce size. The preliminary testing results shows the isolated power supply, gate drive and power stage works well. More thermal runs of the second prototype are in progress. Another 3-level T-type 4-in-1 module that will be released soon will be also investigated due to its premium thermal performance.

Final Product Electrical Design: in order to reduce overall weight and size, the PCB-based structure instead of bus-bar based structure is used. Ten different PCBs have been defined inside the final product of Gen-1 50kW PV inverter. DC/DC converter includes three different PCBs. DC/AC inverter includes three different PCBs. A controller includes three PCBs and one more PCB is for auxiliary power and relay. The detailed functionality for each PCB has been defined and interfaces among PCBs have also been clearly specified. In additional to major power semiconductors, other major electrical components, such as contactors, fuses, chokes and sensors, have been either selected or designed.


Figure 7: Top view of internal mechanical structure

Final Product Mechanical Design: Ultra-light-weight and ultra-compact-size are two critical requirements on mechanical design. Preliminary design is shown in Figure 6. The size of The preliminary mechanical design demonstrates that overall size is 34 in × 29 in × 12 in, which is smaller than required 36 in × 36 in × 12 in stated in specification. The internal structure of the inverter is being designed. Figure 7 shows front view of the internal mechanical structure. Based on preliminary design of internal mechanical design and selection of cabinet material, the overall weight is about 138 pounds, which is less than 143 pounds in the specification

Technology to Market: The Global Market for PV inverters in 2016 has been predicted to be 56.23 GW. 21% of PV inverters will be Small Commercial PV inverters whose power ratings are from 10 kW to 99 kW. The market for Small Commercial PV inverters not only has a large market segment (11.8GW in 2016), but also has a very high growth rate (37% Compound Annual Growth Rate from 2014 to 2016).
The overall PV Inverter Market in the United States is predicted to decrease in 2017 due to Solar Investment Tax Credit (ITC) expiring by the end of 2016. Utility-scale PV Inverter market is predicted to drop around 70% in 2017 and Residential PV inverter market is predicted to drop around 40% in 2017. However, the Small Commercial PV Inverter market is predicted to drop only less than 20% in 2017 and rapidly recover in 2018.

By 2017, the competition in the PV inverter market will shift focus from availability and lead time to differentiated competitive advantages. Customers "will raise the bar" for the efficiency of the inverter. Customer will demand the easy-to-use, easy-to-transport, easy-to-install and friendly-to-inventory PV Inverter Systems.
Toshiba International Corporation (TIC) plans to release SiC Device-based Small Commercial PV Inverters to market at the beginning of 2018 when the market start recovering strongly from 2017. The differentiated competitive advantages (Ultra-high efficiency, easy-to-install, easy-to-transport and friendly-to-inventory) enabled by the use of SiC devices will attract both end customers and large integrators resulting in the long-term success for the product.

Moreover, local manufacturing and local field support is the best way to support customers from initial installation to after-the-market service. TIC is committed to manufacture in US and increase employment in the US. Starting from the 1970s, TIC has manufactured motor drives, UPS, solar inverters, energy storage inverters and motor in Houston to serve the customers in US and overseas. Currently, TIC in Houston has over 1 million square feet manufacturing facilities in Houston, TX. TIC has extensive experiences and broad channel with our end customers.

Plan for Next Budget Period If Funded: The objective in BP-2 is to finish most of design and building for the Final Product 50kW SiC Device based Small Commercial PV Inverter, leading to a product release in BP-3.

Natural convection cooling without fans brings a major challenge on mechanical design and thermal optimization. Mechanical design will be optimized in BP-2 by thermal simulation and thermal experiment with 3D-printing of the cabinet in order to achieve natural convection. Moreover, mechanical design will also be optimized to be manufacturing friendly to reduce assembly cost.

The final product has over 10 PCBs inside, including 3 PCBs for controllers and conditioning, 3 PCBs for DC/DC converters, 3 PCBs for DC/AC converters, 1 PCB for power & relay. These PCBs will be designed, built, tested and optimized in BP-2.

Advanced control (leakage current reduction, UL required protection and anti-islanding) will be developed in BP-2 and tested in the prototype built in BP-1.
A preliminary cost of the BOM and manufacturing will be analyzed in BP-2.
Moreover, several work force education seminars are also planned for the plant work force preparing BP-3 manufacturing in Houston.

Project Output: Submitted IP disclosures

- "Power Supply System of PV Inverter", Da Jiao, Peter Liu.
- "Electronics system incorrect-connection detection", Da Jiao, Peter Liu.

Organization: Transphorm
Task No./Project Title: 2.6: GaN Power Switches & Applications for Accelerating Market Development
Technical Point of Contact: Dr. Yifeng Wu
Sub-award start date: 02/01/2015

Project Objectives:

- To develop a low power AC-DC converter and a high power inverter that could be productized
- Develop devices for the high power inverter and compact AC-DC converter

Auxiliary objective:

- Provide devices and applications circuits to accelerate GaN power switch based power electronics at the Power America Center and its affiliated universities & power systems companies

Project's Contribution to the PowerAmerica Mission: The project's contribution to the Power America Mission is to begin the productizing of two categories of GaN power switches and products based on them via two power blocks: a low power AC-DC converter and a high power inverter covering the power range 100 W to 10 kW.

Technical Approach: To be able to meet the project objectives, the following sub-tasks are being implemented or have been completed:

- Task #2.6.1: High-frequency (HF) Adapter based on 600V GaN switch (S1) for compact adapter:
  - Complete prototype HF devices in SMD packages in mo-8;
  - Compact power supply prototype in mo-12.

- Task #2.6.2 High efficiency high power diode-free bridge/Inverter based on 900V GaN switch (S2)
  - Complete fabrication of HV devices in mo-8;
  - 2x device paralleling with Eff>98.5%@100kHz in mo-6;
  - 480Vrms inverter with Eff>98.5%@100kHz in mo-12.

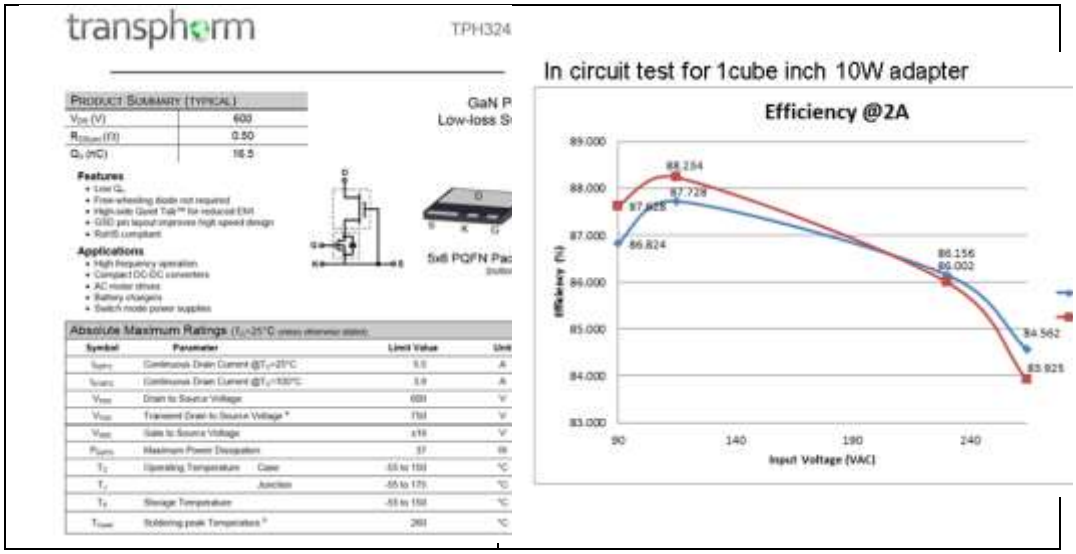
Issues, Risks and Mitigations: The biggest risk for the project is not technical. Based on the progress we have made so far, we feel we will meet all technical targets; but we feel that the next phase of productizing a technology, i.e. the process of taking the technology to the market, has considerable risks. While we are confident that the two product blocks will completed by the end of the project and we will meet the technical goals of the project, we are not quite sure what the process would be to take the technologies to the market. While we are in contact with various companies for such product classes, we feel that a more proactive approach by the Institute would greatly help in the process of technology-to-market.

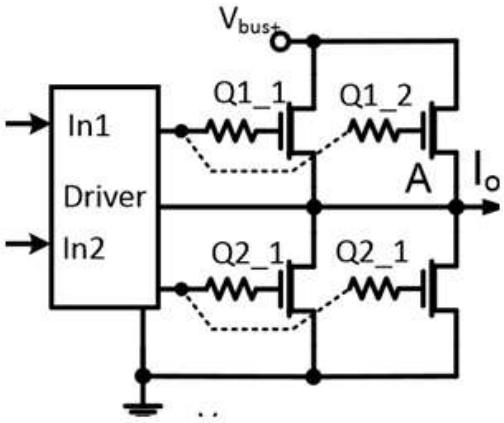
Significant Accomplishments: The following technical tasks have been have been accomplished:

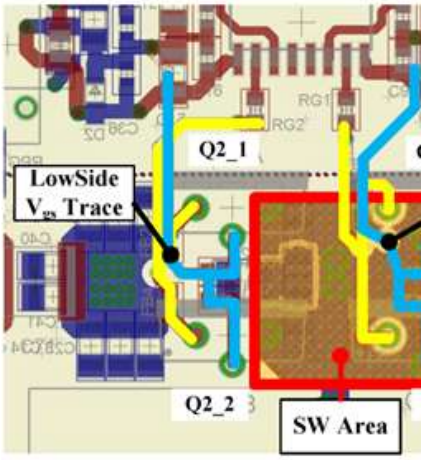
- Sub-task # 2.6.1:
  - Completed first round of prototyping HF devices in two types of SMD package – SO-8 and PQFN;
  - Preliminary datasheets have been made;
  - Device shared with a target customer to have it tested for a 100 W AC-DC fly-back converter.

- Sub-task # 2.6.2:
  - Initial epi and wafer fab lot completed
  - Wafer level data obtained
  - Initial switching tests performed
  - Packaged reliability tests to understand the limits of structure & epi performed
  - Second fab lot based on feedback has been fabricated and is under evaluation
    - To optimize structure design
    - Final design/mask based on learning
  - Meet program specs with structure & epi-layer that enables reliable switching to 720 V & passes JEDEC test
  - Using the prototyped devices the following power blocks have been tested:
    - TO220 and TO247 devices packaged and tested for paralleling in power blocks
    - 1.5kW and 3kW inverter stages made and tested (η > 98% at 100 kHz)

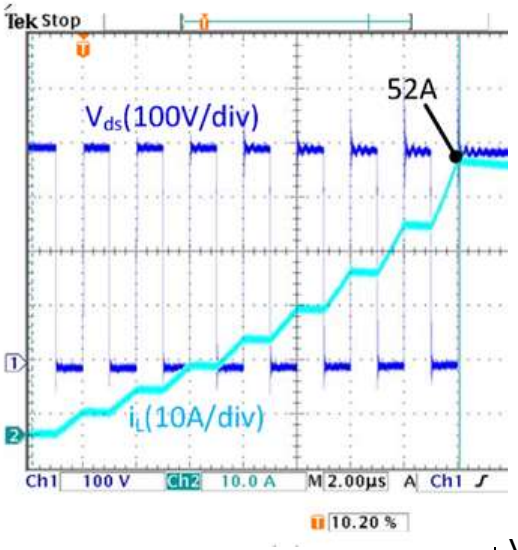
Some results supporting the claims above are tabulated below:



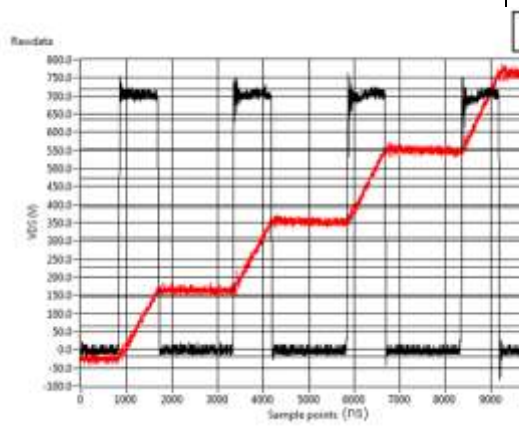




Circuit and board layout for paralleling and testing high speed GaN/Si switches.



Voltage and current waveforms showing paralleled GaN devices switching without oscillating.



Voltage and current waveforms showing 900V GaN/Si devices switching to 720V.

Technology to Market: Commercializing systems based on wide-bandgap power devices is one of the important objectives of Power America and Transphorm. We have done the following for T2M:

- Secure design wins and ramp GaN device sales for PV Inverter and compact Power supply/adapter products
- Ongoing customer engagement (US, World-wide)
- Sampled parts (after ensuring stable operation /qualification suitability)
- Supply chain is in place from epi to final packaged parts
- Package manufacturability needs to be improved (design/sub-con)
- A VP marketing has been tasked with securing US customers and target customers include US based PV Inverter makers, and end PV installers /providers and end users for high efficiency compact power supplies in IT and communications are being educated to create pull for these devices

Plans for Next Budget Period If Funded: There are two important areas we have proposed in the next phase:

- To take the 650 & 900V GaN/Si power switches to the next phase by packaging them in high performance half bridge packages so that the power electronics user community finds it easier to use these high speed switches.
- Design and document an *Open-Source Compact Transformerless Grid-Tied 3kW Inverter* using GaN power switches.

Both the above projects aim to accelerate acceptance of GaN power switches in the industry, research labs and universities.

Project Output: None so far on this project.

Milestone Summary

Subtask 2.6.1		High-frequency GaN switches (S1) & compact power converter (C1) (Months 0-12)		Month 4	Month 5	Month 6	Month 8	Month 9
	Milestone 2.6.1.1	(S1) Complete mask set and first lot of S1 fabricated. On wafer test specifications: HEMT BV > 700V, leakage current at RT < 0.1µA, Ron < 500 mΩ at RT (Month 4)	1	Done				
	Milestone 2.6.1.2	(S1) Complete development of PQFN package for S1 & tested to meet S1 specifications. (Month 8)	1				Done	
	Milestone 2.6.1.3	(S1) Evaluation successful for S1 at high frequency switching to 5 MHz: Stable operation waveforms obtained w/o failure (Month 9)						Jan 15 2016
	Milestone 2.6.1.4	(S1) Complete HTRB stress of S1 per JEDEC specs (80 devices stressed at 150 oC at 480 V for >500 hrs). Release beta samples with datasheet and price for lot quantity of 100. (Month 12) [Pass HTRB qualification with 80 devices x 3 lots and release beta samples for lot quantity of 1k at Month 18)						
	Milestone 2.6.1.5	(C1): Complete design and build of soft switching circuit with primary device loss < 5% at full power, operating at >5MHz, primary side converter power density >50W/cu.in. (Subcon, Month 9)						Jan 15 2016
	Milestone 2.6.1.6	(C1): Complete whole adapter/power supply prototyping meeting final spec of >30W/cu.in (2-3x of current market products), efficiency >90%, adapter surface temperature <60 deg C at 25 deg C ambient. Deliver 2 prototype units (Subcon, month 12) [Adapter/power supply preproduction passing EMI standard per FCC 15 / CISPR 22 class A and surge standard IEC 61000-4-5. Release commercial samples with pricing for >100 quantity (Subcon, month 18). Q1 and Q2 of year-2 will be primarily devoted to passing full JEDEC qualification of 1st generation of S1 and commercial release of adapter/power supply products. Q3 year-2 to Q4 of year-3 will be allocated to the development of the 2nd generation of S1 based on new understandings and feedback received from user groups.						
Subtask 2.6.2		High voltage GaN switches (S2) & diode-free bridge converter (C2) [Months 0-12]		Month 3	Month 5	Month 6	Month 8	Month 9
	Milestone 2.6.2.1	(S2) Epi developed for 900V GaN/Si switches. Vertical breakdown voltage required to support device rating of > 900V and epi-isolation breakdown field > 50V/µm. (Month 6)	1			Done		
	Milestone 2.6.2.2	(S2) Completed mask set and first lot of S2 fabricated completed. On wafer test specifications: HEMT BV > 900V, Leakage < 2µA at RT, R_{on} < 200 mΩ at RT. (Month 8)	1				Done	
	Milestone 2.6.2.3	(S2) Packaged S2 in TO247 or equivalent package and tested to S2 specifications. (Month 9). Complete initial HTRB test and release 1K engineering (alpha) samples with preliminary datasheet and price for Qty of 100. (Month 12)						
	Milestone 2.6.2.4	(C2): Completed inverter circuit for PV application with TO220 GaN switches, Vin=400Vdc, Vout=240Vac, Pout>2.5 kW with device paralleling, peak efficiency > 98.5% at PWM frequency =100kHz. (Month 6)	1			Done		
	Milestone 2.6.2.5	(C2): Completed inverter circuit for PV application with TO247 GaN switches, Vin=720Vdc, Vout=480Vac, Pout>2kW using single bridge and >4kW using device paralleling, peak efficiency > 98.5% at PWM =100kHz. (Month 12) Release inverter reference design for PV application 720V Vin, 480Vac Vout 4kW with complete documentation and pricing for quantity in 1-50 [Month 18]						
	Go/No-go Decision Pt	Show S2 working in a boost converter: 360Vdc to 720 Vdc, Pload > 2 kW, 100 kHz switching frequency, h > 98.5%. (Month 12)						50% Done

Organization: UCSB
Task No./Project Title: # 2.7: Dielectric Engineering with MOCVD dielectrics for D-mode HEMTs
Technical Point of Contact: Umesh K. Mishra
Sub-award start date: 02/01/2015

Project Objectives: A fabrication process for ternary dielectrics by MOCVD will be developed and the crystallinity for dielectric performance optimization tailored by adjusting the process parameters. The MOCVD process offers a much wider dielectric growth design space compared to other methods. Further advantages result from the opportunity to deposit the dielectric in-situ on top of the nitride device structures eliminating exposure to air. Oxide dielectrics such as Al_2O_3 and its alloys offer a high bandgap, high electron barrier, high dielectric constant and a high breakdown field, properties which make it a very promising dielectric material for device applications. An enhanced breakdown voltage combined with low gate leakage and low sheet resistance in (Al,Ga)N devices is expected. In subsequent years a target breakdown of 600 V is anticipated. A key advantage of AlGaN/GaN devices is the high electron mobility at a high charge density with a high critical electric field. In N-polar devices additional benefits result from the reversed direction of the internal electric fields in the device structures which enable a reduced source drain leakage in combination with a higher gate breakdown resulting from the increased effective barrier height in N-polar structures.

Project's Contribution to the PowerAmerica Mission: Successfully implemented, the novel dielectrics will allow to improve the performance of GaN based devices including reliability and durability of the devices and circuits while enhancing their manufacturability in general. While the developed dielectrics can be used for any group III nitride device, additional performance improvements will be achieved via the development of novel N-polar GaN based devices (to be proposed). In the course of the work on this program, future researchers are trained ensuring that a highly trained workforce is available to support US semiconductor industry needs.

Technical Approach: Al_2O_3 and $Al_xSi_{(1-x)}O$ dielectrics will be deposited using metal organic chemical vapor deposition (MOCVD). This technique uniquely provides *in situ* capabilities for depositing dielectrics on GaN-based structures without breaking vacuum, which helps form pristine, low-defect and low-contamination interfaces. In addition, MOCVD enables the use of various precursors and offers a wide range of growth conditions, which can drastically tune structural and electrical properties. This growth space will be thoroughly explored to determine conditions for producing high performance and reliable dielectrics. Different post-deposition annealing treatments will also be evaluated. Emphasis will be placed on achieving high-quality amorphous dielectrics.

In order to attain amorphous dielectrics in the high-temperature nature process of MOCVD, this work considers two viable approaches for parallel implementation. The first of which is to deposit Al_2O_3 at reduced temperatures without trespassing the limit of metalorganic pyrolysis efficiency. Simultaneously growth rates must also be raised to avoid restraining deposition kinetics while preventing significant carbon uptake. The second approach relieves the former restrictions by alloying Al_2O_3 with Si, which allows for amorphous $Al_xSi_{(1-x)}O$ dielectrics to be achieved at temperatures where Al_2O_3 normally crystallizes. This alloying of ternary constituents in MOCVD redefines a broader growth window and creates associated new growth opportunities. Both of these

approaches will be simultaneously explored in the context of their growth impact on material characteristics and reliability performance.

Material characteristics such as crystallinity, dielectric breakdown field, interfacial trap density, and fixed charges will be measured for each dielectric that result from a particular implemented growth condition. Additionally, gate leakage, hysteresis, and threshold stability under stress will be evaluated. The reliability of all the various output dielectrics will be assessed from the charge (and time) to breakdown performance. Integrating these various characterizations together, a holistic evaluation will qualify which best performing dielectrics will be down-selected for further application into HEMTs. Per each trial of analysis, oxide deposition conditions will be revised accordingly and reintroduced into the next characterization cycle for sustaining the objective of finding new dielectrics that can continuously push performance limits.

In further details of the proposed characterization process, metal-oxide-semiconductor capacitors (MOSCAPs) were grown as the test structures for probing dielectric properties. The following characterizations were performed on these *in situ* grown MOSCAP structures. Oxide layer crystallinity was analyzed from grazing incidence x-ray diffraction. Gate leakage and dielectric breakdown fields are determined from I-V measurements. Fixed charges, hysteresis, flat-band voltage, and interfacial trap density are determined from C-V techniques. Charge to breakdown is extrapolated from time-dependent measurements, which employ either a constant current or constant voltage stress to breakdown. This information can be used for estimating the dielectric lifetime and predicting module behavior in an applied device.

The newly developed dielectrics will be used for the fabrication of novel N-polar GaN based power transistors. Record mm-wave performance data were recently obtained for N-polar GaN devices developed under a different program. The combination of state-of- the dielectrics with a state-of-the-art novel device design suggests that an even stronger performance boost can be obtained under this program.

Issues, Risks and Mitigations: No specific issues or risks could be determined yet.

Significant Accomplishments: Prior to the inception of the program, we have developed in place an *in situ* MOCVD capability for depositing Al_2O_3 on GaN-based structures. Early studies from 2013 onwards contributed greatly to our understanding and control of dielectric growth engineering by MOCVD. A comprehensive study of the Al_2O_3 growth space had been detailed.[1] Atom probe studies were conducted to characterize bulk and interface quality.[2] Electrical traps of crystalline Al_2O_3 were evaluated at different growth temperatures.[3] Interfacial trap density and dielectric stress testing were also performed on these early trials of dielectrics.[4] From these works, we have established a detailed, comprehensive methodology that covers techniques from growth to characterization. Our developed toolbox allows us to exert finer control over the growth parameter space and our holistic characterization helps to make well-informed evaluations for each dielectric.

[1] X. Liu *et al*., J. Cryst. Growth **408**, 78 (2014)
[2] B. Mazumder *et al*., J. Appl. Phys. **116**, 134101 (2014)
[3] X. Liu *et al*., J. Appl. Phys. **114**, 164507 (2013), X. Liu *et al*., Appl. Phys. Lett. **103**, 053509 (2013), X. Liu *et al*., App. Phys. Lett **104**, 263511 (2014)
[4] R. Yeluri *et al*., J. Appl. Phys. **114**, 083718 (2013), R. Yeluri *et al*., App. Phys. Lett **105**, 222905 (2014)

We have applied these existing tools to the new dielectrics being investigated under this program. Our toolbox has since expanded to include time-dependent breakdown measurements for reliability testing. Under the funding guidance of ONR, ARPA-E and Power America, significant progress have been made towards the development of MOCVD amorphous oxides. In accordance with the proposed approaches towards achieving amorphous dielectrics, we have tested new growth conditions for Al_2O_3 and developed new growth windows for depositing $Al_xSi_{(1-x)}O$. In this past year, we have identified several MOCVD growth conditions that produced stellar electrical performances. The best dielectrics exhibited ultra-low hysteresis (ΔV_{FB} < 5 mV), reduced interfacial trap densities (D_{it}) on the order of ~10^{11} cm^{-2}, electric field breakdown (E_{ox}) up to 8.9 MV/cm, high threshold stability beyond 10 V (4 MV/cm), and record-breaking high charge to breakdown (Q_{BD}) > 13 C/cm^2. This large Q_{BD} reliability metric is an order of magnitude greater than any other Q_{BD} reported in III-nitride gate dielectrics that were tested under similar injection conditions. A predicted lifetime of 20 years was determined possible for operating gate conditions of ≤ 10 V (4 MV/cm) in thin films with thicknesses ~ 25 nm.

Details of the growth conditions that produced these results are not disclosed for public use as it is still proprietary information at this time. Partial results have been submitted for publication in JJAP and to the ISPSD conference. Moving forward, new knobs are being explored for improving dielectric performance, including sampling alternative Si alloying precursors for attaining ternary amorphous layers at even further reduced temperatures. Dielectrics will be evaluated on AlGaN/GaN platforms to prepare for the transition and implementation into HEMT devices.

Record W-band performance data were recently obtained for N-polar GaN devices developed under a different program and will translate to a breakthrough in GaN-based power conversion performance.

Technology to Market: Since all dielectrics under consideration in this program are grown in a commercial MOCVD tool, their fabrication process can be easily transferred to any production tool. The Al precursor is standard as are the investigated Si precursors, and existing additional gas supply lines can be used to add oxygen to the growth process.

As far as the newly proposed power transistor structure based on N-polar GaN is concerned, this process is running on 3 different MOCVD tool platforms at UCSB and was previously successfully transferred to a production tool at IQE in a record short time under the DARPA NEXT program for mm-wave applications.

Plans for Next Budget Period If Funded: The exploration and optimization of $Al_xSi_{(1-x)}O$ dielectrics will be continued. The current best dielectrics will be tested in novel deep recess N-polar GaN power devices which enable an enhanced manufacturability over conventional Ga-polar devices. The transition from Ga- to N-polar devices was a result of discussions with the Program Management. The novel N-polar devices will feature a reduced source drain leakage in combination with a high gate breakdown resulting from the increased effective barrier height in N-polar structures. In addition the novel device design will enable aggressive lateral scaling, inherently better dispersion because of the lower electric fields in the dielectric, enabling higher reliability and performance. Further benefits arise from the wider R_{on} versus breakdown design space.

Project output: One paper on the growth and properties of $Al_xSi_{(1-x)}O$ is under review.

Milestone Summary

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
2.7.1	Fabricate thin dielectric films with specific properties + Device application	Month 3	Dielectric work completed Device milestones were revised.
2.7.2	Fabricate thin dielectric films with specific properties + Device application	Month 6	Dielectric work completed Device milestones were revised.
2.7.3	Fabricate thin dielectric films with specific properties + Device application	Month 9	Dielectric work completed Device milestones were revised.

Organization: United Silicon Carbide, Inc.
Task No./Project Title: SOPO Task #2.2 - 1.2 kV Diode and MOSFET Foundry Qualification of 150mm SiC Line
Technical Point of Contact: Anup Bhalla
Sub-award start date: 2/1/2015

Project Objectives:

- Qualify SiC specific unit-processes at 150 mm Foundry
- 1200V, 100A Diode Qualified on 150mm SiC Foundry Line
- 40mOhm, 1200V MOSFET Qualified on 150mm SiC Foundry Line (Initial Qual)

Project's Contribution to the PowerAmerica Mission:–USCi's project has been to enable production of SiC products at a 6 inch foundry. In driving to complete our individual milestones, we have contributed to each of PowerAmerica's core missions: reducing the cost of WBG devices, scaling up production, demonstrating reliability and durability, manufacturing process development, as well as education and workforce development. We have transferred our 100 mm SiC process baselines to X-FAB, with a minimum of additional equipment, and used our established capabilities where outsourcing was necessary. This has allowed early successes and proof-of-concept demonstrations of 6 inch capability. Through our collaboration with X-FAB on both "public" and "proprietary" process technology, we have shared our technical experience from years of SiC processing, and contributed significantly to developing their WBG knowledge-base.

Technical Approach: USCi's Technical Approach has been to leverage our existing diode and MOSFET platforms and supply chain from 100 mm foundry operations and apply it to a 150 mm foundry expansion. This allows USCi to help with the development and installation of common processes for SiC processing at X-FAB, as well as install USCi proprietary processes for world-class products taking advantage of the cost benefits of 6 inch operations. At each stage, USCi made an effort to adapt to available tools and processes at X-FAB, deviating to USCi specific processes only at critical IP controlled steps.

Issues, Risks and Mitigations: The primary issues for delivering production ready diodes and MOSFETS from X_FAB are slow lot cycle time, and missing unit process capability. Both of these are due to an incomplete tool set and the need to outsource key process steps, including certain implants, implant anneals, Schottky surface preparation, and the entire backside flow. This has improved as X-FAB is working to acquire and install new tools (implant anneal, Back grind, laser anneal, and back metal deposition).

Significant Accomplishments: In the first year of PowerAmerica, USCi will accomplish its goals. We have transferred a number of key unit processes to X-FAB. These unit processes were used in the fabrication of 1200 V 100 Amp diodes, 650 V 10 Amp diodes, and 1200V MOSFETs. In processing these products we have identified some gaps in process technology needs, and ways to support these needs while parallel development work is ongoing. An example of this is the wafer back-side process. As X-FAB purchased and installed tools, and is bringing processes in-house, USCi managed the entire backside process through external vendors.

Through our hybrid flow, we have delivered high quality, high yielding diodes. Figures 1(a) and (b) show examples of the V_f and I_r behavior, and Table 1 shows the Median Test results for USCi's 650 V 10 A diodes processed at X-FAB. Our forward

voltage drop is right on target, and the reverse leakage is excellent. Wafer yield is >94% despite the many outsourced operations.

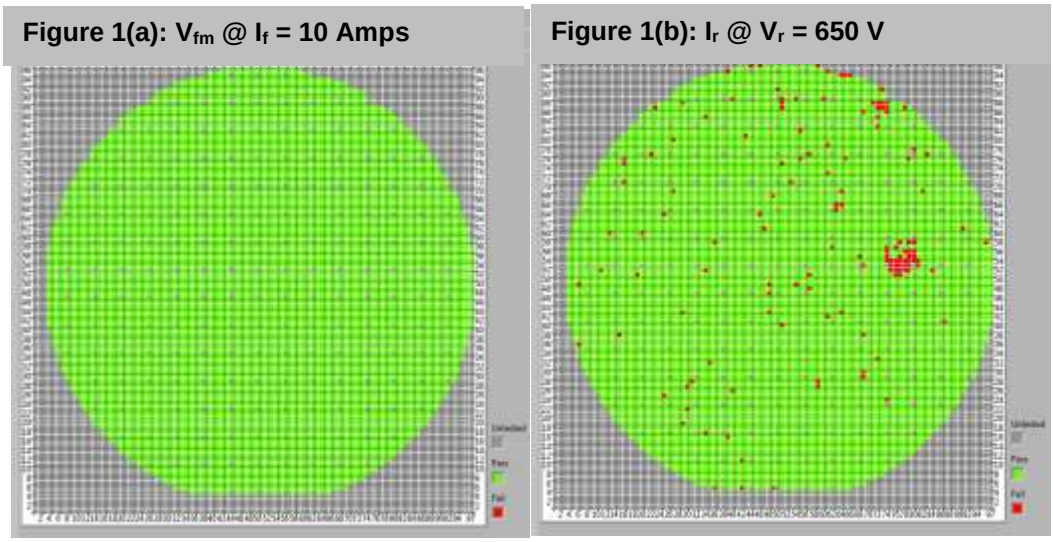


Figure 1: (a) V_f and **(b)** I_r data for USCi's 650V 10A diode product transferred to X-FAB

Table 1: Electrical Test Results (Median Values and Passing Percentages) for recent 650 V 10 A JBS Diode wafers after completing backside processing

	Bias 1	Bias 2	Lower Limit	Upper Limit	5	3
Wafer Total Dies					6777	6777
Wafer Passing Dies					6520	6382
Wafer Yield (%)					96.2	94.2
Median						
Vfm (V)	If=10A		1.30	1.70	1.46	1.43
Ir (A)	Vr=325V		0.00	5.00u	432.89n	273.00n
Ir (A)	Vr=650V		0.00	225.00u	11.80u	15.67u
Ir (A)	Vr=670V		0.00	800.00u	14.09u	20.93u

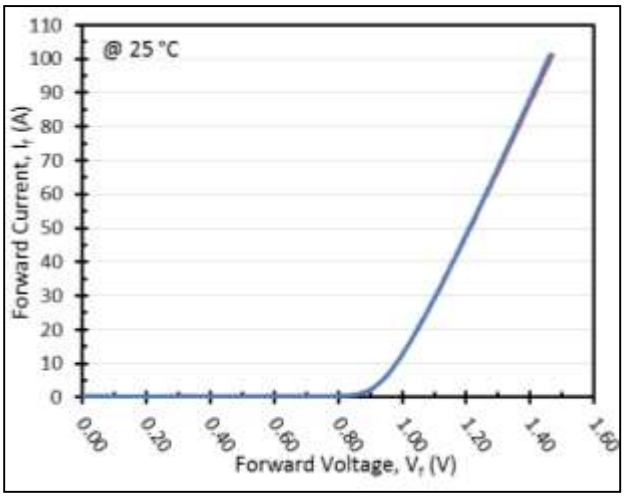
100A 1200V Diodes were set back by the scrapping of a lot due to issues at implant anneal. However earlier lots were able to be used to test back-side processing, sawing, and assembly. Vf was on target, but the leakage was higher, and we are refining process conditions.

(a)

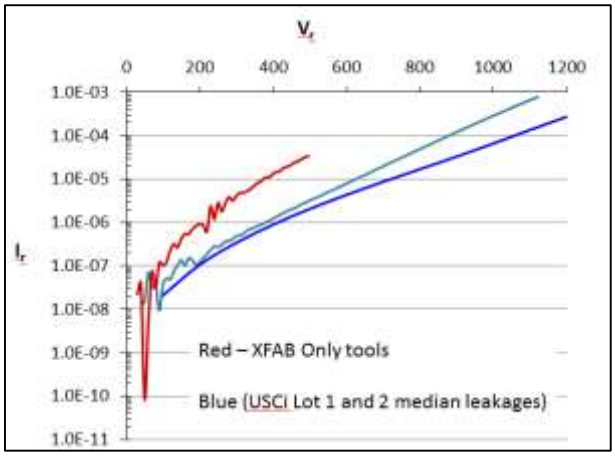
Early split

V_F at target

Thickness 150u



(b)



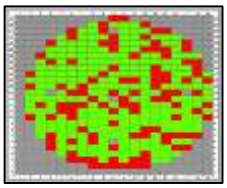


Figure 2: Wafer level testing of **(a)** Forward and **(b)** reverse IV-curves for first 1200V 100A diodes. (inset (a): picture of diode wafer, and inset (b) leakage yield)

As mentioned above, and as listed in Table 2, three lots were lost to issues at implant anneal, two MOSFET lots and one 1200V Diode lot. We are continuing to process our 1200V 100A diodes, and we are pushing our 1200V 40mΩ Vertical MOSFETs as hot lots. We should complete front side processing before the year is out, and with a no-cost extension, we will complete back-side processing, packaging, and burn-in within an additional 3 months.

Our vertical MOSFET is shown in Figures 3 (a) and (b). The gate structure, source contact, interlayer dielectric, and overlay metal are all visible.

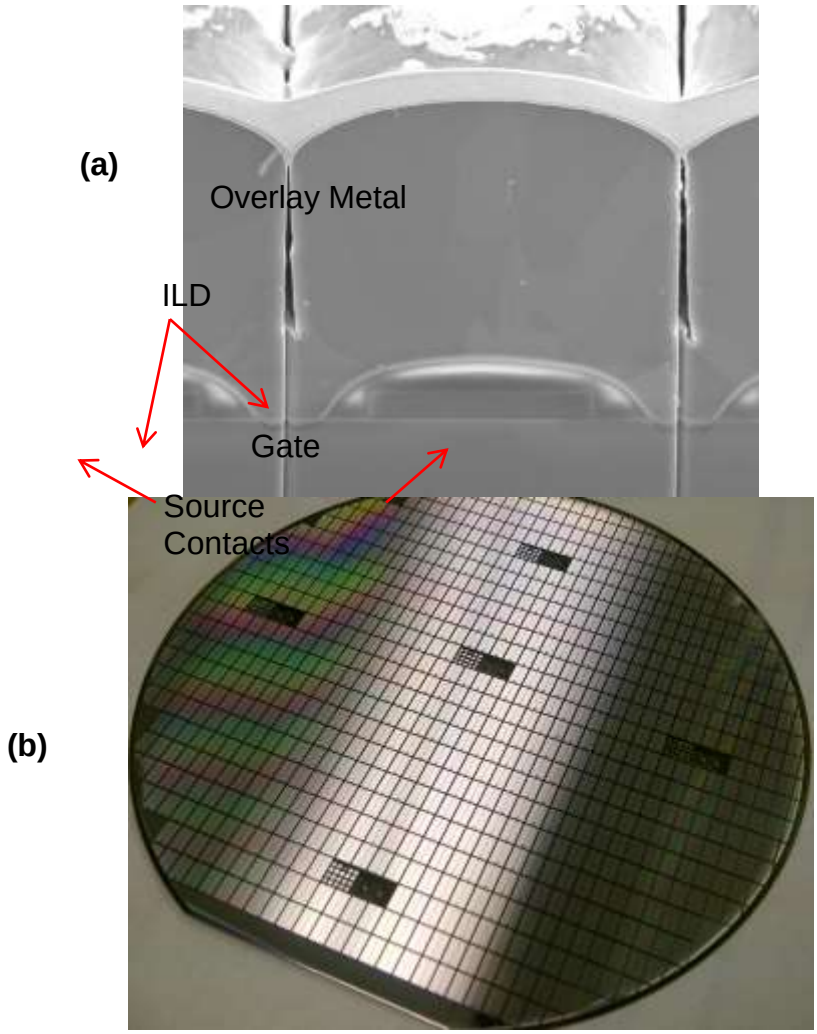
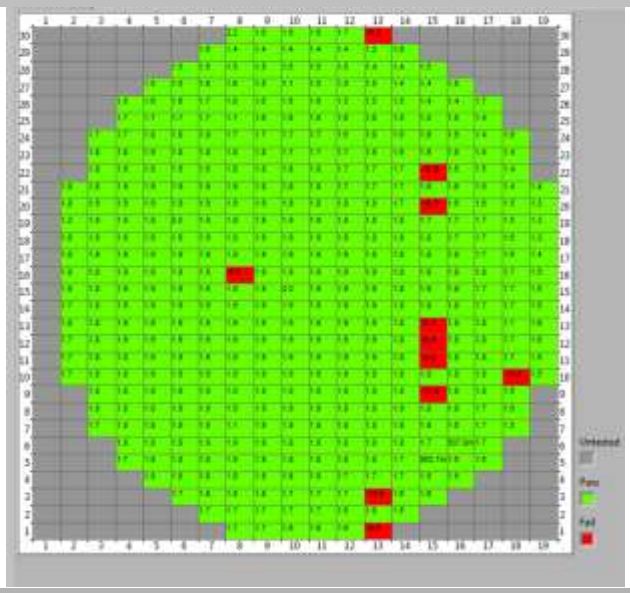


Figure 3: **(a)** MOSFET unit cell. **(b)** Picture of wafer

As part of our development efforts ahead of the Vertical MOSFETS, USCi ran processing splits on a Lateral MOSFET device (not funded by PowerAmerica) that would not require backside processing for characterization. We have demonstrated uniform and consistent threshold voltages and drain currents across a wafer. We have explored variables around gate processing, as well as device passivation. Different processing conditions have resulted in shifts in the threshold voltage, but the distribution of threshold voltages across a wafer has remained tight and uniform, as seen in figures 4 (a) and (c). Figure 4 (b) shows the uniform wafer map of the $I_{d, ON}$. This indicates that the process is uniform and a good benchmark or starting point for process splits and optimization. The place we do see some small variation is in gate oxide thickness (as extracted by CV measurements). When corrected for oxide thickness, the wafer to wafer variation in field effect mobility is negligible as seen in figure 4 (d).

Figure 4(a): V_{th} @ I_D = 1 μA and V_{DS} = 5 V



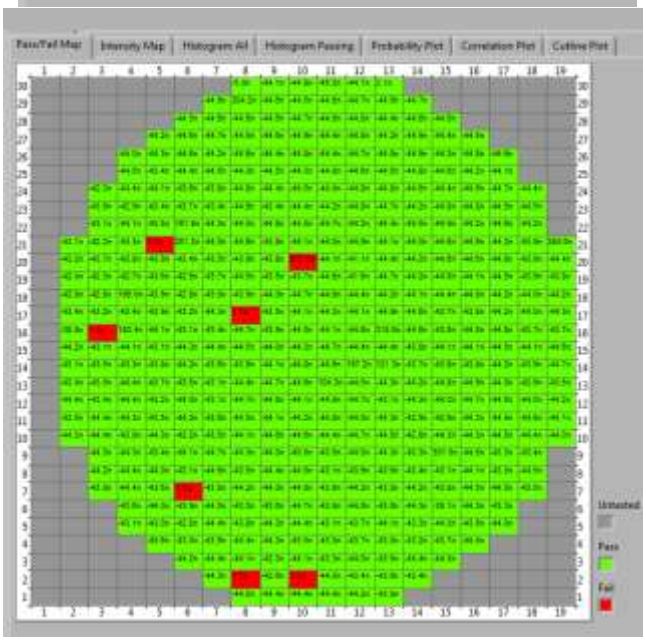


Figure 4(b): $I_{d, ON}$ at V_{GS} = 20 V and V_{DS} =

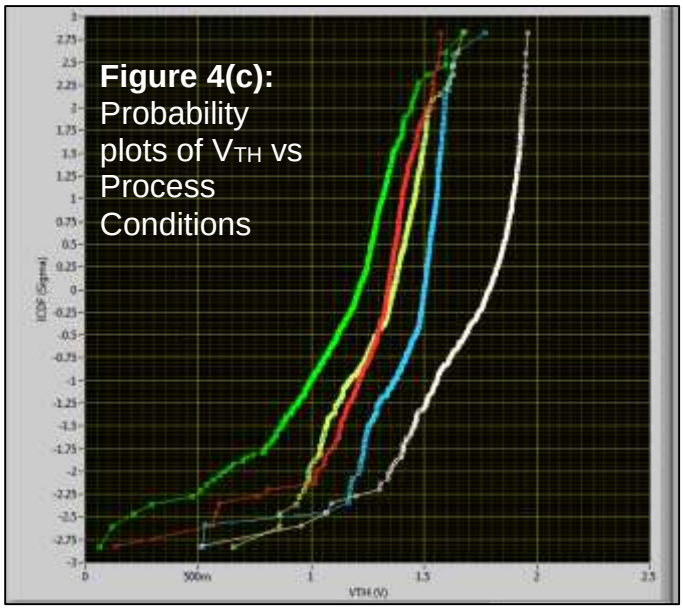


Figure 4(d): Extracted Field Effect Mobility

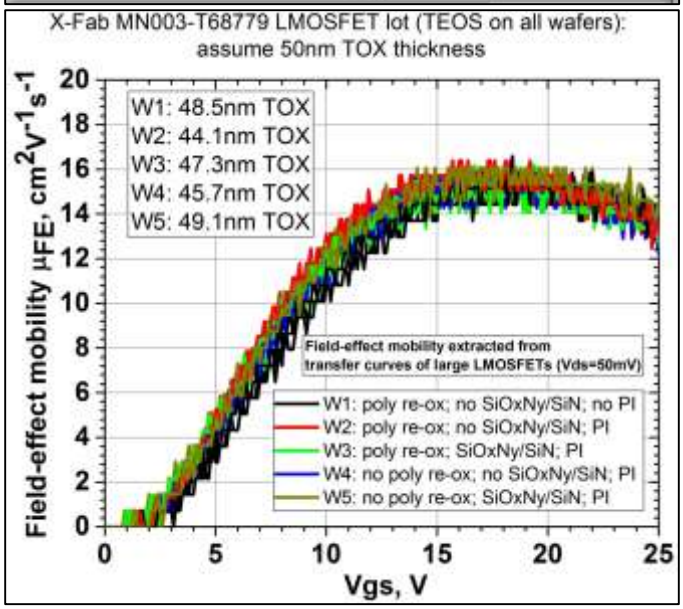


Figure 4: Example Lateral MOSFET device parameter maps for **(a)** Threshold Voltage (V_{TH}) at I_D = 1 µA and V_{DS} = 5 V, and **(b)** $I_{d, ON}$ at V_{GS} = 20 V and V_{DS} = 1 V. **(c)** Probability plots of V_{TH} showing shifts for various process splits. **(d)** Extracted Field Effect Mobility

Table 2: List of Lots run at X-FAB

Product	Type	Program	Lot	Splits Run	Results Summary
MOSFET	40m, 1200V	PowerAmerica	1		scrapped
MOSFET	40m, 1200V	PowerAmerica	2		scrapped
MOSFET	40m, 1200V	PowerAmerica	3	Passivation	@ Overlay Metal

Product	Type	Program	Lot	Splits Run	Results Summary
JBS Diode	100A, 1200V	PowerAmerica	1	schottky surface prep	Vf=1.45, Ir@1200V = 500uA - 1mA
JBS Diode	100A, 1200V	PowerAmerica	2		scrapped
JBS Diode	100A, 1200V	PowerAmerica	3	implant	@ Implant Anneal
JBS Diode	10A, 650V	other	1	schottky prep + implant + epi	Vf=1.45, Ir@650V = 11-20uA
JBS Diode	10A, 650V	other	2	schottk prep + implant	@ Schottky Prep
JBS Diode	10A, 650V	other	3		@ Implant

Technology to Market: USCI has installed key product technologies at X-FAB in Year 1, hereby moving the foundry model for SiC to 6 inch. Significant technology and cost improvements can be seen through improved yields, and processing consolidation.
JBS Diodes dominate the SiC market. The 100A, 1200V device slated to complete qualification shortly after Year 1 is very useful for co-packaging with Silicon IGBTs and SiC FETs in power modules. The large current rating reduces package complexity. In addition, 650V diode development has been started at X-FAB and shows the potential for high yielding, high performance devices. Since these devices dominate current market volume, transition to a 6" foundry is needed to expand into additional markets. Longer term, power MOSFETs will be released. Volume growth of these devices helps US suppliers of SiC wafers and epi, foundry services, and packaging services.
Several items are needed to reduce time to market. First is to enable more efficient development (both process and product). This can be helped with more readily available starting materials, and the installation of key processing and test equipment at the foundry. This accelerates development lots in process and speeds up the feedback loop for process improvements applied to later lots.
Feedback from Institute members who are designers/users of these devices can ensure that new products are filling an un-met need in the market. Institute partners who are engaged in system development with these new SiC products, can help identify more high impact applications, and give device and module manufacturers a more fully developed target for new product or process needs.

Plans for Next Budget Period If Funded: In Budget Period 2, the primary focus will be on qualifying and releasing 4 Amp to 10 Amp derivative 650V Diodes using all X-FAB equipment, with the exception of ion implantation. This is critical for customer acceptance and volume ramp in 2017. In addition to the 650V family, the 1200V JBS Diode family will be re-qualified using all X-FAB equipment. Transitioning from outsourced implantation to a fully in-house process flow may be explored as new process capabilities become available.

Based on funding, 3 lots of 1200V MOSFETS processed entirely on X-FAB equipment (implants conditional on process availability/readiness) will be run for JEDEC qualification.

Project Output: The output of USCi's portion of PowerAmerica is a demonstration a hybrid processing flow for production ready SiC Diodes and MOSFETs.

Milestone Summary

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
2.2.1.1	Member development agreement in place with foundry	0 mos.	Done
2.2.1.2	Member manufacturing agreement in place with foundry	12 mos.	Done
2.2.1.3	3 Major SiC specific process steps transferred to foundry	6 mos.	Done
2.2.2.1	Diode mask set designed and procured	3 mos.	Done
2.2.2.2	SiC wafers procured – substrates + Epi	3 mos.	Done
2.2.2.3	6 substrates for Equipment and unit step completed	4 mos.	Done
2.2.2.4	12 substrates for back grind and back metal set up	6 mos.	Done (Outsourced flow is working, X-FAB flow in development)
2.2.2.5	Engineering Lot 1 – yield and device characteristics reported	6 mos.	Done
2.2.2.6	Engineering Lot 2 – yield and device characteristics reported	9 mos.	Done
2.2.2.7	Qualification Lot 1 - yield and device characteristics reported. Target specifications: Median VF=1.5V, Max=1.7V at rated current, can only be measured accurately after packaging. Max Leakage <1mA at 1200V.	~~12 mos.~~ 13 mos.	Scrap event – replacement lot (650V 10A) completing @ 13 mos.
2.2.2.8	Qualification Lot 2 - yield and device characteristics reported. Target specifications: Median VF=1.5V, Max=1.7V at rated current, can only be measured accurately after packaging. Max Leakage <1mA at 1200V.	~~12 mos.~~ 13 mos.	In Process - Delayed due to lot 1 scrap event

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
2.2.2.9	Qualification Lot 3- yield and device characteristics reported. Target specifications: Median VF=1.5V, Max=1.7V at rated current, can only be measured accurately after packaging. Max Leakage <1mA at 1200V.	~~12 mos.~~ 14 mos	In Process - Delayed due to lot 1 scrap event
2.2.3.1	Mask Set designed and procured	6 mos.	Done
2.2.3.2	Lot 1: 1.2kV 40 mOhm MOSFET completed. Achieve target blocking >1200V @ 500 uA, target Rdson with Vth=2-3 V	~~6 mos.~~ 12 mos.	Lot 1 and Lot 2 scrapped – replacement lot (Lot 3) in process
2.2.3.3	Backside Processing of lot 1	~~9 mos.~~ 13 mos.	In Process
2.2.3.4	Packaging and Burn in completed for lot 1	~~12 mos.~~ 14 mos.	In Process

Virginia Tech

Organization: CPES, Virginia Tech
Task No./Project Title: Task 4.8 High Frequency GaN Converters for Distributed Power Systems
Technical Point of Contact: Dr. Fred C. Lee
Sub-award start date: 02/01/2015

Project Objectives: Data center is growing at a rate of 20% annually in the past decade. With increasing cloud computing and big data, it is expected that data center alone will consume 10% of the total electricity by 2020. Presently, all major devices such as multi-core processors, memories, chip sets, and hard drives, et al. are powered from a 12 volt bus. This 12 V bus architecture was developed in the early 90's, when power consumption was minuscule in comparison with today's usage. The i^2R related copper loss for 12 V bus is excessive. Recently, IBM has adopted a 360 V DC bus and 48 VDC bus for their next generation super computers. Google has adopted 48 VDC bus for their data centers. To support these power architecture changes, it is mandatory that the power conversion devices off the utility lines to be in a form of distributed power on the printed circuit board in the vicinity of the core processors and memory devices. The distributed power conversion devices have to be very efficient and with high power density to be compatible with core processors, memories, et al. Present power conversions devices are operating at 50-100 kHz with a power density less than 50 W/in3. An order of magnitude power density improvement is necessary for the wide spread use of the distributed power for all computer servers and data centers.

The project objectives are including dramatic increase of the power density of front-end converter from today's 30-50 W/in^3 to 100-150 W/in^3, and the front-end power processing to be fully modularized. In this manner, a customized power system can be synthesized by using simple modular building blocks such as multi-phase boost power factor correction (PFCs), and high voltage DC/DC converters and DC/DC transformers (DCXs) for input/output isolation.

Project's Contribution to the PowerAmerica Mission: The successful demonstration of GaN devices for the chosen applications will lead to wide spread use of GaN converters to replace the Silicon counterparts for all forms of switch-mode power supplies including but not limited to computer, telecommunication, network products, data centers, PV inverters, battery chargers industrial and consumer electronics products. This paradigm shift is accompanied with significant improvement of efficiency, power density and cost. Furthermore, the proposed GaN based power supply with PCB winding inductor and transformer can enable a fully automated manufacturing to greatly reduce labor content in the assembly process, which will give U.S. very competitive position to manufacture this high performance power supply.

Technical Approach: In the proposed effort, we will use high voltage GaN devices for the server power supplies to push its frequency 20 folds, from today's 50-100 kHz to 1-5 MHz. As a result, the power density of front-end converter can be dramatically increased from today's 30-50 W/in^3 to 100-150 W/in^3.

A 1 kW data server power system will be demonstrated with GaN based front-end converters including multi-phase PFCs and DCX, operating at 1-5 MHz. PFC stage will achieve 300-500W/in3 power density and 98% efficiency; DC/DC stage will achieve 700-1000W/in^3 power density and 96% efficiency. Both PFC rectifier and DC/DC converter will be designed with PCB integrated magnetic components. Traditional Litz wire PFC inductor on a toroidal core is hand wound with poor

tolerance. In the proposed work, we will replace it with a two-phase inverse coupled inductors with windings integrated into a four-layer printed circuit board (PCB). In addition, we can integrate two additional inductors into the same magnetic structure to reduce EMI noises (a patented technology developed at CPES). For DC/DC converter, we can replace the bulky transformer with a matrix structure of 8 transformers with PCB windings. The PCB integrated magnetic design will enable a fully automated manufacturing.

Issues, Risks and Mitigations: None

Significant Accomplishments: The driving circuit for GaN device is evaluated in the first. As the switching speed of GaN device is much faster than its Si counterpart, the driver should be able to handle high dv/dt and high di/dt conditions. Through our research, a batch of noise immunity techniques are proposed including important PCB layout rules to avoid primary-secondary overlapping, and to minimize boot-strap charging loop; selection of small parasitic capacitance digital isolator to achieve PWM signal level shift; and noise filter and negative bias circuits right in front of in driver inputs. Finally, the driving circuit is developed with high noise immunity like dv/dt>100 V/ns and di/dt>10A/ns. At the same time, the driver has propagation delay less than 20ns and high frequency capability up to 5MHz.

Different available 600V-class GaN devices are collected and studied including both E-mode GaN and D-mode GaN in cascode structure. A series of double-pulse testing are conducted with different devices in similar test setup. The measured switching loss indicates that for all of GaN devices, the turn on loss is high and the turn on loss is small. Furthermore, the turn off loss of E-mode GaN device is smaller at low turn-off current and then it goes up quickly due to miller effect. On the contrary, the cascode GaN has relatively flat turn-off loss when turn-off current increased. This is due to the current source turn-off mechanism discovered by us. With this deep understand of different GaN devices, we chose best candidates for both PFC and LLC design.

Then hard switching and soft switching is compared. Very different with many people's first impression, soft switching not becoming less important but becoming even more important for GaN device to operate at MHz high frequency. This is because hard switching brings lots of troubles to GaN device like significant turn-on loss, poor efficiency, and tremendous parasitic ringing and related driving issues and EMI noise issues. Soft switching is proved to be the right way to fully utilize the advantages of GaN device particularly for MHz converter design. This conclusion is reinforced by analysis, simulation, and experiments.

The topology of both AC/DC stage and DC/DC stages are selected. Totem-pole topology is becoming the most suitable one for GaN due to its simplicity and symmetry. LLC is still considered as the most attractive topology for DC/DC stages with higher potential offered by GaN. The totem-pole PFC can operate at 1MHz to 5MHz with >98% efficiency. The LLC converter can operate at 1MHz with >97% efficiency.

Then packaging is becoming another bottleneck for GaN device. Traditional packaging has large parasitics thus it limits the performance of GaN device. Packing impact is previously studied in CPES. As a continued efforts, a preliminary module is designed with interconnect parasitics less than 3 nH and good thermal dissipation capability. The developed full-bridge GaN can be used for 1.2kW totem-pole PFC very efficiently and its volume is less than 20cm^3.

Finally, magnetic design is also studied in this year. Different high frequency core materials are evaluated by CPES proposed test setup. The core loss of each material is measured under non-sinusoid excitation with DC bias for frequency range 1-5MHz. Then best magnetic material for PFC inductor and DC/DC transformer are identified at 1 MHz with core losses fully characterized according to the way they are used in the proposed circuit operation. Specific data are including core loss density <60kW/m^3 with Bac_pp=15mT, Fs=3MHz.

Technology to Market: The demands for AC/DC front-end converters are growing rapidly in recent years, including but not limited to computers, telecommunication, data centers, battery chargers, industrials, and aerospace applications. Collectively, these products consume more than 10% of the total electric power. One percent efficiency improvement in this industry sector represents 20 TWH of energy saving, which is equivalent to the total energy outputs of three average size nuclear power plants, each at 7 TWH annual production. Moreover, with the increasing of cloud computing and big data, it is expected that data center alone will consume 10% of the total electricity by 2020. Typical 1kW AC/DC power supplies is labor intensive in terms of manufacturing and assembling processes. Forty percent of the components are manually inserted. Thus, manufacturing of switching power supplies are largely moved off shores to low labor cost countries. The trend will not reverse unless there is a paradigm shift in the way we design and manufacture these power supplies.

Within the above mentioned industry sector, data center server power supplies are the most performance driven, energy and cost conscious. Within a data center, all major devices are powered from a 12V bus. This 12V bus architecture was developed in the early 90's, when the power consumption was minuscule in comparison with today's usage at 100A-200A levels per CPU. The i^{2}R related copper loss for 12V bus is excessive. In order to place the high voltage DC/DC converter on the CPU board (mother board), this converter has to be very efficient and high-density to be compatible with core processors, memories, et al. Today, power converters are designed to operate at 50-100 kHz with a power density less than 50 W/in^3 and they are not suited for the intended applications. Recently, the International Electronics Manufacturing Initiative (iNEMI) at the behest of IBM and other server manufacturers undertook a project to develop an industry standard for DC-DC converters. This converter is used to step down 380V directly to 12V and placed directly on the motherboard. This architecture will eliminate the use of bulky cables and the losses associated with them. This proposed power architecture is deemed superior to current practice. With the elimination of online UPS and cables and harness, the efficiency improvement is estimated at least 5%. A survey by iNEMI suggested that the power supply with the target efficiency (97%) and form factor (500W/in3 power density) is not readily available. It is highly unlikely to achieve this tall order with current design practice using silicon devices. This iNEMI initiative indeed

signifies a potential paradigm change and, thus, presenting a great opportunity for GaN to make an en route to this high volume market. CPES currently has more than 80 industry members. Many of them have direct interest in the data center related business. In this project we will work closely with our industry members, such as Emerson, Delta Electronics, Texas Instruments, Intel, Eaton, ABB to pursue product development for commercialization. Since the proposed power supply is built with PCB winding inductor and transformer, it is well suited for manufacture automation.

Plans for Next Budget Period If Funded: Building upon the advances we have made during the Year 1 effort, the proposed work in Year 2 will be focused on developing a MHz GaN based front-end converter with 99% efficiency for PFC stage and 97-98% efficiency for DC/DC stage. Both PFC and DC/DC stage will achieve 700-1000W/in^3 power density. This high density high efficiency front-end converter can be used in today's AC datacenter, as well as the next generation of Data center proposed in the iNEMI initiative.

There are four major goals/milestones we will achieve for next budget period. The first one is to design coupled inductor for the dual-phase interleaved totem-pole PFC. The coupled inductor will be integrated with PCB so it could be automatic manufactured. Balance technique will also be applied in the coupled inductor design so that the common-mode noise of PFC can also be reduced and the input EMI filter can be further simplified.

The second goal is to further optimize the DC/DC stage to meet both efficiency and density requirement of iNEMI initiative for future Data center. This high density DC/DC stage could be used for both AC and DC Data center

The third goal is to optimize the design of EMI filter for the whole system. The PFC and LLC converters will operate in series and the total EMI noise will be minimized by applying both balancing and shielding technics. Then EMI filter for this front-end converter will be optimized to suppress the remaining noise. It is estimated that the structure of EMI filter can be simplified from two stage to single stage due to the MHz high frequency operation.

The fourth goal is to achieve programmable outputs (12V, 5V) for DC/DC stage. This function can be realized within a single converter topology and a single digital controller. This simple controller incorporates the CPES patented state-trajectory control techniques with significantly improved performances including: soft start-up and short-circuit protection to minimize stresses; auto-tuning; fast load transient response; burst mode for light load efficiency improvement.

Project Output:

[1] Zhengyang Liu, Zhengrong Huang, Fred C. Lee, Qiang Li, and Yuchen Yang, Operation Analysis of Digital Control based MHz Totem-pole PFC with GaN Device, 3rd IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Nov. 2–4, 2015

[2] Zhengyang Liu; Zhengrong Huang; Fred C. Lee; Qiang Li, "Digital-Based Interleaving Control for GaN-based MHz CRM Totem-pole PFC", to be published at APEC 2016

Milestone Summary

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
4.8.1.1	High frequency driving circuit for GaN device	Month 3	Complete
4.8.2.1	Identified suitable converter topology for PFC stage	Month 6	Complete
4.8.3.1	Preliminary GaN module design	Month 9	Complete
4.8.4.1	Magnetic materials characterization	Month 12	Complete

Virginia Tech

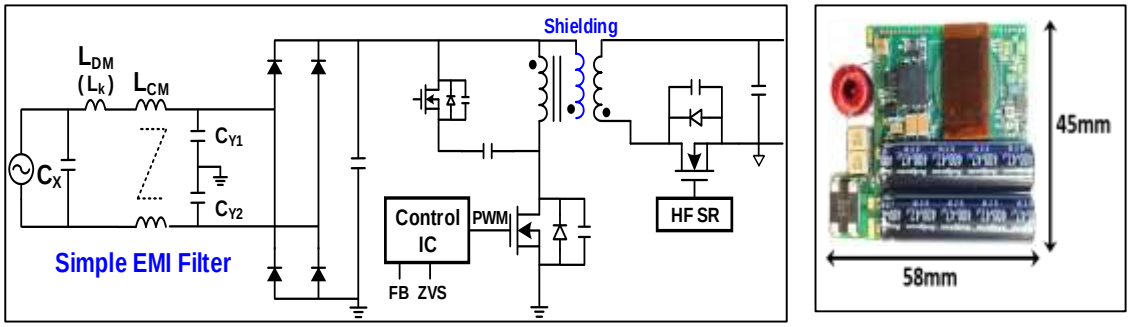
Organization: CPES, Virginia Tech
Task No./Project Title: 4.7 High-density high-efficiency adapter
Technical Point of Contact: Dr. Fred C. Lee
Sub-award start date: 02/01/2015

Project Objectives: One of the biggest market of power supplies, in both volume and dollar, is the ac-dc adapter/charger for consumer electronics. Todays, most of the adapters are operating at relative low frequency (<100 kHz) with the state-of-the-art efficiency up to 91.5%. The adapter power density is rather meager, at 6-9 W/in^3.

The emerging gallium-nitride (GaN) device is deemed as a game changing device in this particular application with improved efficiency and significant size reduction. Our initial experiments using the first generation of GaN devices were conducted with 10X increase in switching frequencies and 5X improvement in power density. We will develop 65W and 45W adapter prototypes with GaN devices to achieve 26W/in^3 and 20W/in^3 in power density, respectively. The prototype efficiency should be higher than 92% and the temperature should be lower than 70℃.

Project's Contribution to the PowerAmerica Mission: In this project, we will collaborate with an Institute industry member to develop a GaN device with targeted design for this application. We also partner with another Institute industry member to develop a high-density high-efficiency adapter suitable for commercialization. More importantly, the proposed adapter is built with PCB winding transformer, the automation manufacture can be realized to significantly reduce labor content, which will give U.S. very competitive position to manufacture this high performance adapter.

Technical Approach: High frequency is the major catalyst for size reduction in the advancement of adapter technology. The emerging GaN device, with much improved figures of merit, opens the door for operating frequency well into the MHz range. To realize the benefits of GaN devices resulting from significantly higher operating frequencies, a number of issues have to be addressed, such as converter topology, magnetics, control, packaging, gate drive and thermal management. The research team at CPES has successfully demonstrated in the Year 1 of the program that the GaN based adapter design is capable of operating at 1-2 MHz frequency with an improved efficiency up to 93.5%, together with 27W/in^3 density which is 3X improvement compared to the state-of-the-art product. Since the prototype is selected at 45W and 65W power level and hence, no power factor requirement, a simple flyback converter is chosen as shown in Fig 1. This topology is universally selected by all products under 75W for low cost.



(a) Active clamp flyback diagram (b) preliminary prototype

Fig. 1 MHz active clamp flyback front-end converter

Even though the topology is common, we have implemented a number of unique features

as listed below:

- Active clamp circuit is applied to recycle the transformer leakage energy and realize soft-switching for the primary switches. The di/dt and dv/dt are significantly reduced with soft-switching which is beneficial for high frequency EMI reduction.
- Over 90% of switching related losses are eliminated by soft switching for both the primary side and secondary side devices, which allows for MHz or even higher frequency operation.
- Common-mode noise is significantly reduced using the patented shield layer based on PCB winding based transformer [10]. The shielding is effective through all the conducted EMI testing frequency range (150kHz~30MHz) with over 20dB reduction of CM noises and, thus, simplifying the EMI filter design to a single-stage. It should be noted that the high frequency flyback transformer winding is implemented for the first time using only 6-layer PCB board.
- PCB winding transformer is used to build the proposed high density adapter, the automation manufacture can be realized to significantly reduce labor content

Issues, Risks and Mitigations: None

Significant Accomplishments: During year 1 program, we have completed all the subtasks and meet the milestones. To sum the major task of year 1:

- We have done evaluation and characterization for different type of GaN devices, including enhancement mode GaN and depletion-mode GaN in cascode configuration. We identify that hard-switching turn-on is detrimental from both efficiency and noise point of view. Soft-switching is still desired for GaN at high frequency operation. Packaging is also critical to GaN devices in terms of switching loss and gate ringing. We have proposed a better package for cascode GaN devices which enhance the device performance significantly. Actually our package concept has been adopted in several manufactory's recent GaN devices.
- We have developed a suitable driving circuit for GaN devices, especially for high side switches, that can achieve high dv/dt immunity up to 150V/ns as well as fast driving capability.
- We have developed a high frequency synchronous rectifier driving method to tackle the current oscillation which only occurred at very high frequency.
- We have identified a suitable topology for low power adapters using active clamp flyback converter. This topology can recycle the transformer leakage energy and realize ZVS for primary switches which is beneficial for both efficiency and EMI aspect.
- We have applied shielding technique to reduce the common-mode noise which can further increase the corner frequency of the EMI filter, and therefore, shrink the filter size significantly.
- We have used finite-element-analysis to model and design the preliminary PCB winding based transformer to achieve small winding loss and leakage inductance. It should be noted that the high frequency flyback transformer winding is implemented for the first time using only 6-layer PCB board including shielding

layer.

- We have designed a preliminary power-stage hardware to demonstrate the advantage and benefits of increasing the switching frequency with GaN devices. We have achieved above 93% in efficiency and over 27W/in^3 in power density.

Technology to Market: One of the biggest market of power supplies, in both volume and dollar, is the ac-dc adapter/charger for consumer electronics, including laptop, tablet, smart phone, mobile devices, game console, printer, and stereo sound-bars, etc. The market is projected to surpass $8 billion in 2015 and reach $9 billion by 2018; with much of this growth being driven by smart phones, tablets and a number of emerging applications. CPES currently has more than 80 industry members. Many of them have potential to commercialize the proposed high frequency GaN adapter. In this project we will work closely with our industry members, such as Texas Instruments, ON Semiconductor, Sonos, Delta Electronics, to pursue product development for commercialization.

Plans for Next Budget Period If Funded: We want to improve the year 1 design with higher efficiency and density as well as standardized system structure for wide power range adapters. As the plan of year 2 program, we will work on an innovative universal topology that is based on a two-stage approach as show in Fig.2. For power less than 75W, the first stage serves two functions: 1) to replace the diode bridge with active switches. The expect efficiency improvement is about 0.5-1%; 2) Instead of serving as a PFC circuit, the first stage can provide harmonic injection, resulting to a much reduced bulk capacitor. For power greater than 75W, the first stage will serve as a bridgeless PFC. This topology, while not practical for silicon devices due to excessive switching losses and body diode losses, is deemed very effective for GaN devices operating in multi-megahertz. The bulky electrical capacitor can also be reduced to some extend with harmonic injection as long as the input current can meet the requirement (IEC 61000-3-2). The second stage is a LLC resonant converter and is usually operating at a semi-regulated mode. The switching frequency is very close to resonant frequency to minimize conduction loss and switching loss. The SR driving signal can be the same as the primary PWM signal that can significantly simplify the system control. The transformer of the 2nd stage will be implemented using PCB winding for efficiency, density and easy automation consideration. The anticipated system efficiency is over 95% and the power density can reach 50W/in^3.

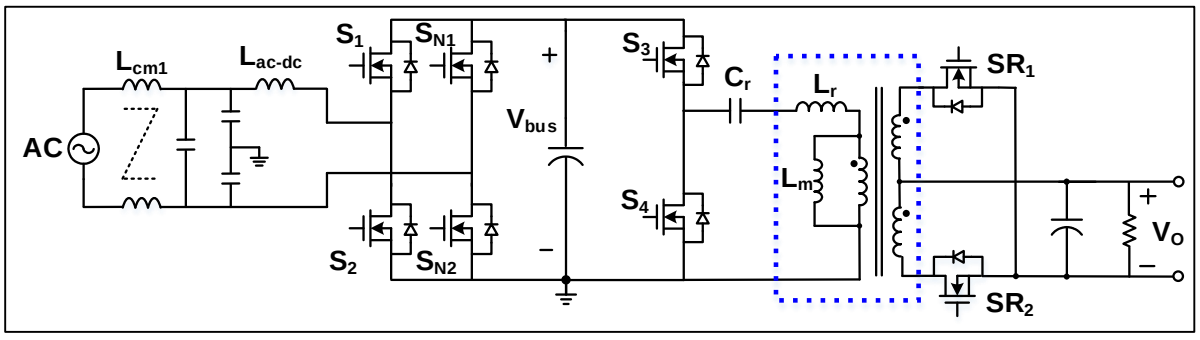


Fig. 2 Universal two-stage structure for wide power range adapters

1. Project Output

[1] X. Huang, T. Liu, B. Li, F. C. Lee, and Q. Li, “Evaluation and applications of 600V/650V enhancement-mode GaN devices, ” in proc. IEEE WiPDA, 2015.

[2] X. Huang, J. Feng, W. Du, F. C. Lee, and Q. Li, “Design consideration of MHz active clamp flyback converter with GaN devices for low power adapter application,” in proc. IEEE APEC, 2016, to be published.

[3] X. Huang, J. Feng, F. C. Lee, and Q. Li, "Conducted EMI analysis and filter design for MHz active clamp flyback front-end converter," in proc. IEEE APEC, 2016, to be published.

[4] Y. Li, F. C. Lee, Q. Li, X. Huang, and Z. Liu, “A Novel AC-to-DC Adaptor with Ultra-High Power Density and Efficiency,” in proc. IEEE APEC, 2016, to be published.

Milestone Summary

Milestone No.	Short Title	Due date	Status (complete/incomplete, notes)
4.7.1.1	GaN driving evaluation	Month 3	Complete
4.7.2.1	GaN switching characteristic	Month 6	Complete
4.7.3.1	Topology evaluation	Month 9	Complete
4.7.4.1	Transformer design	Month 12	Complete

Organization: X-FAB Texas, Inc.
Task No./Project Title: Task 2.1: SiC Power Device Commercial Foundry Development
Technical Point of Contact: Andy Wilson, andy.wilson@xfab.com
Sub-award start date: 02/01/2015

Project Objectives: X-FAB Texas will develop a "device agnostic" 6-inch silicon carbide (SiC) commercial foundry. Ultimately, the transition to a commercial foundry model for SiC power device fabrication will enable companies with a variety of device technologies (Diodes, JFETs, MOSFETs, etc.) to utilize the foundry for volume production. Rather than building a SiC fab from scratch, an existing 6-inch silicon foundry will be converted to process SiC wafers. This approach will leverage existing silicon processing equipment, but will require the addition of specialized equipment unique to SiC processing as well as the development of SiC unit processes that can be run on the existing silicon processing equipment.

To provide scalability such that multiple companies can use the foundry for their device of interest a Process Installation Kit model will be used. In addition to having a baseline process in place, this will allow companies to transfer their existing process flows to the 6-inch SiC wafer foundry while maintaining propriety control over specific process steps that may be viewed as critical IP. By sharing baseline unit process steps and the capacity that will be installed, Institute member companies will enjoy the cost and scalability benefits of a large wafer fabrication facility even though they would not individually be in a position to support such a large scale operation. By establishing this foundry domestically, Institute members will not need to send their production overseas which could jeopardize the security of their design and process IP.

Project's Contribution to the PowerAmerica Mission: The Open SiC Device foundry established in this task will be instrumental in achieving the DOE's goal of price parity between SiC and Si devices. Bringing the scale and manufacturing efficiency of an established Silicon foundry to Silicon Carbide will enable drastic reductions in the cost to process a 6-inch SiC wafer. Additionally, a foundry will be able to aggregate the SiC EpiWafer demand of multiple customers and bring the purchasing power to the market that will reduce the cost of SiC starting wafers. Finally X-FAB will work to establish Standard process (Subtask 2.1.5) that will enable process harmonization and cost reductions for all customers utilizing the Open Foundry.

Technical Approach: Over 90% of the processes required to fabricate a Silicon Carbide device wafer can be realized on standard silicon fabrication equipment. This equipment will need to be modified in order to accommodate the fact that SiC wafers are thinner than Si wafers and transparent while Si wafers are opaque. The tool modifications performed as part of Subtask 2.1.3 will result in existing Silicon tools installed in X-FAB Texas being able to run both Silicon and Silicon Carbide wafers. This model will allow the fixed costs related to these tools to be shared between both Silicon and SiC production enabling a more cost effective approach than a model where a dedicated SiC line is established and SiC wafers must absorb the full fixed cost.

For the processes that cannot be supported on existing tools, equipment will be purchased as part of Subtask 2.1.1 to develop a pilot line within the X-FAB Silicon foundry fab that will close these gaps and provide capability to support all processes that are required to fabricate SiC Device Wafers.

Issues, Risks and Mitigations: It should be recognized that establishing a full flow SiC open foundry line in parallel with a running Silicon foundry fab has never been

demonstrated. Risks exist with regards to cross-contamination of non-compatible materials, inability of Silicon based tools to achieve required capability in SiC processes as well as demonstration of the concept to run Si and SiC interchangeably on shared equipment. Risk will be mitigated by providing for equipment redundancy (when possible), along with establishing and maintaining relationships with external processing vendors that would allow for continuation of support in the event that internal capabilities are compromised.

Significant Accomplishments: The X-FAB Texas team has accomplished most of the milestones ahead of schedule. Working with Institute device partners, the team has been successful in establishing the wafer processing capabilities defined in Task 2.1 and have delivered 6-inch SiC wafers to device partners that contain functional devices. Outsourced processes have been brought in-house as equipment is installed and qualified providing the foundation for cost and cycle time improvements.

Technology to Market: As a make function, X-FAB's contributions to Technology to Market center around the ability to enable our device customers to quickly bring their products to market, reduce their costs and continue to innovate with both process and design optimizations.

Plans for Next Budget Period If Funded: X-FAB plans to purchase and install a high temperature Al implanter in BP2. With this final piece of equipment, the X-FAB Texas SiC pilot production line will have capability to fully process SiC Power Device wafers without relying on outsourced steps. Eliminating reliance on outsourcing is critical to meeting the pricing targets established by the PowerAmerica. X-FAB also plans to add inspection tools in BP2. Given the high cost of starting SiC Epiwafers, the cost of scrap is more significant than with Silicon. To reach the PowerAmerica pricing targets, the following inspection tools will be required to support Yield Enhancement and process control improvement activities.

- Patterned Wafer Defect Inspection Tool
- Un-patterned Film Defect Inspection Tool
- Film Thickness Ellipsometer

X-FAB also plans the continued development of Generic Unit Processes that has been started in Budget Period 1. The proposed generic unit processes for development in BP2 are:

- Self-Aligned Channel Implant Mask (2-Stage)
- Diode ILD (SiN and/or SiO2)
- Backside Ohmic Metal and Laser Anneal
- Schottky Contact (Surface preparation, metal deposition and anneal)
- Polysilicon Gate Formation
- Backside Metal Stack

Project Output: The primary output of Task 2.1 is to establish the manufacturing capability and cost structure that will enable the success of SiC device partners and

accelerate the adoption of WBG devices in the market. We have however delivered several technical reports to PowerAmerica as output of Task 2.1:

- High temperature implant ROI analysis report evaluating high temperature implant options for foundry operations
- Process Installation Kit Specifications
  - Generic Unit Process Specification – Polyimide Protective Overcoat
  - Generic Unit Process Specification – Frontside Power Metal (4um)
  - Generic Unit Process Specification – Frontside Power Metal (5um)
  - Generic Unit Process Specification – SiC MOSFET ILD Layer
  - Generic Unit Process Specification – Implant Blocking Oxide Hard Mask

Milestone Summary

Milestone No.	Short Title	Due Date	Status (complete/incomplete, notes)
2.1.1.1	High temperature anneal (HTA) furnace, backside metal deposition (BSM), and backside grinding (BG) tool ordered	30-Apr-15	Complete (Feb 18, 2015)
2.1.1.2	Backside laser anneal (BSLA) tool ordered	31-Jul-15	Complete (June 1, 2015)
2.1.1.3	Site work for BSM tool	31-Jul-15	Complete (May 13, 2015)
2.1.1.4	Site work for HTA furnace and BG tool	31-Oct-15	Complete (Aug 17, 2015)
2.1.1.5	Installation of BSM tool and BG tool	31-Oct-15	Complete (June 12, 2015)
2.1.1.6	Qualification of BSM tool	31-Oct-15	Complete (Oct 24, 2015)
2.1.1.7	Installation of HTA furnace and BSLA tool	31-Mar-16	On schedule
2.1.1.8	Qualification of HTA furnace and BG tool	31-Mar-16	On schedule
2.1.2.1	High temperature implant ROI analysis report	31-Oct-15	Complete (June 10, 2015)
2.1.2.2	Phase 1 of the ROI analysis report plan	31-Jan-16	On schedule
2.1.3.1	Qualification of NO furnace and N2 implant conversion	30-Apr-15	Complete (April 9, 2015)
2.1.3.2	SiC wafer handling conversion plan	30-Apr-15	Complete (April 30, 2015)
2.1.3.3	Phase 1 SiC wafer handling conversion plan	31-Jul-15	Complete (Aug 4, 2015)
2.1.3.4	Phase 2 SiC wafer handling conversion plan	31-Oct-15	Complete (June 30, 2015)
2.1.3.5	Phase 3 SiC wafer handling conversion plan	31-Mar-16	On schedule
2.1.4.1	Standard Device Foundry Development Agreement	30-Apr-15	Complete (June 24, 2015)
2.1.4.2	Standard Device Foundry Supply Agreement	31-Jul-15	Complete (July 28, 2015)
2.1.4.3	IP Protection Plan	31-Jul-15	Complete (Oct 24, 2015)
2.1.5.1	Process Installation Kit specification document	30-Apr-15	Complete (April 30, 2015)

Milestone No.	Short Title	Due Date	Status (complete/incomplete, notes)
2.1.5.2	Phase 1 of the generic unit process development	31-Jul-15	Complete (July 31, 2015)
2.1.5.3	Phase 2 of the generic unit process development	31-Oct-15	Complete (Oct 29, 2015)
2.1.5.4	Phase 3 of the generic unit process development	31-Mar-16	On schedule
2.1.5.5	Cycle time goals	31-Mar-16	On schedule
2.1.6.1	Thin Wafer Handling Roadmap	31-Jan-16	On schedule